High-Performance W-Band SiGe RFICs for Passive Millimeter-Wave Imaging

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Abstract **— A W-band square-law detector was implemented in a commercial SiGe 0.12μm BiCMOS process (IBM8HP, f_t = 200 GHz) and was integrated with a SiGe LNA and SPDT switch. The combined LNA+Detector is 0.26 mm^2, achieves a peak responsivity of ~4 MV/W at 94 GHz with a minimum NEP < 0.02 pW/Hz$^{1/2}$, and consumes 29 mA from a 1.2 V supply. A low-loss W-band SPDT is also integrated on some designs for an internal 50 Ω reference. The chip can achieve a temperature resolution of 0.3-0.4 K with a 30 ms integration time and ~ 20 GHz bandwidth. This represents, to our knowledge, the first W-band SiGe passive mm-wave imaging chip with state-of-the-art temperature sensitivity.**

Index Terms **— Millimeter waves, passive imaging, radiometer, millimeter wave imaging, millimeter wave integrated circuits, millimeter wave detectors.**

I. Introduction

Passive mm-wave imaging systems operating in the W-band or in the 140/220 GHz bands provide high spatial and temperature resolution while penetrating obscurants such as dust, fog, or clothing. Currently, these systems utilize high-gain GaAs or InP amplifiers followed by either a diode detector or a heterodyne mixer [1]. The recent development of low noise, high-responsivity zero-bias diodes [2,3] has allowed unprecedented temperature resolution with only a 20 dB gain GaAs or InP preamplifier for passive imaging arrays [4-6]. These diodes, however, are not compatible with standard GaAs or InP epitaxial layers needed for the low-noise amplifiers, and this leads to a two-chip solution. We believe that, due to the recent advances in SiGe technologies, a low cost system with high temperature resolution can be achieved at W-band using a SiGe LNA and a SiGe detector (Fig. 1). The low-noise output op-amp can also be eventually integrated on the same SiGe chip. It is also possible to integrate an SPDT switch with a reference resistor for calibration purposes using CMOS transistors (if available in the process).

The usual detector figure-of-merit is noise-equivalent power (NEP), which is the measured output noise voltage divided by the responsivity (responsivity = $Vout_{DC}/Pin_{RF}$). The NEP is related to the minimum detectable temperature difference (NEDT) by

$$NEDT = \frac{v_{rms}}{dv/dT} = \frac{NEP}{\alpha KB\sqrt{2\tau}} \qquad (1)$$

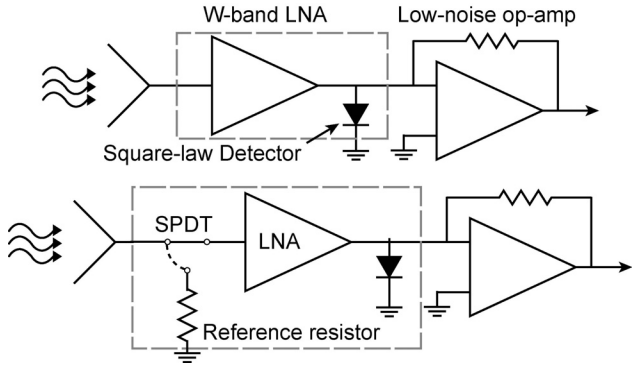

Fig. 1: Proposed receiver architectures. The circuits within the dashed boxes have been integrated on a single SiGe chip.

where v_{rms} is the output noise voltage, *dv/dT* is the change in voltage per change in target temperature, α is the pre-input attenuation, *K* is Boltzmann constant, *B* is the RF bandwidth, and τ is the integration time or frame rate [4,7]. The systems in [3-6] target NEP < 1 pW/Hz$^{1/2}$ and temperature sensitivities of 0.2-0.5 K. This paper presents a SiGe square-law detector that, when combined with a SiGe LNA, achieves state-of-the-art NEP and NEDT values (even when compared to the GaAs designs) and has a compact, low-power design.

II. Wideband W-Band LNA

A five-stage LNA was first designed using the procedure in [8], and the bias currents are chosen for low noise in stages 1 and 2 and higher gain in stages 3-5 (Fig. 2). Each stage uses four-layer metal-oxide-metal (MOM) capacitors beneath the inductive transmission line loads to provide approximately 5 pF of total supply decoupling capacitance at W-band. The fabricated LNA achieves a peak gain of 23 dB and > 20 dB gain from 86-103 GHz

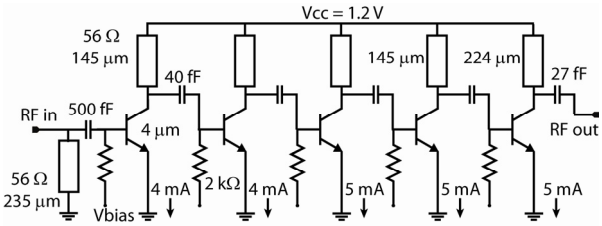

Fig. 2: LNA schematic (biasing not shown). Interstage metal-oxide-metal (MOM) caps are made between metal layers M3 and M4 in the interconnect stackup.

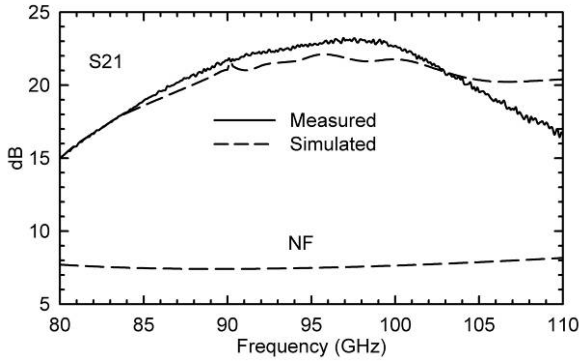

Fig. 3: Measured LNA gain with simulated noise figure.

(Fig. 3). The simulated noise figure is ~8 dB and was not measured - the noise figure of a similar LNA was measured in [8] and agreed well with simulations.

II. W-BAND SQUARE-LAW DETECTOR

A W-band square-law detector was implemented using a common-emitter BJT (Fig. 4a) with a low bias current to minimize 1/f noise. The detector is biased using a simple current mirror. A notch filter is present at the output to remove first-order response components (W-band signal), and a large output resistor (750 Ω) is used to achieve high responsivity. The fabricated detector occupies only 0.14 mm^2 including pads (Fig. 4b).

The measured detector S-parameters agree well with simulations, having a wideband input match, and one can clearly see the notch filter response in the S_{21} response (Fig. 4c). The detector NEP and responsivity were measured using a W-band tripler, an external low-noise amplifier (SRS 552), and a spectrum analyzer (Fig. 5a). The SRS amplifier has an input impedance of 100 kΩ and a noise figure of ~1 dB (1.9 $nV/Hz^{1/2}$) when driven by a 1 kΩ source. The input signal was AM modulated (100% modulation) at 400 kHz to be well above the 1/f noise corner (1-50 kHz) for transistors in this technology. The output spectrum (signal and noise) were measured using a high-performance Agilent spectrum analyzer (E4448C). Fig. 5b presents the measured and simulated NEP and responsivity of the chip. The measured output RMS noise voltage was 39 $nV/Hz^{1/2}$ at the detector output near the modulation frequency and includes the SRS 552 noise (the SRS gain was normalized out of the measurement). The detector achieves a measured of NEP of 3-4 $pW/Hz^{1/2}$ with a responsivity of 12-16 kV/W over the W-band range. The measured input P_{1dB} of the detector is -20 dBm.

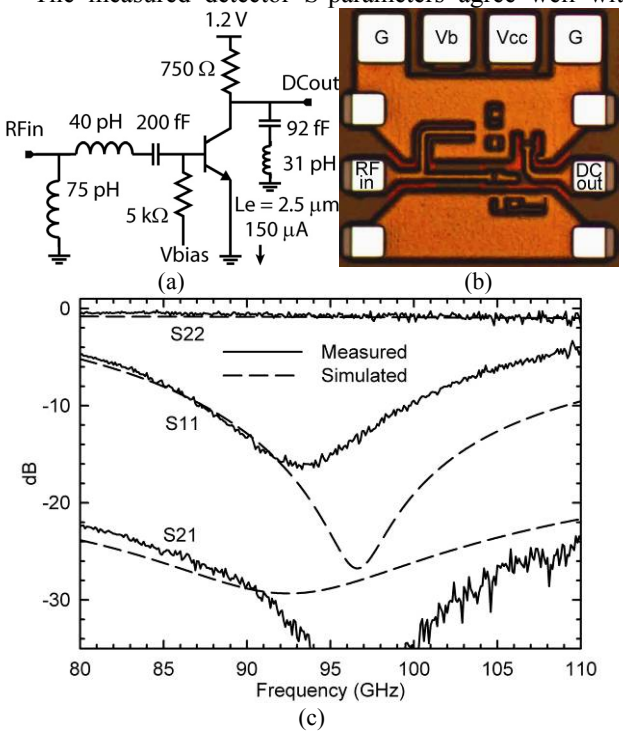

Fig. 4: (a) Detector schematic, (b) chip micrograph (386 × 370μm^2) and (c) measured S-parameters. S_{12} is << -30 dB and is not shown.

It should be noted that the noise performance of the SiGe detector can be improved by a factor of 3-5 using a smaller bias resistor in conjunction with an RF choke. At low frequencies the impedance at the base node is determined by the bias network. The low frequency noise is therefore dominated by the voltage noise from the bias network, which is multiplied by the low-frequency gain of the detector (~4 at 150 μA bias current).

It is worthwhile to consider the detector noise figure

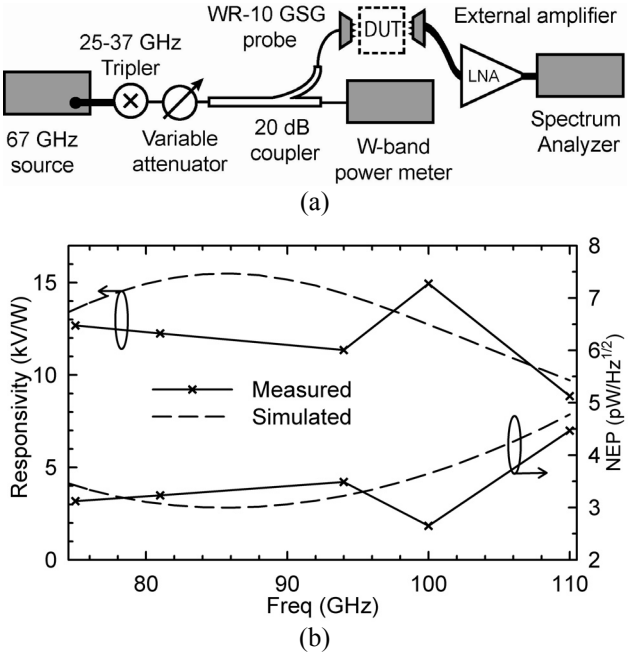

Fig. 5: (a) Test setup for noise and power measurements. (b) Detector responsivity and NEP, Pin = -42 dBm.

when considering an LNA+Detector system. The detector NF can be expressed by

$$NF = 1 + \frac{NEP}{KTo\sqrt{B}} \qquad (2)$$

where B is the RF bandwidth. Using an LNA bandwidth of 17-18 GHz, the NF of the SiGe detector is 37.5 dB. A pre-amplifier with a 23 dB gain and 8 dB NF results in a system with an input-referred NF of 15.5 dB. The LNA effectively adds only 1 dB of NF, so the system is dominated by the diode detector noise. Future designs should integrate a 30-33 dB gain amplifier for best system sensitivity.

III. W-BAND LNA+DETECTOR

The fabricated LNA+Detector chip is shown in Fig. 6. It occupies < 0.26 mm^2 with pads and consumes 29 mA from a 1.2 V supply. The composite chip is well matched at the input from 80-110 GHz (Fig. 7), and again, one can clearly see the notch filter response in S_{21}. The responsivity and noise were measured as described in Section II using an input signal modulated at 400 kHz. The output noise voltage is 49 nV/Hz$^{1/2}$, which agrees well with the simulated 51 nV/Hz$^{1/2}$ at 400 kHz. The chip has ~4000 kV/W peak responsivity, a 3-dB bandwidth of 84-103 GHz, NEP of 0.014 pW/Hz$^{1/2}$ at 94 GHz, and should have an NEDT of 0.3-0.4 K in a system with a 30 ms integration time (Fig. 8). The imaging chip works well with input power up to -40 dBm (Fig. 9). The measurements have ±1 dB accuracy due to the -20 dB coupler and attenuator calibration, and agree quite well with simulations. Results are summarized in Table 1.

A W-band noise source was also used to verify the total power responsivity of the receiver. The noise source had ENR values ranging from 20 to 14 dB from 75-110 GHz for approximately -52.3 dBm total in-band noise. This excess noise resulted in a DC output voltage difference of

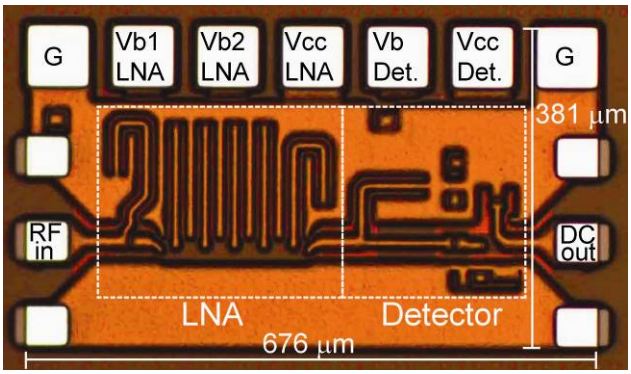

Fig. 6: LNA+Detector chip micrograph. The chip is 381 × 676 μm^2 with pads.

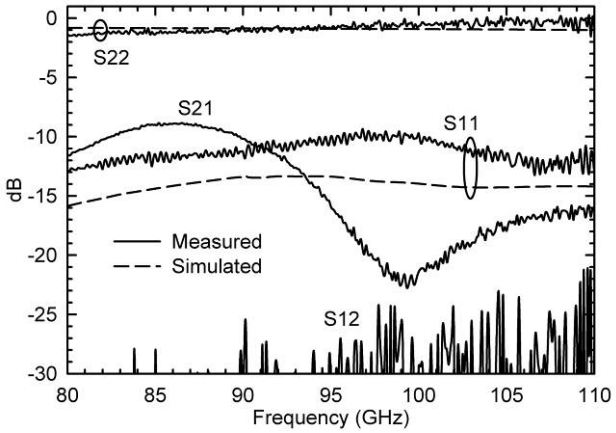

Fig. 7: LNA+Detector measured and simulated S-parameters.

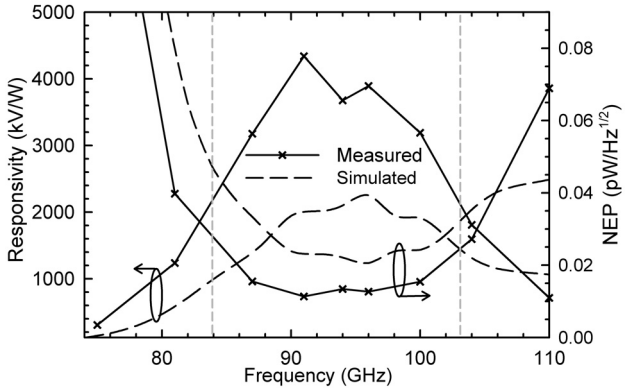

Fig. 8: LNA+Detector measured responsivity and NEP vs. frequency. Measurements done at Pin = -47 dBm.

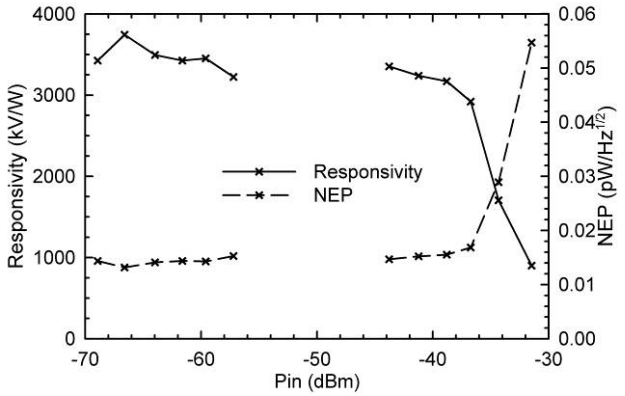

Fig. 9: LNA+Detector measured responsivity and NEP vs. input power. Measurements done at 94 GHz.

TABLE I
MEASURED LNA+DETECTOR PERFORMANCE

Size	0.26 mm^2
Current	29 mA
Supply Voltage	1.2 V
Peak Responsivity	~ 4 MV/W
3-dB Bandwidth	84-103 GHz
Output Noise Voltage	49 nV/Hz$^{1/2}$
Minimum NEP	0.012 pW/Hz$^{1/2}$
NEDT (30 ms)	0.3-0.4 K

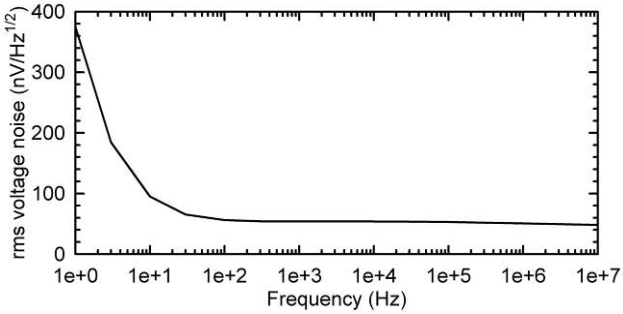

Fig. 10: LNA+Detector simulated 1/f noise. The noise floor is dominated by the 5 kΩ resistor in the detector bias network.

22.1 mV at the detector output, yielding an average LNA+Detector responsivity of 3,750 kV/W over the amplifier bandwidth and an NEP of 0.015 pW/Hz$^{1/2}$. The simulated LNA+Detector 1/f noise is shown in Fig. 8. The noise is dominated by the detector bias resistor, which results in a simulated 1/f noise corner below 100 Hz.

We are also in the process of testing a chip which integrates the LNA+Detector with a W-band SPDT switch and a 50 Ω reference resistor (Fig. 11). The reflective λ/4-based SPDT has a measured 2.8 dB insertion loss, 19 dB isolation, and 84-102 GHz matching bandwidth (Fig. 12), and has a topology similar to the GaAs SPDT presented in [9] and SiGe SP4T in [10]. Measured responsivities are ~2000 kV/W at 94 GHz and agree with

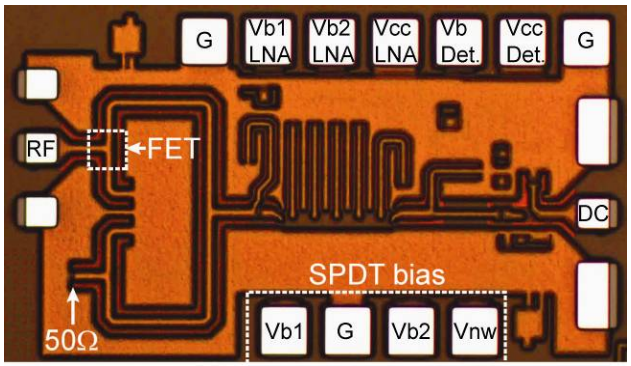

Fig. 11: SPDT+LNA+Detector chip micrograph. The chip is 918 × 531 μm^2 with pads.

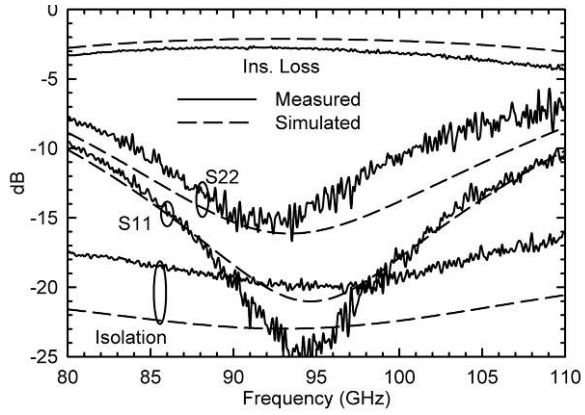

Fig. 12: Measured and simulated SPDT switch S-parameters.

simulations.

IV. Conclusion

A low-noise square-law detector has been implemented in SiGe and combined with a SiGe LNA to form a compact W-band passive imaging system. This is, to our knowledge, the only W-band SiGe imaging chip in existence. Future designs will focus on removing the input noise from the bias network and increasing the LNA gain for ~10x improvements in performance.

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