A Scalable High Frequency Noise Model for Bipolar Transistors with Application to Optimal Transistor Sizing for Low-Noise Amplifier Design

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ABSTRACT: Fully scalable, analytical HF noise parameter equations for bipolar transistors are presented and experimentally tested on high speed Si and SiGe technologies. A technique for extracting the complete set of transistor noise parameters from Y parameter measurements only is developed and verified. Finally, the usefulness of the noise model is demonstrated in the design of tuned LNAs in the 1.9GHz, 2.4GHz, and 5.8GHz bands.

INTRODUCTION

The recent boom in wireless consumer applications has emphasized the requirement for low-cost, highly integrated RF parts. Steady improvement in transistor performance, and desire for higher level of integration have lead to the increased application of silicon technology. Since substrate and interconnect losses are significantly higher in Si than in GaAs, Si RF circuit design should target the optimization of the size of transistors in order to simplify matching, rather than design the matching circuit around a given transistor. Such an approach requires a physically based, scalable compact model for bipolar transistors [1], as well as accurate, closed-form noise parameter equations, suitable for circuit design.

In the first part, expressions for the four noise parameters of a bipolar transistor are derived. The accuracy of these equations is investigated using scalable variants of the HICUM and Spice Gummel Poon (SGP) models and measured transistor noise data. Next, a technique is presented for extracting the complete set of noise parameters from measured Y parameters only. It avoids the inaccuracy of on-wafer noise parameter measurements which is especially severe for small geometry devices or devices biased in the sub-mA range. Finally, the scalable noise model is applied in the design of tuned LNAs in the 2-6 GHz band.

NOISE PARAMETER EQUATIONS

Equations (1)-(3), describing the noise resistance, R_n, optimum source admittance, Y_{sop}, and minimum noise figure, F_{MIN}, were derived as functions of the shot noise current sources, transistor Y parameters, series emitter resistance, r_E, and total base resistance r_B, in a manner similar to that employed for GaAs MESFETs [2]. The bias current dependence of the noise parameters appears in explicit form via the I_B and I_C terms, and also implicitly in r_B and in the Y parameters. V_T represents the thermal voltage. In the derivation of eqns. (1)-(3) it is assumed that the base and collector noise currents are uncorrelated. This is a reasonable simplification given the different physical origins of the two noise currents. Since noise-specific parameters are not present in eqns. (1)-(3), it follows that noise measurements are not required to obtain the transistor noise parameters.

$$R_n = \frac{I_C}{2V_T|Y_{21}|^2} + \left(r_E + r_B\right) \qquad (1)$$

For the bias currents and frequency range used in wireless design, the noise parameter equations can be recast in easy-to-interpret formats (4)-(6). These can be employed to tailor the device size - typically only the emitter length l_E - to achieve optimal low-noise matching at the desired frequency and input impedance. As indicated by eqns.(4) and (5), the noise resistance and optimum noise admittance scale as l_E^{-1}, and l_E respectively. β_0 is the dc current gain and n is the collector current ideality factor.

$$Y_{sop} = \sqrt{\frac{I_B|Y_{21}|^2 + I_C|Y_{11}|^2}{2V_T|Y_{21}|^2\left(r_E + r_B\right) + I_C} - \left(\frac{I_C Im\{Y_{11}\}}{2V_T|Y_{21}|^2\left(r_E + r_B\right) + I_C}\right)^2} - j\frac{I_C Im\{Y_{11}\}}{2V_T|Y_{21}|^2\left(r_E + r_B\right) + I_C} \qquad (2)$$

$$F_{MIN} = 1 + \frac{I_C}{V_T|Y_{21}|^2}\left(Re\{Y_{11}\} + \sqrt{\left[1 + \frac{2V_T|Y_{21}|^2\left(r_E + r_B\right)}{I_C}\right]\left[|Y_{11}|^2 + \frac{I_B|Y_{21}|^2}{I_C}\right] - \left(Im\{Y_{11}\}\right)^2}\right) \qquad (3)$$

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$$R_n \cong \frac{n^2 V_T}{2I_C} + \left(r_E + r_B\right) \sim l_E^{-1} \qquad (4)$$

$$Y_{sop} \cong \frac{f}{f_T R_n}\left\{\sqrt{\frac{I_C}{2V_T}\left(r_E + r_B\right)\left(1 + \frac{f_T^2}{\beta_0 f^2}\right) + \frac{n^2 f_T^2}{4\beta_0 f^2}} - j\frac{n}{2}\right\} \sim l_E \quad (5)$$

As long as the length-to-width ratio (l_E/w_E) of the emitter stripe is larger than 10, F_{MIN} remains invariant to changes in emitter length.

$$F_{MIN} \cong 1 + \frac{n}{\beta_0} + \frac{f}{f_T}\sqrt{\frac{2I_C}{V_T}\left(r_E + r_B\right)\left(1 + \frac{f_T^2}{\beta_0 f^2}\right) + \frac{n^2 f_T^2}{\beta_0 f^2}} \quad (6)$$

All noise parameters are non-linear functions of emitter width, w_E, via the $I_C(r_E+r_B)$ term. The ability to predict the impact of (statistical) emitter width and length variations on the noise parameters depends on the availability of a physically based, scalable compact model. In this paper, scalable variants of HICUM [1] and of the SGP models have been used. In the case of the SGP model, a subcircuit was employed to reflect the distributed nature of the base resistance, and the physical partitioning of the base-emitter and base-collector capacitances [3]. This makes the SGP model scalable at low and moderate currents. Unlike the SGP model, HICUM accurately predicts output conductance (non-linear effects) and has built-in avalanche and self-heating. In the low-noise regime however, HICUM and SGP-modeled transistor characteristics are practically indistinguishable.

While noise parameters are available from the postprocessor of microwave circuit simulators such as LIBRA, only equivalent noise voltages and currents can be modeled directly using SPICE-like simulators. To circumvent this problem, an HSPICE input deck was developed, using eqns. (1)-(3) to simultaneously compute F_{MIN}, f_T, f_{MAX}, R_n, Y_{sop} as functions of I_C, in a single simulation run. The HSPICE-calculated noise parameters were found to agree within 0.25dB, up to 10GHz, with those generated by LIBRA.

EXPERIMENTAL

Automated, on-wafer noise parameter measurements were carried out in the 2-6 GHz range using an NP5 measurement system from ATN Microwave Inc. Devices with variable widths, lengths, and with single- or multi-stripe geometries have been investigated in three technologies: 1) a single-poly BiCMOS npn; 2) NT25, Northern Telecom's self-aligned, double-poly, implanted-base, Si npn, and 3) IBM's self-aligned, double-poly SiGe HBT [4]. The peak cutoff frequencies at V_{CE}=2V are 20, 26 and 45GHz, respectively, while typical f_{MAX} values are 27, 47 and 65GHz, respectively. Measured and SGP-modeled F_{MIN}, associated power gain G_A, f_T, and f_{MAX} are compared in Fig.1 as functions of the collector current for a 0.65x25 μm^2 single-poly bipolar transistor. The agreement is well within the typical on-wafer noise measurement error. The minimum noise current density is almost independent of V_{CE} and emitter length, but increases weakly with frequency. It is typically 6-10 times smaller than the peak f_T current density. The simulation results were obtained with a set of SGP model parameters extracted from dc and S parameter measurements on the modeled device. No fitting of the noise measurement data was performed, thus confirming the accuracy of eqns. (1)-(3).

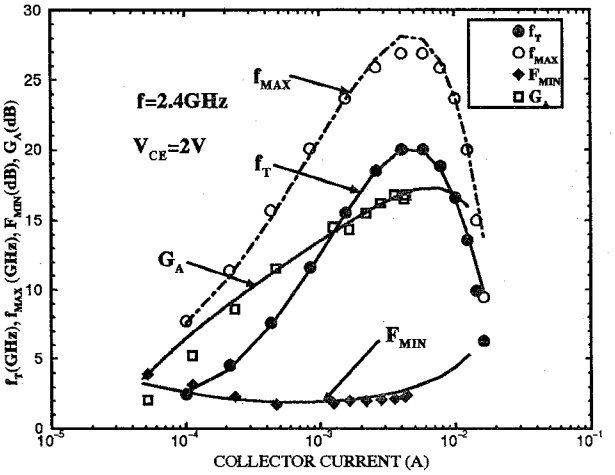

Fig.1: Measured (symbols) and SGP-modeled (lines) F_{MIN}, f_T, f_{MAX}, G_A vs. I_C for a 0.65x25μm^2 single-poly npn.

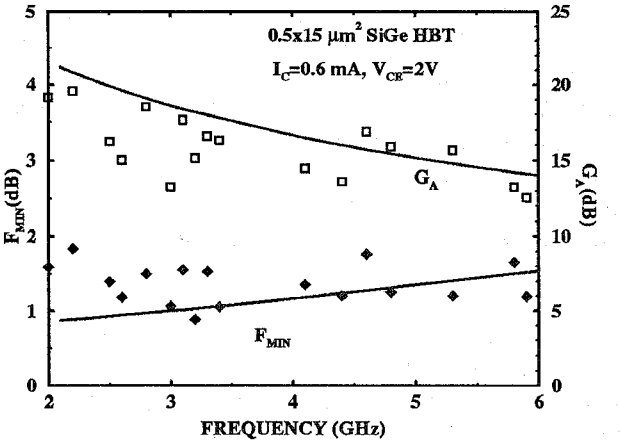

Fig.2: Measured (symbols) and modeled (lines) F_{MIN}, G_A for a 0.5x15μm^2 double-poly SiGe HBT at minimum noise bias.

The measured and modeled frequency dependence of the noise parameters is plotted in Fig.2 for a 0.5x15 μm^2 SiGe HBT biased close to the minimum noise current. The rate of F_{MIN} degradation with frequency is inversely proportional to f_T. The scatter in the measured data is due to the fact that the current NP5 system is unable to provide a controlled number of high impedance source states in a specified region of the Smith Chart, as required by a small device with typical optimum source reflection coefficients larger than 0.8.

Alternatively, we propose to use eqns.(1)-(3) to determine the noise parameters of the transistor (F_{MIN}, R_n, Y_{sop}) from measured Y parameters *only*, eliminating the

need for lengthy and "noisy" on-wafer noise measurements. Such a possibility of measuring the 50Ω noise figure has been suggested earlier [5]. Here, it is extended to the complete set of noise parameters. r_E and $r_B(I_C)$, which are required in addition to the Y parameters, are obtained as follows. r_E is determined from the frequency and collector current dependences of the real part of the measured Z_{12} characteristics, and $r_B(I_C)$ is extracted from the real part of $(Z_{11}-Z_{12})$. This technique was implemented in HP-EESOF's device characterization software package, ICCAP, and provides f_T, f_{MAX}, F_{MIN}, R_n, Y_{sop}, and G_A data from the same set of measured Y parameters. It also elegantly solves the noise parameter de-embedding problem since the Y parameters have already been de-embedded using a conventional 2-step shunt-series technique. Fig.3 presents measured and modeled data for the SiGe HBT emphasizing the impact of the r_B(Ic) model on F_{MIN}. The agreement with the noise measurements in Fig.2 is very good. In Fig.4, this simple measurement technique is used to investigate the measured and modeled emitter width dependence of f_T, f_{MAX} and F_{MIN} for double-poly NT25 Si BJTs.

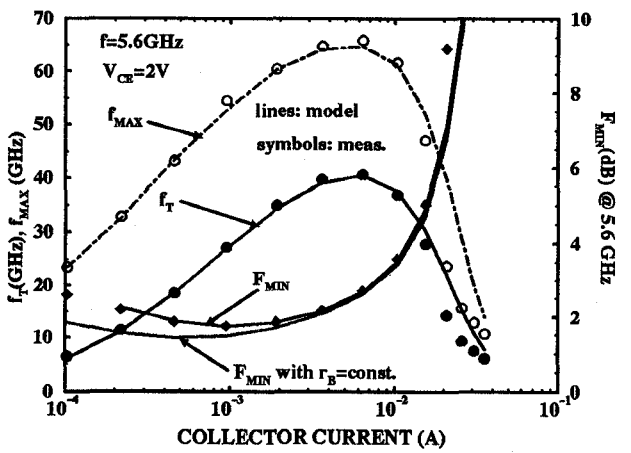

Fig.3: Measured (from Y parameters) vs. modeled f_T, f_{MAX}, and F_{MIN} for 0.5x15μm² SiGe HBT, showing impact of r_B modeling.

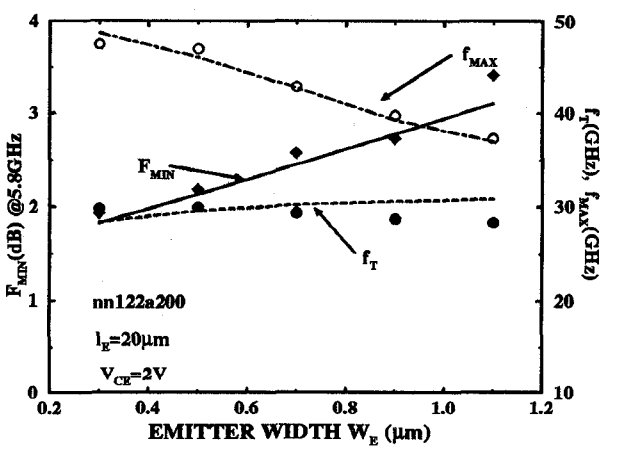

Fig.4: Measured (from Y parameters) vs. modeled peak f_T, f_{MAX}, and F_{MIN} as functions of emitter width, for NT25 Si BJTs.

APPLICATION TO LNA DESIGN

Finally, the noise parameter equations are applied to the design of tuned low-noise amplifiers at 1.9GHz, 2.4 GHz, and 5.8GHz using Si and SiGe double-poly bipolar transistors. The goal of the design is to achieve simultaneous noise and input impedance match. The first step involves finding the optimal noise current density from eqn.(3) using the HSPICE deck. The emitter length is then adjusted so that the optimum source resistance, R_{sop}, equals Z_0 (50Ω) at the minimum noise current density and at frequency f, as expressed in eqn.(7).

The variation of the noise parameters with respect to emitter length is illustrated in Fig.5 for the NT25 double-poly Si process.

$$R_{sop} \cong \frac{\frac{R_n f_T}{f}\sqrt{\frac{I_C}{2V_T}\left(r_E+r_B\right)\left(1+\frac{f_T^2}{\beta_0 f^2}\right)+\frac{n^2 f_T^2}{4\beta_0 f^2}}}{\frac{I_C}{2V_T}\left(r_E+r_B\right)\left(1+\frac{f_T^2}{\beta_0 f^2}\right)+\frac{n^2}{4}\left(1+\frac{f_T^2}{\beta_0 f^2}\right)} = Z_0 \quad (7)$$

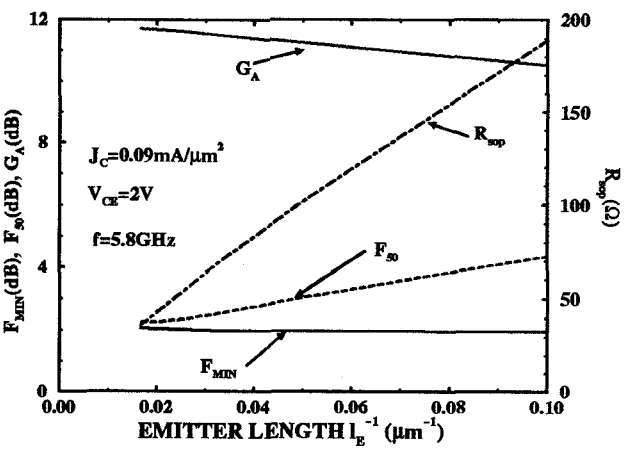

Fig.5: SGP-modeled noise parameters as functions of the emitter length, l_E, for the 0.5μm emitter, NT25 double-poly Si bipolar process at 5.8GHz. F_{50} is the noise figure in a 50Ω system.

After these two steps the transistor size and bias current are determined and the design proceeds in the conventional way [6]. An emitter inductor, L_E, is added to match the real part of the input impedance to Z_0

$$L_E \cong \frac{Z_0}{2\pi f_T} \quad (8)$$

If lossless, L_E does not change the value of R_{sop} but it does affect X_{sop} which becomes:

$$X_{sop} \cong \frac{\frac{nR_n f_T}{2f}}{\frac{I_C}{2V_T}\left(r_E+r_B\right)\left(1+\frac{f_T^2}{\beta_0 f^2}\right)+\frac{n^2}{4}\left(1+\frac{f_T^2}{\beta_0 f^2}\right)} - 2\pi f L_E \quad (9)$$

Simultaneous noise and input impedance match is finally obtained by connecting an inductor, L_B, in the base. It can-

cels out the reactance due to the input capacitance, C_{in}, of the device, and, at the same time, it transforms the optimum noise reactance of the amplifier to 0Ω.

$$L_B \cong \frac{1}{\omega^2 C_{in}} - L_E \qquad (10)$$

This design methodology guarantees optimal noise and input impedance match with the simplest matching network. The design can be completed by adding a suitable matching network in the collector in order to maximize the power gain. Simulation results obtained with LIBRA are shown in Fig.6. Table 1 illustrates several design examples at 1.9GHz, 2.4GHz, and 5.8GHz. Ideal (lossless) inductors were assumed. As expected from the noise parameter equations, the optimal transistor size and bias current decrease with increasing frequency. The SiGe HBT design achieves lower noise and higher gain with lower power dissipation.

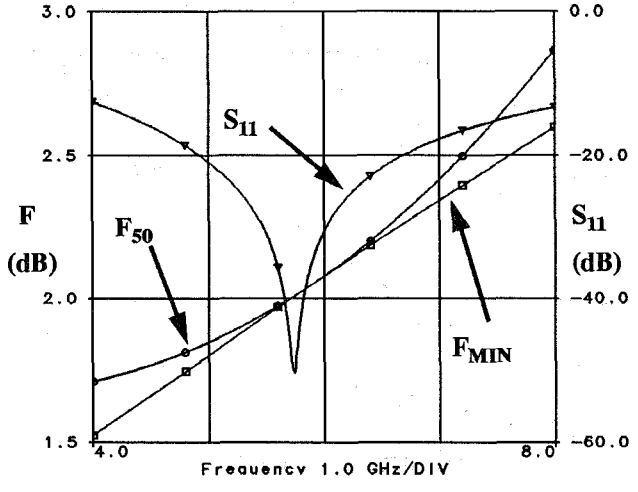

Fig.6: LIBRA simulated F_{MIN}, F_{50}, and $|S_{11}|$ for a 5.8GHz LNA employing a 2x0.5x20 μm^2 Si double-poly transistor at V_{CE}=2V.

Single transistor test structures with emitter inductors only, and with both base and emitter inductors, were fabricated in the NT25 Si bipolar process at 1.9, 2.4, and 5.8GHz. The measured data confirmed the simultaneous noise and input impedance match. The input return loss was better than -19dB in all cases. When compared to the ideal inductor simulation data, the finite Q of the fabricated inductors, typically 7-10, degraded the noise figure by 0.7-1.4dB. It was found that the base inductor contributed 0.4-0.7dB to the measured overall noise figure.

CONCLUSIONS

The capability of scalable variants of the SGP and HICUM models to accurately predict noise parameters was demonstrated using measurements and simulations on three different high-speed Si and SiGe technologies. A technique for extracting noise parameters from S/Y parameter measurements only was described. Finally, a design methodology for low-noise amplifiers was illustrated with the goal of optimizing the emitter geometry in order to minimize matching circuit losses and overall noise figure. In essence, this design methodology allows for the design of transistors that have the real part of the optimum noise impedance equal to 50 Ω at the desired frequency.

TABLE 1: 0.5 μm multiple-finger emitter, NT25 and SiGe HBT single-transistor LNA design data *at minimum noise bias* & V_{CE}=2V. Ideal inductors were used with no output matching. Cut-off and oscillation frequency values are at the low-noise bias current.

	Si npn 1.9 GHz	Si npn 2.4 GHz	Si npn 5.8 GHz	SiGe HBT 5.8 GHz
w_E, l_E	4x0.5x28μm	4x0.5x23μm	2x0.5x20μm	3x0.5x15μm
I_C	3.1 mA	2.5 mA	1.7 mA	1.4 mA
f_T	11 GHz	12 GHz	15 GHz	20 GHz
f_{MAX}	31 GHz	33 GHz	38 GHz	45 GHz
L_E	1.04 nH	1.01 nH	0.54 nH	0.45 nH
L_B	2.30 nH	1.84nH	0.60 nH	1.09 nH
F_{min}	0.87 dB	0.98 dB	2.02 dB	1.43 dB
F_{50}	0.88 dB	0.98 dB	2.02 dB	1.45 dB
G_A	15.2 dB	14.2 dB	11.1 dB	14.0 dB
$\|S_{11}\|$	-38 dB	-31 dB	-42 dB	-33 dB

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