Parameter Extraction for HBT's Temperature Dependent Large Signal Equivalent Circuit Model

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Abstract

An eleven node large signal HBT model in hybrid-π configuration is investigated which is derived from HBT topology. This is the first circuit simulation model where the temperature is introduced as a variable simulation parameter using the concept of thermal resistance and pseudotemperature to account for the temperature dependent thermal conductivity of GaAs. The temperature and bias dependence of key model parameters - thermal resistance, transit time, emitter resistance, base-emitter and base-collector junction parameters - are extracted analytically from measured DC and S-parameter data in the temperature range from 20 °C to 160 °C using on wafer thermochuck measurements. The devices have f_t and f_{max} values of 40 GHz each. The verification of the proposed model is carried out on a simple oscillator circuit at 4.7 GHz, where the temperature dependence of oscillation frequency and output power of the first three harmonics is compared to measured data.

Introduction

Temperature as a variable simulation parameter is necessary for HBT equivalent circuit models [1], [3] to describe the effects of self-heating on intrinsic equivalent circuit elements. Therefore it is necessary to measure the transistors static and dynamic thermal resistances R_{th} and C_{th} to introduce the temperature as electrical simulation parameter during circuit simulation.

Figure 1 shows the detailed HBT profile of the investigated device including all equivalent circuit elements. The transistor consists of an emitter area of $2 \cdot 20\ \mu m^2$. The p-type base - 80 nm thick - is doped with $2 \cdot 10^{19}\ cm^{-3}$ carbon. The nonlinear current gain has a value of $b \approx 100$ at a collector current density of $i_c = 3 \cdot 10^4\ A/cm^2$. The elements marked by a slash are temperature dependent. This paper describes a step by step procedure how to measure and extract the parameters and their temperature coefficients.

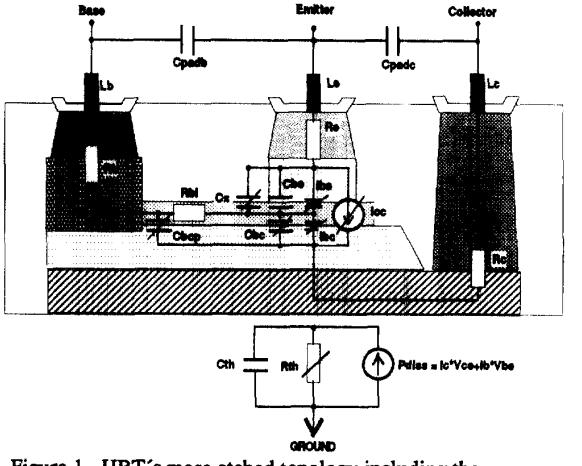

Figure 1. HBT's mesa etched topology including the equivalent circuit.

Thermal Resistance

The most temperature dependent static electrical characteristics of an HBT over a wide range of operation are the base-emitter voltage V_{be} and the collector current I_c. These two characteristics, forceing the base current and the collector-emitter voltage, are used for thermal resistance calculation similiar to the method described in [4]. Additionally, we show in Figure 2 that the thermal resistance R_{th} calculated at a constant temperature and different dissipated power levels P_{diss} has a linear dependence on P_{diss}. R_{th} at a given temperature is then defined as the value at zero power level P_{diss}. In this example of Figure 2, the regressional fit gives the value of thermal resistance R_{th} = 876 K/W at a substrate temperature of 23.5 °C. The temperature dependence of R_{th} shows a polynomial behavior of the form

$$R_{th}(T) = R_{th}(T_0) \cdot (T/T_0)^n. \qquad (1)$$

Figure 3 yields the value n=1.17 at T_0=363 K. This is in good agreement with the literature value for this parameter in GaAs of n=1.25 at room temperature T_0=300 K [6]. To take this effect into consideration for circuit simulation it is necessary to introduce a transformation from the real temperature T to

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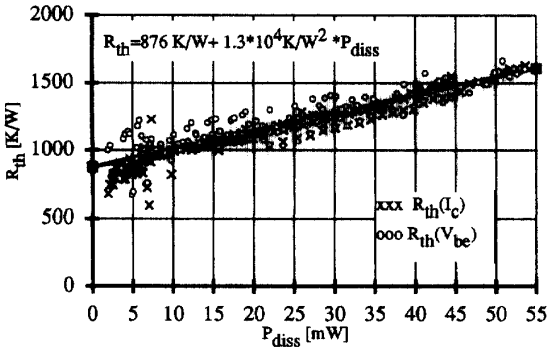

Figure 2. Dependence of R_{th} on dissipated power.

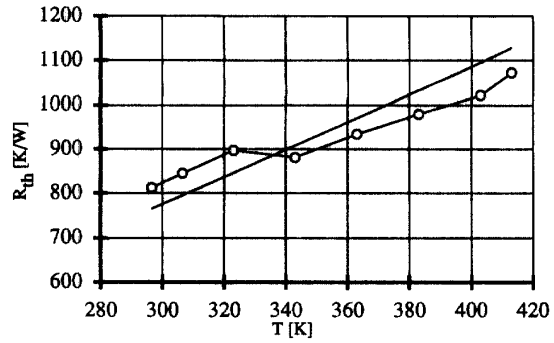

Figure 3. Measured (ooo) and calculated (——) from eq. (1) dependence of R_{th} from temperature.

the pseudotemperature τ. This transformation is choosen as

$$\tau = T_0 + R_{th}(T_0)^{-1} \int_{T_0}^{T} R_{th}(T') \, dT', \qquad (2)$$

to solve Poisson's equation for heat flux [2]. Then the transistor's pseudotemperature rise is calculated as

$$\Delta\tau = R_{th}(T_0) \cdot P_{diss} \qquad (3)$$

using the fixed value of thermal resistance at substrate temperature. To determine the actual device temperature from the pseudotemperature rise the retransformation of eq. (2), using eq. (1) and (3), gives

$$\Delta T = T_0 \cdot [(\Delta\tau / T_0 \cdot (1-n) + 1)^{1/(1-n)} - 1] \quad \text{for } n \neq 1, \text{ and}$$

$$\Delta T = T_0 \cdot (\exp(\Delta\tau / T_0) - 1) \quad \text{for } n = 1. \qquad (4)$$

To neglect the temperature dependence of the thermal resistance R_{th} produces an error of 50 K in the device junction temperature at a power density of $4 \cdot 10^5$ W/cm^2 as seen in Figure 4. This leads to an error of about 100 mV in base - emitter voltage assuming a temperature coefficient of 2 mV/K.

The dynamic time constant α for this self-heating effect is in the 1 µs range and can be determined by pulsed measurements [1], [5]. The calculated capacitance value modeling this time constant with an parallel RC circuit is therefore given as:

$$C_{th} = \alpha / R_{th}. \qquad (5)$$

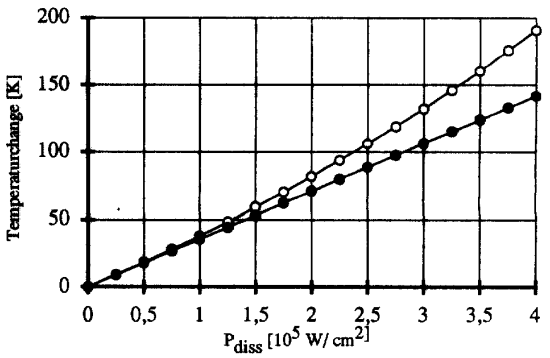

Figure 4. Difference between pseudotemperature change $\Delta\tau$ and real temperature change ΔT at different dissipated power levels.

Once the intrinsic device temperature is known, the temperature dependence of other circuit elements can be introduced into the simulation model.

DC - Extractions

DC measurements of the Gummel plot and the base-collector I-V characteristics at different temperatures between 20 °C and 160 °C are used to determine the model parameters to describe the base-emitter and base-collector junctions and the behavior of the voltage controlled current source Icc. Each of the elements describing Ibe, Ibc and Icc can be modeled using three model parameters : the maximum saturation current, the ideality factor and the activation energy.

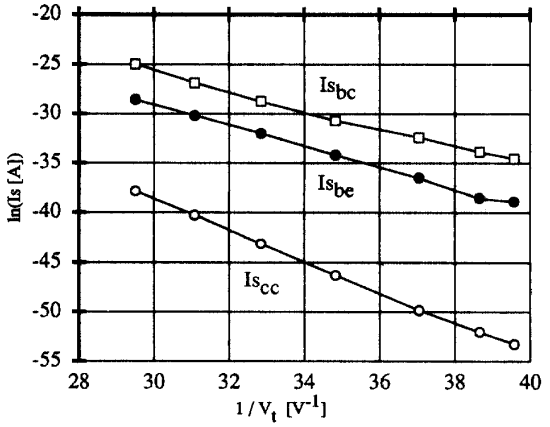

Figure 5. Temperature dependence of the saturation currents Is_{be}, Is_{bc}, Is_{cc}.

The equations describing the currents are then :

$$Ibe = Is_{be\infty} \cdot \exp(-Va_{be} / V_t) * \exp(V_{be} / (N_{be} \cdot V_t)) - 1)$$
$$Ibc = Is_{bc\infty} \cdot \exp(-Va_{bc} / V_t) * \exp(V_{bc} / (N_{bc} \cdot V_t)) - 1)$$
$$Icc = Is_{cc\infty} \cdot \exp(-Va_{cc} / V_t) * \exp(V_{be} / (N_{cc} \cdot V_t)) - 1). \quad (6)$$

The saturation currents which are defined as

$$Is_{be} = Is_{be\infty} \cdot \exp(-Va_{be} / V_t)$$
$$Is_{bc} = Is_{bc\infty} \cdot \exp(-Va_{bc} / V_t)$$
$$Is_{cc} = Is_{cc\infty} \cdot \exp(-Va_{cc} / V_t), \quad (7)$$

are extracted in the low power region of the gummel plot and the base-collector current, where the dissipated power density $p_{diss} < 1 \cdot 10^3$ W/cm^2. This corresponds to a temperature increase < 0.6 K. Therefore the self-heating effect has not to be considered. The substrate temperature dependence of these saturation currents shown in Figure 5 is used to calculate two parameters: the maximum saturation current and the activation energy.

S - Parameter Extractions

Cold S - parameter measurements under different bias conditions are used to calculate the voltage dependence of the base-emitter and the base-collector junction capacitances. The bias conditions are Ve = 0 V, Vc = 0 V with Vb ranging from -2 V to +0.8 V. Here the simpified equivalent circuit of Figure 6 can be applied to model the measured S-parameters.

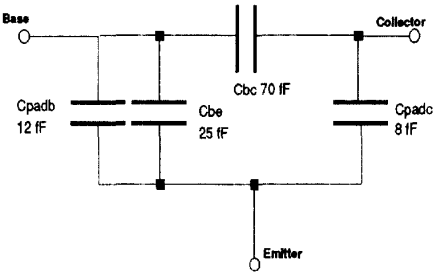

Figure 6. Simplified equivalent circuit for 'cold' S - parameter measurements. The extracted values are for the bias condition Vb = 0 V.

After converting the S-parameters to Y-parameters the junction capacitances can be expressed as

$$Cbc = - imag(Y12 + Y21) / (2 \cdot \omega)$$
$$Cbe = imag(Y11 + Y12) / (2 \cdot \omega) - Cpadb. \quad (8)$$

The value for Cpadb is extracted from an extra on wafer open test structure. The voltage dependence for these junction capacitances follows the expression of the standard SPICE gummel poon model where the built-in potential, the zero voltage junction capacitance and a grading exponent are used as model parameters. The zero voltage base-emitter junction capacitance shows no temperature dependency, while the zero voltage base-collector junction capacitance increases linearly with temperature. A 100 K temperature increase leads to a 10 % increase of this capacitance value.

The hot S-parameter measurements are used to analytically calculate the transit time, the parasitic resistances and inductances of Figure 1. This equivalent circuit can be simplified for frequencies up to 10 GHz as shown in Figure 7. DC-measurements are additionally used to calculate the

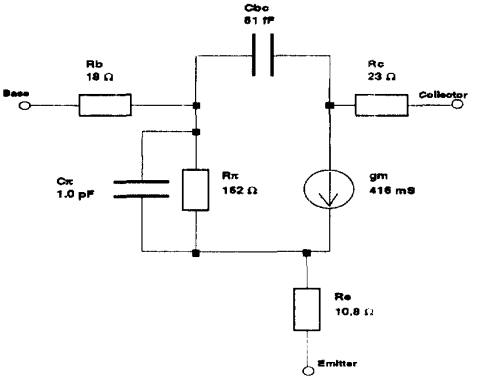

Figure 7. Simplified HBT equivalent circuit for 'hot' S - parameter measurements. The extracted values are for the bias condition Vc = 2 V and Ib = 0.13 mA.

intrinsic device temperature using equations (3) and (4). Then the transconductance and the differential base-emitter conductance can be determined:

$$g_m = I_c / (N_{cc} \cdot V_t),$$
$$g_\pi = 1 / R_\pi = I_b / (N_{be} \cdot V_t). \quad (9)$$

The other equivalent circuit elements of Figure 7 are expressed using Z-parameters and the abbreviations

$$u = imag(Z22 - Z12) / imag(Z12 - Z21), \text{ and} \quad (10)$$
$$v = (g_m + g_\pi)^2 + (\omega \cdot C_\pi)^2. \quad (11)$$

Using eq.(9), (10) and (11), these remaining elements are calculated as :

$$\omega \cdot C_\pi = sqrt[(u \cdot g_m - g_\pi) \cdot (g_m + g_\pi)],$$
$$\omega \cdot C_{bc} = g_m \cdot (g_m + g_\pi) / [v \cdot imag(Z21 - Z12)]$$
$$R_e = real(Z12) - (g_m + g_\pi) / v$$
$$R_b = real(Z11) - real(Z12)$$
$$R_c = real(Z22) - real(Z21)$$
$$\omega \cdot L_e = imag(Z12) + \omega \cdot C_\pi / v$$
$$\omega \cdot L_b = imag(Z11 - Z12)$$
$$\omega \cdot L_c = imag(Z12 - Z21) + 1 / (\omega \cdot C_{bc}). \quad (12)$$

The knowledge of the transconductance g_m and the diffusion capacitance C_π can then be used to determine the transistors transit time. For devices with high current gain, the transit time calculation can be simplified to

$$\tau = C_\pi / g_m \approx 1 / \omega \cdot sqrt(u). \quad (13)$$

Figure 8 shows the bias dependence of the transit time in normal operation mode. For collector-emitter voltages greater than 1.2 V, this transit time increases linearly with the collector-emitter voltage and therefore, assuming constant base-emitter voltage, with negative base-collector voltage. From the slope of Figure 8 the model parameter

$$c_V = \Delta\tau / \Delta V_{bc} = - 0.55 \text{ ps / V} \quad (14a)$$

can be extracted. This effect is attributed to the increasing base-collector space charge region with decreasing base-collector voltage which leads to a reduction of electron

velocity.

The temperature dependence of the total transit time is measured in the same way using eq. (13):

$$c_T = \Delta\tau / \Delta T = 0.0144 \text{ ps / K.} \qquad (14b)$$

The large signal diffusion capacitance has the form

$$C_\pi = I_c / (N_{cc} \cdot V_t) \cdot (\tau_0 + c_T \cdot \Delta T + c_V \cdot V_{bc}), \qquad (15)$$

using eq.(13), and the coefficient from eq.(14a) and (14b).

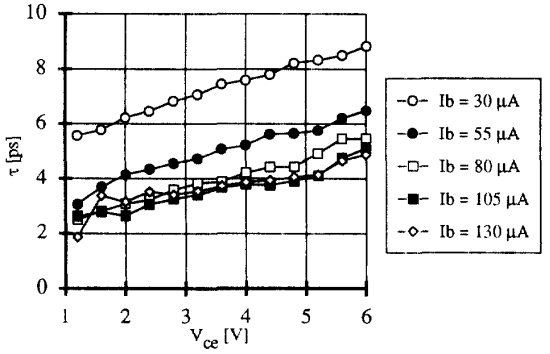

Figure 8. Transit time under different bias conditions.
F = 8.1 GHz, T_0 = 20 °C

Verification

A MMIC oscillator circuit using the same transistor in common base and series feedback configuration is used to show the capabilities of the model. First, the measured temperature dependence of the oscillators resonance frequency is compared to the simulations in Figure 9. From the measured data a temperature coefficient of

$$\Delta F / \Delta T = 2.8 \text{ MHz / K}$$

is calculated which is in good agreement with the simulations.

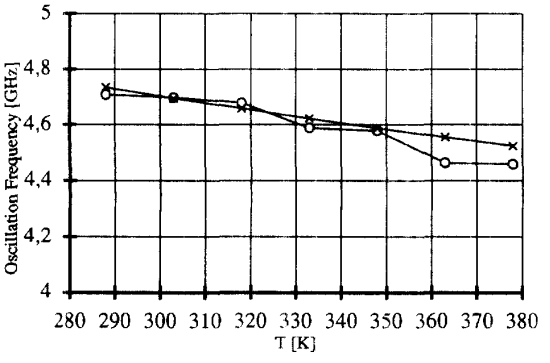

Figure 9. Measured (ooo) and simulated (xxx) oscillation frequency versus substrate temperature.

Table 1 shows a comparison between measured and simulated power levels of the first three harmonics at 300 K substrate temperature. The agreement is better than 1dB. Also the temperature dependency of the output power is investigated. In the substrate temperature range from 288 K to 382 K the first three harmonics fit with 2 dB accuracy between measured and simulated data.

measured data	simulated data
Tsubstrate = 300 K	Tsubstrate = 300 K
Osc. Freq. = 4.697 GHz	Osc. Freq. = 4.694 GHz
power(1*Freq) = 10.1 dBm	power(1*Freq) = 10.7 dBm
power(2*Freq) = -10.0 dBm	power(2*Freq) = - 9.2 dBm
power(3*Freq) = -13.4 dBm	power(3*Freq) = -13.8 dBm

Table 1. Comparison between measured and simulated oscillation frequency and power levels.

Conclusion

A consistent thermal and electrical model for GaAs/AlGaAs HBT's is presented. The model accounts for the temperature dependent thermal conductivity of GaAs using the concept of thermal resistance and pseudotemperature. Parameter extraction and measurement techniques are developed which allow analytical calculation of the most important model parameters like the transit time, the emitter resistance or the base-collector junction capacitance. The temperature dependencies of the equivalent circuit elements are investigated and implemented into the model equations.

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