Chapter 7
Integrated Beamforming Arrays

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7.1 Introduction

The advantages of using millimeter waves for communication and radar systems have been known for many years. The major impediments for the wide deployment of commercial millimeter-wave systems have been high cost and poor performance. With the advancement in silicon based processing technologies and their unprecedented device performance, it is likely that the cost of such systems will be lowered in a manner similar to other wireless communication devices such as cell phones and wireless local area network cards. Antenna arrays are used to enhance the performance of wireless communication and radar systems under various names such as phased arrays, beam-forming arrays, spatial diversity and MIMO transceivers.

As is the case with most fundamental discoveries, the origin of the antenna array is shrouded in some doubt. Some point to Nobel Prize winning scientist Guglielmo Marconi and his landmark transatlantic wireless communication experiment in December 1901 [1]. The original antennas conceived for the experiment consisted of an array of twenty aerials. These were unfortunately destroyed by devastating storms, and hence mere two-element arrays were used, through which a repeated Morse Code signal representing the letter 'S' was successfully transmitted from Poldhu in Cornwall, United Kingdom to St. Johns in Newfoundland, Canada.

The credit for the invention of the electronically-steered, linear, phased array is universally given to another Nobel Prize winning scientist Luis Alvarez. His invention was primarily motivated by the U.S. war effort in WW II and formed the basis for *Eagle*, the first radar-based bombing system. Even today, the use of phased arrays is most widespread in the realm of defense, with most warships and fighter planes

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featuring phased-array radars. An example is the AN/SPY1 phased array radar, which is a part of the U.S. Navy's *Aegis Combat System*.

The current trend of integration of phased arrays on silicon for commercial applications is characterized by a completely different set of challenges when compared to the archetypal phased array for military applications (Table 7.1). Military phased arrays are traditionally used in high-performance radar systems and hence employ thousands of elements to achieve a fine spatial resolution. Beam-scanning is used to locate and track multiple targets simultaneously. As silicon-based technologies are only recently coming into millimeter-wave capability, these phased arrays have traditionally been built using discrete components based on compound semiconductors. Unit cost is usually not a concern, and in the case of warships and, to an extent, fighter planes, size is of limited importance as well. As an example, the AN/SPY1 radar employs 68 receiving sub-arrays, each of which utilizes 2 array modules. Each array module in turn is composed of 32 radiating elements for a total of 4352 elements. The phase-shifters used are non-reciprocal, toroidal ferrite phase shifters [2].

Table 7.1 Comparison of conventional antenna arrays suitable for military applications versus those suitable for the emerging commercial applications.

	Conventional (>50 years)	**Emerging ($\approx$5 years)**
Applications	Military Radar	Wireless Communications Automotive Radar
Typical Range	Long Range ($>$ 1km)	Short Range ($<$ 100m)
Array Size	Large (100-10000)	Small (4-64)
Why an Array?	* Focussed, High-Power Beam * Multiple, Simultaneous Beams * Spatial Interference Cancellation * SNR Improvement in RX	* SNR Improvement in RX * Relaxed PA Requirement * Link Reliability (Comm.) * Spatial Selectivity (Radar)
Driver (in order)	* Performance * Size * Cost	* Cost * Size * Power Consumption
Realization	Module-based	Single Chip
Technology	III-V	Silicon

On the other hand, the burgeoning commercial applications, such as high data rate wireless communications for Wireless Personal Networks (WPANs) at 24GHz and 60GHz and vehicular radar at 22-29GHz and 77GHz, are relatively low-performance systems when compared with military systems. The link distances involved are of the order of a few meters and a fine spatial resolution is not required. As a result, these commercial phased arrays will likely employ tens of radiating elements, rather than thousands. The unit cost is a critical issue for market success, and hence, integration onto silicon-based technologies, particularly CMOS, is critical. This is rendered feasible by the lower required performance, in terms of Effective Isotropic Radiated Power (EIRP) and array sensitivity for example, and the ability of the latest generation of silicon-based technologies to handle millimeter-wave frequencies.

Further, silicon-based technologies boast the advantage of being able to integrate millions of devices onto a single chip with near-zero incremental device cost and high reliability. This can be harnessed to increase system functionality and implement calibration circuitry to fine-tune system performance at virtually no extra cost. The latter is particularly important as the packaging of single-chip antenna arrays at millimeter-wave frequencies is challenging. Specifically, the interface between the single-chip and the widely spaced off-chip antennas introduces channel mismatches that deteriorate array performance. Calibration circuitry allow for the correction of packaging mismatches, and hence can greatly reduce packaging effort and cost.

Much in the way that advancement in silicon integration and mixed-signal IC design led to the dramatic cost reduction and performance enhancement of commercial wireless communication systems, silicon based antenna arrays will play a key role toward the wide deployment of future millimeter wave communication and sensing systems.

7.2 What is a Phased Array?

A phased array is a multiple-antenna system that *electronically* modifies the direction of transmission/reception of the electromagnetic beam. This is done by introducing a variable time delay in each antenna's signal path to compensate for the path differences in free space. Fig. 7.1 depicts the block diagram of an N-channel phased array receiver. The uniform antenna spacing is assumed to be d, and each antenna's signal path contains a variable delay block, following which the different signal paths are combined. A plane-wave beam is assumed to be incident on the array at an angle of θ_{in} to the normal direction. Because of the spacing between the antennas, the beam will experience a time delay equal to $\frac{d\sin\theta_{in}}{c}$, where c is the speed of light in free-space, in reaching successive antennas. Hence, if the incident beam is a sinusoid at frequency ω with an amplitude of A, the signals received by each of the antennas can be written as

$$S_i(t) = A\cos\left(\omega(t-(i-1)\frac{d\sin\theta_{in}}{c})\right). \tag{7.1}$$

The incident plane wave experiences a *linear delay progression* in arriving at the successive antennas. Therefore, to compensate for this, the variable delay blocks must be set to a similar but reverse delay progression. Fig. 7.1 shows the i^{th} delay block set to $(N-i+1)\Delta\tau$. This would perfectly compensate for the incident progression if $\Delta\tau = \frac{d\sin\theta_{in}}{c}$. The signal in each channel at the output of the variable delay block can be written as

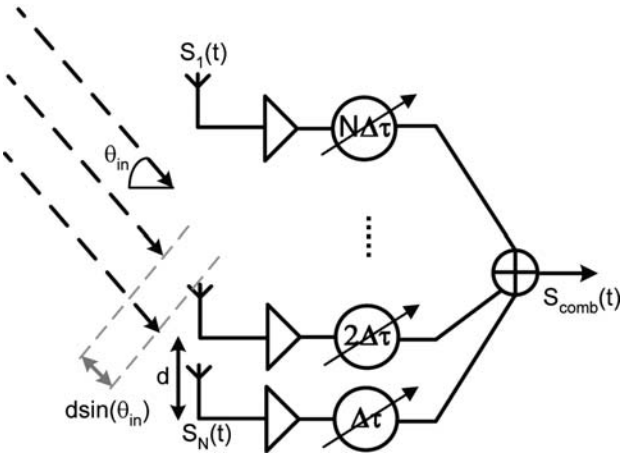

Fig. 7.1 Basic phased array receiver block diagram

$$S_{i,delayed}(t) = G \times A\cos\left(\omega(t-(i-1)\frac{d\sin\theta_{in}}{c} - (N-i+1)\Delta\tau)\right), \quad (7.2)$$

where G is the gain of each channel's front end. We are now in a position to compute the *array factor* (AF) of this phased array receiver. AF is defined as the additional power gain achieved by the phased array receiver over the power gain of a single channel. After summing $S_{i,delayed}(t)$ across the different channels and determining the ratio of the power of the summed signal to that of the signal in each channel, AF can be found as

$$AF(\Delta\tau,\theta_{in}) = \left(\frac{\sin\frac{N(\omega\Delta\tau-\frac{\omega d}{c}\sin\theta_{in})}{2}}{\sin\frac{\omega\Delta\tau-\frac{\omega d}{c}\sin\theta_{in}}{2}}\right)^2. \quad (7.3)$$

When $\Delta\tau = \frac{d\sin\theta_{in}}{c}$, an additional power gain of N^2 is achieved by the phased array as the path differences in free-space are perfectly compensated for and the received sinusoids are added coherently. AF is lower for other angles of incidence, and hence the angle of incidence of peak gain, called the beam-pointing angle, can be written in terms of $\Delta\tau$ as

$$\theta_m = \sin^{-1}\left(\frac{c\Delta\tau}{d}\right). \quad (7.4)$$

The fact that AF is lower for other angles of incidence indicates that the phased array receiver possesses spatial selectivity. This can be extremely critical in wireless

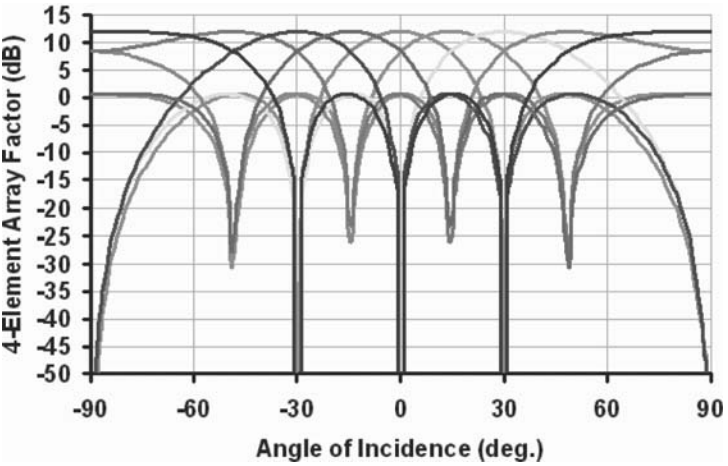

Fig. 7.2 4-channel receiver array factor for different values of $\Delta\tau$, namely $\frac{\pi}{4\omega}, \frac{2\pi}{4\omega} \ldots \frac{8\pi}{4\omega}$. The inter-antenna spacing is assumed to be $\frac{\lambda}{2}$, where λ is the free-space wavelength at the frequency of operation ω.

systems that are interference limited - a strong interferer that is located in a direction that is different from the desired transmitter can be rejected by a phased array receiver. Fig. 7.2 shows AF versus the angle of incidence for different values of $\Delta\tau$, namely $\frac{\pi}{4\omega}, \frac{2\pi}{4\omega} \ldots \frac{8\pi}{4\omega}$. A 4-element phased array receiver is considered with the inter-antenna spacing set to $\frac{\lambda}{2}$, where λ is the free-space wavelength at the frequency of operation ω. Each setting of $\Delta\tau$ results in a different beam-pointing angle. Hence, the changing of the value of the variable delay elements in each signal path allows us to electronically steer the beam[1].

From antenna theory, the beamwidth (in radians) of a radiating aperture is approximately equal to $\frac{\lambda}{D}$, where D is the width of the aperture. In the case of a linear phased array with a half-wavelength inter-antenna spacing, the total width is $(N-1)\frac{\lambda}{2}$, and hence the beamwidth is given by

$$\text{Beamwidth} \approx \frac{2}{\text{N}-1}. \tag{7.5}$$

An increase in the number of elements results in a narrower beam.

[1] $\frac{\lambda}{2}$ is the most commonly used inter-antenna spacing. A smaller spacing reduces the array's spatial selectivity. A larger spacing results in multiple main lobes.

As can be seen from the array patterns of Fig. 7.2, there are incidence angles where the received signal completely vanishes. These are called *nulls* and occur because the signals from the different channels cancel each other. In the formulation of this section, all channels are assumed to have the same gain. However, by modifying the gain of the individual channels, it is possible to arbitrarily set the location of the nulls, which is useful for interference cancellation. In addition, there are local maxima in the array pattern away from the main lobe. These are called *sidelobes* or *grating lobes*. The number of sidelobes increases with an increase in the number array elements. For the 4-element example in Fig. 7.2, there are two sidelobes, one on either side of the main lobe.

In addition to spatial selectivity, phased array receivers have the ability to improve the receiver sensitivity. In the direction of peak gain, a phased array achieves an addition power gain of N^2 over that of a single channel. However, if one assumes that each antenna picks up *uncorrelated* noise from the ambient surroundings, then the total output noise after the combining of the different channels is only N times larger than that of a single channel. Therefore, the signal-to-noise (SNR) ratio improves by a factor of N in an N-channel phased array. This SNR-improvement is also seen when the noise of the channel front-end dominates over the input noise (high noise figure receivers), as the front-end noise is uncorrelated across the different channels.

The array factor may also be viewed as the enhancement achieved over the antenna gain of a single element. In this context, phased arrays are also called *active antennas*, as the directionality of this enhancement can be electronically controlled. In the context of transmitters, the implementation of an N-channel phased array transmitter implies that each channel must generate $\frac{1}{N^2}$ times the power of a single-element transmitter to maintain the same received power level in the direction of maximum radiation. Thus, the total transmit power that needs to be generated is N times lower than the single-element case. This is specially significant in silicon-based technologies, specifically CMOS, as the low breakdown voltages render power generation challenging.

7.2.1 Case Study: A 60GHz WPAN Link Budget

As was mentioned in the introduction, there is a significant industrial and academic effort towards the deployment of 60GHz WPAN systems. One of the significant challenges for 60GHz systems is the low achievable link budget as free space path loss increases quadratically with carrier frequency. Additionally, as discussed, in the case of CMOS, the output power levels that are achievable in single transmitting elements are severely limited by the low breakdown voltages. In this case study, we examine the link budget at 60GHz and demonstrate how phased array transceivers alleviate the link budget requirement.

For indoor, dense, multipath environments, OFDM is the preferred modulation scheme due to its high spectral efficiency in these scenarios. Let us consider an OFDM signal composed of 192 data sub-carriers and 16 pilot sub-carriers with

a bandwidth of roughly 325MHz. Assuming a reasonable receiver noise figure of 10dB, the resulting sensitivity can be computed as

$$P_{noise} = -174 + 10log(325) + NF = -79dBm. \tag{7.6}$$

On the transmitter side, typical 60GHz CMOS PAs achieve output-referred 1-dB compression points of around 6dBm only[3]. Furthermore, the substantial peak-to-average power ratio (PAPR) in OFDM requires significant backoff in the PA. Assuming a backoff of 6dB, the average transmitted power is around 0dBm. The free-space path loss for a 10m link is 88dB at 60GHz. Assuming that the transmitting and receiving antennas have a gain of 5dB and an implementation loss of another 5dB, the received power can be computed to be

$$P_{RX} = 0 - 88 + 5 + 5 - 5 = -93dBm. \tag{7.7}$$

Thus, this CMOS-based WPAN link budget is deep in the negative SNR regime by 14dB. However, phased array techniques can come to the rescue. If a 8-channel phased array is employed on the transmitter side, the effective transmitter antenna gain is enhanced by 18dB. A 4-channel receiver phased array enhances SNR by 6dB. If both are employed in the link, the SNR is boosted to a positive 10dB. In addition, phased arrays offer the advantage of being able to harness alternate reflection paths, such as reflections of walls, when the direct line-of-sight (LOS) path is broken.

7.3 Phased Arrays versus Timed Arrays

As was described in section 7.2, a phased array modifies the direction of transmission/reception of the electromagnetic beam by introducing a variable time delay in each antenna's signal path to compensate for the path differences in free space. Integrated variable time delay blocks are difficult to implement in practice, particularly on silicon. Therefore, in narrowband systems, the required variable time delay is often approximated with a variable phase shift, and the variable delay elements are replaced with phase shifters. The term *phased array* is actually a misnomer when variable delay elements are used and applies to arrays that use the narrowband approximation (Fig. 7.3(b)). A more appropriate term for an array that employs variable delay elements is *timed array* (Fig. 7.3(a)).

The validity of the delay-phase approximation in phased arrays naturally depends on the instantaneous bandwidth of the system. The approximation begins to fail when the instantaneous bandwidth of the system becomes large. Since timed arrays do not employ the delay-phase approximation, their functionality is theoretically unaffected by the signal bandwidth. In this chapter, we examine the phenomenon of

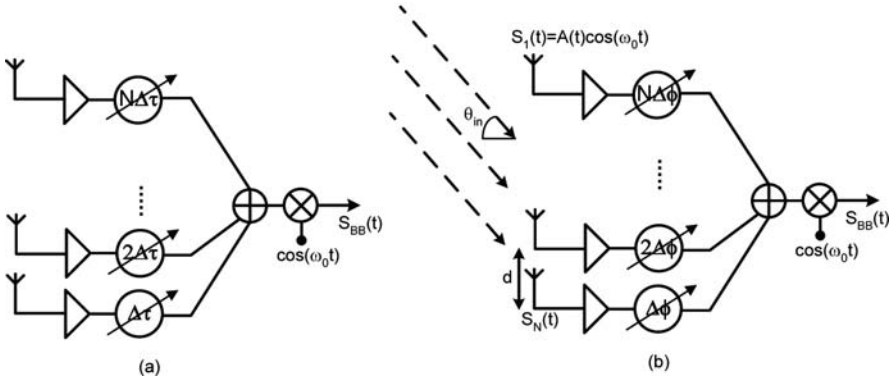

Fig. 7.3 (a) Timed array (b) Phased array.

Array-induced Inter-Symbol Interference in phased arrays, which is a direct result of this approximation.

Let us assume that an electromagnetic beam is incident on the phased array of Fig. 7.3(b) at an angle θ_{in}. If one assumes that the signal received by the first antenna is of the form $S_1(t) = A(t)cos(\omega_0 t + \alpha(t))$, then the signal received by the i^{th} antenna can be written as

$$S_i(t) = A\left(t-(i-1)\frac{d\sin\theta_{in}}{c}\right)\cos\left(\omega_0(t-(i-1)\frac{d\sin\theta_{in}}{c})+\alpha(t-(i-1)\frac{d\sin\theta_{in}}{c})\right). \tag{7.8}$$

Assuming that the antenna spacing, d, is equal to one half of the free-space wavelength at the frequency of operation, $S_i(t)$ reduces to

$$S_i(t) = A\left(t-(i-1)\frac{d\sin\theta_{in}}{c}\right)\cos\left(\omega_0 t-(i-1)\Delta\phi+\alpha(t-(i-1)\frac{d\sin\theta_{in}}{c})\right), \tag{7.9}$$

where $\Delta\phi = \pi\sin\theta_{in}$. To receive this incident beam with maximum sensitivity, the phase shifters must be set to compensate for the free-space path difference. Specifically, $\Delta\phi_i$ must be set to $(i-1)\Delta\phi$. Assuming that the second harmonic generated by downconversion is filtered out, the resultant downconverted baseband signal then becomes

$$S_{BB}(t) = \sum_{i=1}^{N}\frac{A\left(t-(i-1)\frac{d\sin\theta_{in}}{c}\right)\cos\left(\alpha(t-(i-1)\frac{d\sin\theta_{in}}{c})\right)}{2}. \tag{7.10}$$

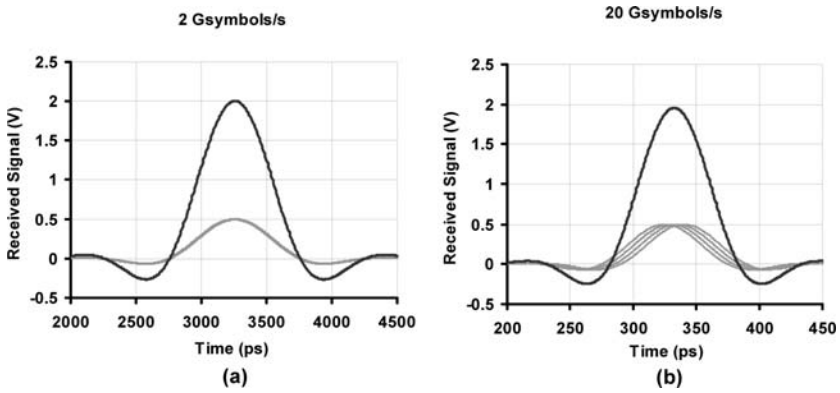

Fig. 7.4 Downconverted baseband pulses from each channel for different symbol rates. The electromagnetic beam is assumed to be incident at 36^o to a 4-element 60GHz phased array.

Equation (7.10) reveals that the delay experienced by the modulation signal in reaching the different antennas is not compensated for, resulting in an Array-induced Inter-Symbol Interference effect. This is illustrated in Fig. 7.4, which depicts simulation results from a 4-element 60GHz linear phased array. An electromagnetic beam is assumed to be incident at 36° and the phase shifters are set appropriately. The incident beam is amplitude modulated with raised-cosine-filtered baseband pulses with a roll-off factor of 0.5. For simplicity, phase modulation is assumed to be absent. Different symbol rates (and hence signal bandwidths) are considered. Fig. 7.4 depicts the downconverted baseband contribution of each channel, and the resultant combined baseband pulse. When the symbol rate is 2G/s, the uncompensated delays in the baseband pulses are negligible when compared to the pulse-width. Hence, the baseband pulses from the different channels lie virtually on top of each other and no appreciable ISI is seen. On the other hand, when the symbol rate is 20G/s, the uncompensated delays now become a significant fraction of the pulse-width. The ISI effect now becomes noticeable and the combined baseband pulse is reduced in amplitude. Since the baseband pulse-width is dependent on the signal bandwidth, and the uncompensated delays are a function of the operating frequency, it follows that the severity of the ISI-effect is dependent on the *fractional bandwidth* of the signal, which is the ratio of signal bandwidth to carrier frequency. This underscores an important motivating factor behind the push to millimeter-wave frequencies : 5GHz of ISI-free bandwidth can easily be achieved in a 60GHz phased array, but would require a true-time-delay implementation if deployed in the 3-10GHz frequency range.

The reduction in the amplitude of the combined baseband pulse can also be viewed as a decrease in the SNR. This is because the total output noise power remains unchanged with the approximation of time delays with phase shifts, if one assumes that each antenna picks up uncorrelated noise from the ambient surroundings. To quantify this SNR decrease, different symbol rates are considered and the reduction in baseband pulse amplitude and hence SNR are computed for different angles of

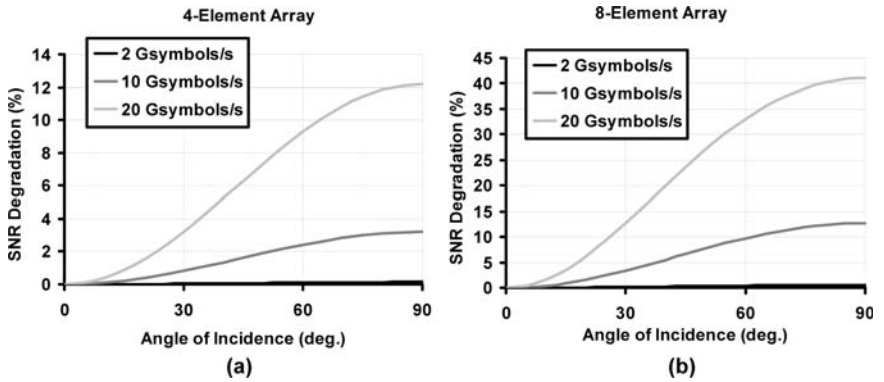

Fig. 7.5 SNR degradation due to the phase-shift approximation for different angles of incidence and symbol rates in (a) a 4-element array (b) an 8-element array.

incidence. The results are shown in Fig. 7.5. As is evident from the figure, the SNR degradation increases with the angle of incidence, as there is a larger inter-antenna delay that is uncompensated for in the information signal. The SNR degradation also increases with the symbol rate (and hence signal bandwidth) as was discussed in the previous paragraph. Finally, the SNR degradation due to the phase-shift approximation is larger for larger array sizes due to the larger delay between the first and the last antenna.

It is clear that signal bandwidths as large as 5GHz show insignificant SNR-deterioration due to the phase-shift approximation at 60GHz for the anticipated array sizes, thus eliminating the need for true-time-delay implementations. However, the 22-29GHz frequency band, allocated for short range automotive UWB radar systems, is an example of an application where a large signal bandwidth may necessitate the use of timed arrays. The radar range resolution is inversely proportional to the signal bandwidth; a signal with 5GHz bandwidth can achieve a theoretical range resolution of 3cm . A common radar signal waveform is a pulsed sinusoid. Consider a pulsed sinusoid with a center frequency of f_0 =25.5GHz and 200ps pulse width for an automotive radar system. The bandwidth of this signal is roughly 1/200ps or 5GHz. The beam width of an array with $\lambda/2$ spacing was given in (7.5). In order to have a beam width (spatial resolution) of 7.5°, a 16-element array is needed. The time delay between successive array elements, given by $\sin(\theta_{in})/2f_0$, is 16.9ps for $\theta_{in} = 60^o$. As can be seen from Fig. 7.6, there is no overlap between the signals of the last five elements (A12-A16) and the first element (A1) for the 60° incidence angle. A broadband phase shifter will align the sinusoids so that they add up coherently, only *if* they have some overlap. Delay elements are needed to shift the signals in time domain and align them. In this example, the 16-element array for the 60° incident angle will behave like a 12-element one *at best*! It should be reminded again that the need for variable true time delay element versus variable phase shifter is a function of signal fractional bandwidth, array size, and the maximum scanning angle. For a

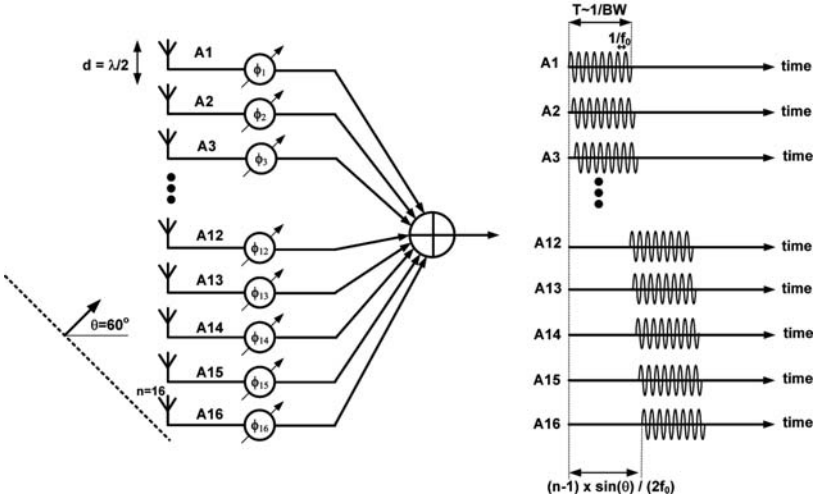

Fig. 7.6 The need for *timed arrays* in vehicular radar for 22-29GHz operation.

given fractional bandwidth, the larger the array size or the steeper the scanning angle, the more a variable true time delay element will be needed.

7.4 Conventional Phased Array Architectures

The phase-shifters required to achieve phased-array functionality can be incorporated in different parts of the transmitter/receiver chain. This results in three distinct phased array architectures - *RF Phase-shifting*, *LO Phase-shifting* and *Digital Arrays*. This chapter examines the trade-offs involved in these three architectures in detail[2]. In addition, common phase-shifter circuits for the implementation of each of these architectures in a silicon process are presented from the existing literature.

[2] Although all schematics represent receiver arrays, the basic principles apply to transmitter arrays as well.

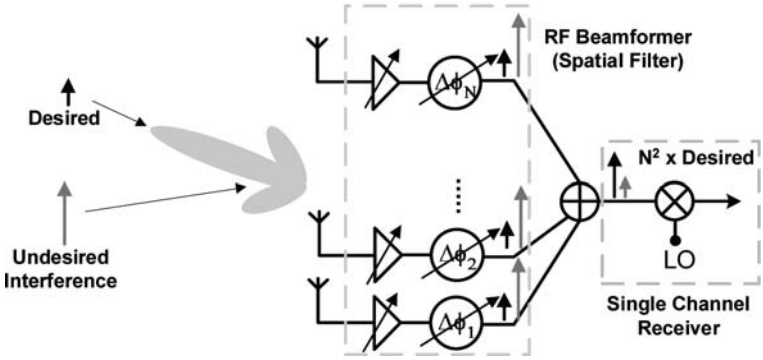

Fig. 7.7 The RF phase-shifting architecture

7.4.1 RF Phase-shifting

Fig. 7.7 illustrates the RF phase-shifting architecture for phased arrays. In this architecture, the signals in the various channel are phase-shifted and combined in the RF domain. The combined signal is then downconverted to baseband using any generic receiver such as heterodyne, homodyne or other image rejection architectures. RF phase-shifting has traditionally been the most widespread phased-array architecture because of its ability to insulate a larger portion of the receiver chain from strong, in-band interferers, as is shown in Fig. 7.7. A weak, desired signal and a strong, in-band interferer are assumed to be incident on the RF Phase-shifting array, with the interferer incident along a null direction. Since the combining point occurs prior to downconversion in this architecture, the interferer is cancelled prior to the downconversion mixer. Therefore, the dynamic range requirements on the mixer and the blocks that follow it are alleviated.

The main challenge in this architecture is the implementation of RF phase-shifters in silicon. Passive implementations tend to be lossy while active phase shifters must be designed with sufficient linearity to accomodate strong interferers. An active phase shifter with insufficient linearity essentially negates the advantage that the RF phase-shifting architecture enjoys in interference rejection. In addition, the noise performance of the phase shifter is critical as the phase shifter lies in the RF signal path and hence can potentially degrade the system noise figure. Another design choice is the implementation of variable true-time delay elements for wideband timed arrays versus phase shifters for narrowband phased arrays.

As was mentioned earlier, control of the individual channel amplitudes is desirable as it allows for the modification of the null locations in the array pattern. Since the spatial filtering is done completely in the RF domain in this architecture, the variable-gain amplifiers required for individual amplitude control must be placed in the RF domain. This is challenging as RF blocks are usually parasitic-sensitive, and hence a change in the gain usually is accompanied by a change in the phase response.

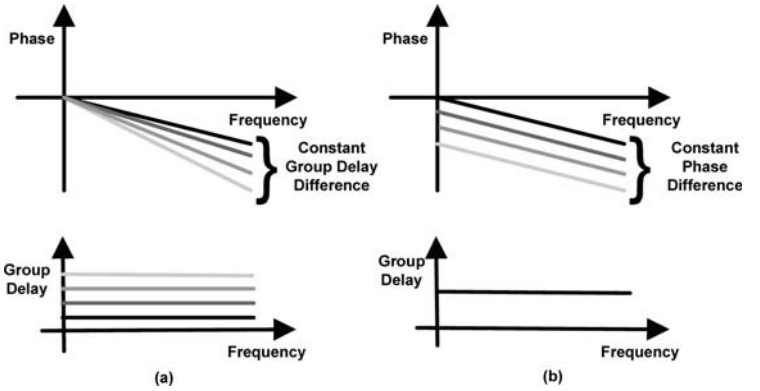

Fig. 7.8 (a) Phase and group-delay profile of a variable true-time delay element (b) Phase and group-delay profile of a broadband phase shifter.

Therefore, the RF variable-gain amplifiers must work in conjunction with the RF phase-shifters to set the null location while not altering the primary beam-pointing direction.

7.4.1.1 RF Variable True-Time Delay Elements

Variable true-time delay elements exhibit a constant group delay difference across different settings over frequency. Their use in timed arrays allows array functionality to be preserved independent of signal bandwidth. Fig. 7.8(a) shows the phase response of a variable true-time delay element. The response of a broadband phase shifter is shown in Fig. 7.8(b) for contrast. Broadband phase shifters maintain a constant phase difference between their different settings across the designed frequency range. As a result, phased arrays that employ these broadband phase shifters can only operate *in a narrow frequency range* around any center frequency in the designed frequency range.

Variable delay elements typically employ transmission-line structures. Since the delay of an electromagnetic wave in a transmission line depends on the wave velocity and the distance travelled, either one or both of these may be varied to control the delay of the RF signal. Fig. 7.9 summarizes mechanical techniques that are used to accomplish this. The *trombone line* varies the delay by mechanically changing the distance travelled by the RF signal. The name arises because its operation is similar to a trombone, where the position of a tuning slide is varied to change the tube length and hence the pitch. The wave velocity may be varied by controlling the separation between the signal and ground conductors or by modifying the nature of the dielectric between them.

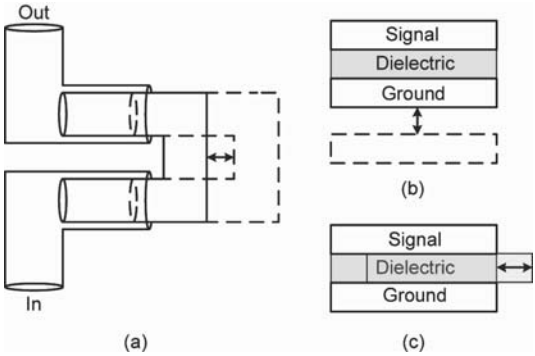

Fig. 7.9 (a) The mechanical trombone line manipulates the distance travelled by the signal (b) Manipulation of the wave velocity through control of the signal-ground separation (c) Manipulation of the velocity through control of the dielectric material between the signal and ground conductors.

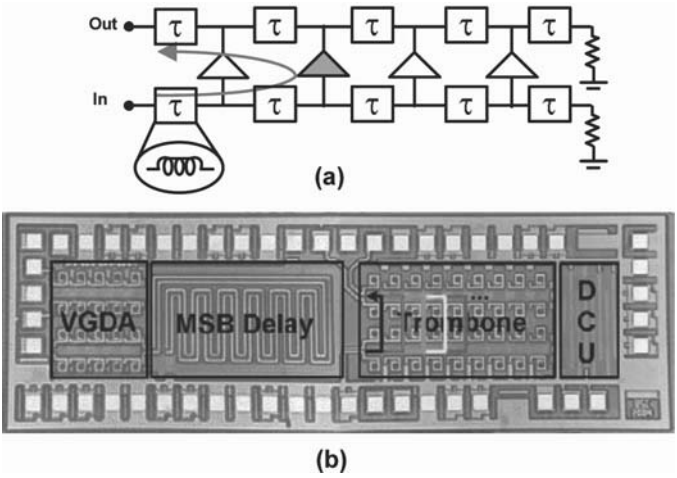

Fig. 7.10 (a) The trombone line delay element (b) A 1-13GHz UWB beamformer in a 0.18μm SiGe BiCMOS technology [5]. The beamformer employs a trombone line delay element (©IEEE 2006).

Fig. 7.10(a) depicts the electrical equivalent of the trombone line. The delay element consists of an input and an output transmission line. The transmission lines are typically implemented as lumped, quasi-distributed structures, and at each node, buffer amplifiers are employed to transfer the signal from the input to the output transmission line. At a time, only one buffer amplifier is activated and by switching between buffer amplifiers, the distance travelled by the electromagnetic signal and hence its delay are varied [3]. Fig. 7.10(b) is a chip microphotograph of a 1-13GHz

[3] The circuit diagram of the trombone line bares a strong resemblance to that of a distributed amplifier with two key differences - the output terminal is on the other end of the output transmission line and only one buffer amplifier is on at a time.

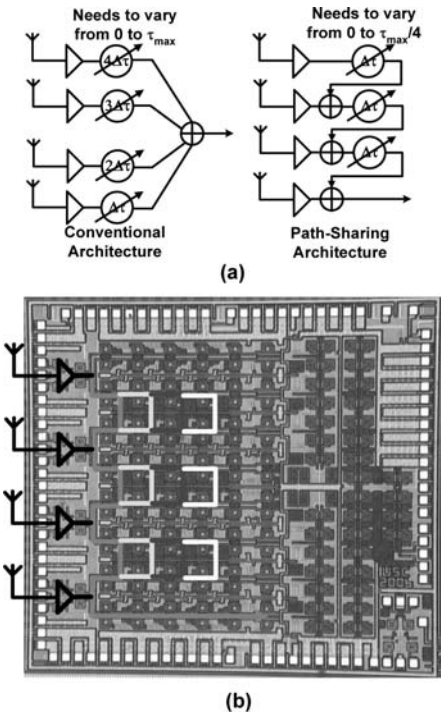

Fig. 7.11 (a) Path-sharing timed array architecture (b) A 4-channel, 0.13μm CMOS UWB beamformer employing the path-sharing architecture (©IEEE 2007).

UWB beamformer that employs a trombone line delay element and is implemented in a 0.18μm SiGe BiCMOS technology [5].

The component values for the trombone line are set by the desired characteristic impedance and delay/phase resolution. In Fig. 7.10(a), the sections of the quasi-distributed transmission line are low-pass in nature, with series inductors and shunt capacitors. The capacitors of each section are usually completely derived from the parasitic capacitances of the inductors and the buffer amplifiers. If the inductors have an inductance of L and the parasitic capacitance at each node is denoted by C_{par}, then the characteristic impedance of each line is $\sqrt{\frac{L}{C_{par}}}$. The delay resolution, or the delay difference between two sucessive buffer amplifier settings, is $\sqrt{LC_{par}}$. Therefore, if the desired delay resolution and characteristic impedance are known, the inductance value and tolerable parasitic capacitance at each node are fixed. The allowable parasitic capacitance at each node, coupled with the unity gain frequency (f_T) of the technology used, determines the amount of gain that can be achieved in the buffer amplifiers. For additional design guidelines and considerations, the reader is referred to [5]. In the UWB beamformer reported in [5], the lines are designed for

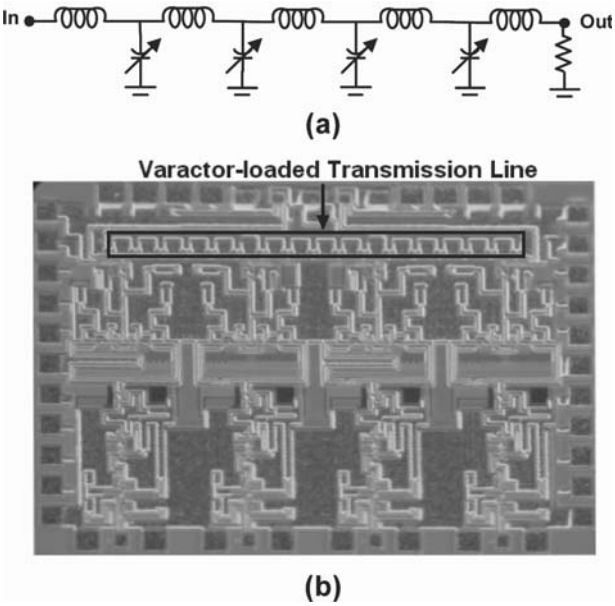

Fig. 7.12 (a) The varactor-loaded transmission line delay element. (b) A 4-element 60GHz phased array receiver in a 0.13μm SiGe BiCMOS technology employing varactor-loaded transmission line delay elements in a path sharing architecture [8] (©IEEE 2007).

a characteristic impedance of 100Ω (differential) and the delay resolution obtained is 4ps.

In order to reduce the area required by the trombone line delay elements, a *path-sharing* architecture has proposed for timed arrays in [6]. The architecture is depicted in Fig. 7.11(a) and takes advantage of the fact that a timed array requires a linear delay progression across the receiver channels. Each channel is delayed using a trombone line and is then combined with the adjacent channel, thus introducing the required delay progression. When compared with the conventional architecture, the maximum delay requirement from the trombone lines is reduced by a factor of N due to the series reuse of the lines. This results in significant area savings. Fig. 7.11(b) shows the chip microphotograph of the 4-channel, 0.13μm CMOS UWB beamformer reported in [6] that employs the path-sharing architecture. The architecture can be used with other delay elements or phase shifters as well to reduce the delay/phase requirements.

The *varactor-loaded transmission line* delay element as shown in Fig. 7.12(a). The capacitance of each section is realized in part through varactors. By varying the capacitance of the varactors, the wave velocity and hence the delay of the RF signal is varied. An unfortunate consequence of this is that characteristic impedance of the line also changes with a change in capacitance, which deteriorates the matching at the input and output terminals. Therefore, the extent of mismatch that is tolerable at

the terminals sets the allowable delay variation [4]. Another challenge that is specific to millimeter-wave implementations is the Quality Factor (Q) of varactors in silicon-based processes. Varactors, typically realized through MOS capacitors, exhibit poor Q values ($<$10 at 60GHz) at millimeter-wave frequencies[7], which results in high loss levels in the varactor-loaded transmission line. For instance, [8] reports a 4-element 60GHz phased array receiver in 0.13μm SiGe that employs the varactor-loaded transmission line delay element in the path-sharing architecture mentioned above. The path-sharing architecture reduces the requirement on each delay element to 45° of phase variation in the implementation reported in [8]. Over this phase variation range, the insertion loss varies from 2 to 4.5dB due to the loss of the varactors employed. The chip microphotograph of this phased array receiver is shown in Fig. 7.12(b).

The trombone line delay element is not a true passive delay element due to the presence of the buffer amplifiers, which limit the linearity performance. The varactor-loaded transmission line, on the other hand, is truly passive and hence highly linear[5].

7.4.1.2 RF Phase Shifters

The first RF phase shifter considered in this subsection is the *switched transmission line* phase shifter is shown in Fig. 7.13(a). The phase shifter consists of multiple, quasi-distributed, transmission-line Π-sections, combined with MOSFET switches. When the digital control bit of the first section, b_1, is high, switch M1 is open and M2 is closed. The inductor L_1 and capacitors of value C_1 then form a Π-section. Their values are chosen to yield a characteristic impedance of 50 ohms ($\sqrt{\frac{L_1}{2C_1}}=50\Omega$) and an insertion phase of 180°, the highest phase-shift bit ($\omega\sqrt{2L_1C_1}$=180°). When b_1 is low, L_1 is shorted by switch M_1. Furthermore, switch M_2 is open and its capacitive parasitics are resonated out by inductor L_{s1}. As a result, the capacitances of value C_1 are rendered ineffective and the Π-section as a whole is bypassed. A cascade of multiple, quasi-distributed, Π-sections with bypass-capability corresponding to the different phase-shift bits completes the phase shifter design. It should be noted that while this phase shifter appears to be a true-time delay element, the narrowband match between L_{s1} and the parasitics of M_2 limits its performance to that of a phase shifter.

Since the MOSFETs are used only as passive switches, this phase shifter exhibits good linearity performance. The main challenge in the design of the switched transmission line phase shifter is the loss associated with the MOSFET switches. In [9], the authors report a 4-bit switched transmission line phase shifter operating from 30-

[4] Alternately, the load impedance can be varied to maintain matching. However, this involves incorporating input impedance tunability in the following stage, and it would have to be accomplished without modifying the phase response of that stage.

[5] The varactors in the transmission line have a voltage-dependent capacitance that is a source of nonlinearity. However, for this delay element, compression of the output amplitude and variations in the output phase tend to occur only at extremely high power levels and are seldom sources of concern.

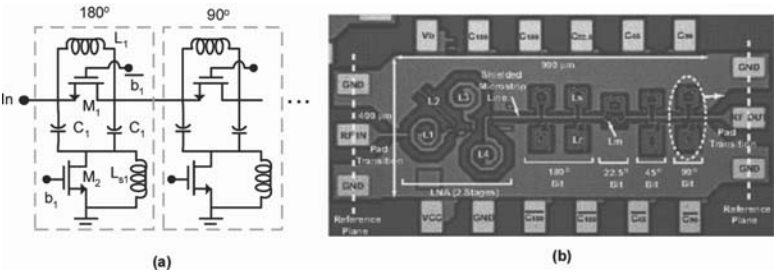

Fig. 7.13 (a) Switched transmission line phase shifter concept (b) Chip microphotograph of a 30-38GHz LNA and switched transmission line phase shifter implemented in a 0.13μm SiGe BiCMOS process [9] (©IEEE 2007).

38GHz and implemented in a 0.13μm SiGe BiCMOS technology. The phase shifter is preceded by an LNA that exhibits 15dB of gain at 34GHz. The insertion loss of the phase shifter is reported to be around 13dB from 30-38GHz and the overall insertion loss of the LNA-phase shifter combo is reported to be 1 ± 1.5dB across the different phase-shift states at 34GHz, including the input and output pads. Fig. 7.13(b) shows the chip microphotograph of the implemented LNA and phase shifter.

The *high-pass/low-pass* phase shifter functions by taking the difference between the phase response of a high-pass filter path and a low-pass filter path. Fig. 7.14(a) shows the schematic of the first bit of such a phase shifter. Each individual bit has a high-pass and low-pass paths, with Single-Pole-Double-Throw (SPDT) switches on both sides. Depending on the switch states, either the high-pass or the low-pass path is inserted. Therefore, across the switch states, a phase difference is created that is equal to the difference between the insertion phases of the high- and low-pass paths. Each individual bit is designed for different phase differences.

The filter elements may be designed for flat gain in the frequency band of operation and a linear phase response. The challenges include the losses in the passive elements and the switches. Additionally, the switch may increase the phase variation associated with the phase shifter. For design guidelines, the reader is referred to [10]. Fig. 7.14(b) shows the chip microphotograph of a 12GHz phase shifter implemented in a SiGe process that employs the high-pass/low-pass phase shifter for the highest (180°) bit [11].

The high-pass/low-pass phase shifter is fundamentally passive and hence exhibits good linearity performance. However, if the SPDT switches are implemented in an active manner to minimize insertion loss, a large amount of current may need to be burnt in the switches to maintain linearity performance.

Another common RF phase shifter is the *reflection-type phase shifter* (RTPS), which employs a 4-port directional coupler and purely reflective (i.e. imaginary) loads. Fig. 7.15(a) depicts an example, where the directional coupler is implemented as a branchline 3dB 90° coupler. The *through* and *coupled* ports are terminated with the reflective terminations and the isolated port is used as the output. The incident signal at the input reaches the output only through reflections at the imaginary

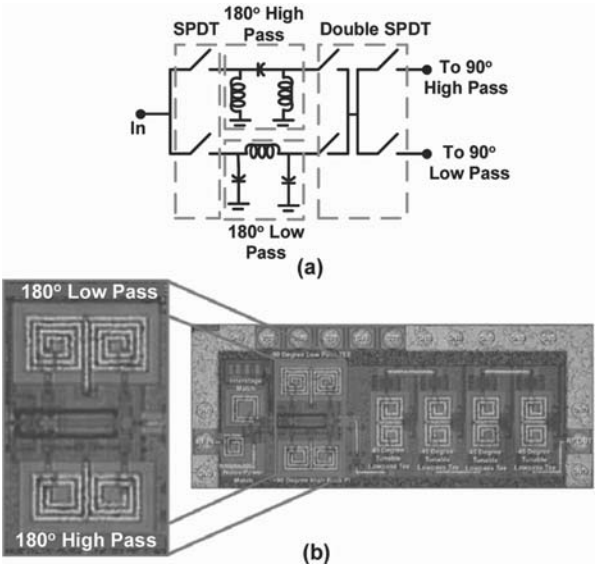

Fig. 7.14 (a) Schematic of the first bit of a High-Pass/Low-Pass phase shiter (b) A 12GHz SiGe phase shifter employing the High-Pass/Low-Pass phase shifter for the highest (180°) bit of phase shift (©IEEE 2005).

terminatons. Therefore, by varying the value of the imaginary terminations, the phase of the reflection coefficient at the through and coupled ports and hence the phase of the output are varied.

If the imaginary impedances at the *through* and *coupled* ports are denoted by jX, then the total phase shift from the input to the output is given by $-\frac{\pi}{2} - 2\tan^{-1}(\frac{Z_o}{X})$, where Z_o is the impedance to which the ports are matched. Fig. 7.15(b) plots this phase shift as a function of capacitance when the reflective terminations are implemented through varactors. The operating frequency and port impedance are assumed to be 60GHz and 50Ω respectively. To achieve a total phase variation of 180°, the termination capacitance must vary from 0 to ∞, which obviously cannot be realized through any physical varactor. Therefore, to maximize the achievable phase shift range, higher order terminations are employed, such as series LC networks. A detailed discussion on reflective termination design may be found in [12].

The RTPS, being fundamentally passive, shows excellent linearity characteristics. The main challenge in integrated, silicon-based RTPS design is loss. The two main sources of loss in an RTPS are the transmission-line losses in the directional coupler and the loss in the reflective terminations. The latter is specially significant at millimeter-wave frequencies due to the limited Q of varactors. To reduce phase shifter loss, active negative resistance circuits have been used in RTPS designs [13]. This, however, limits the linearity and noise performance of the RTPS.

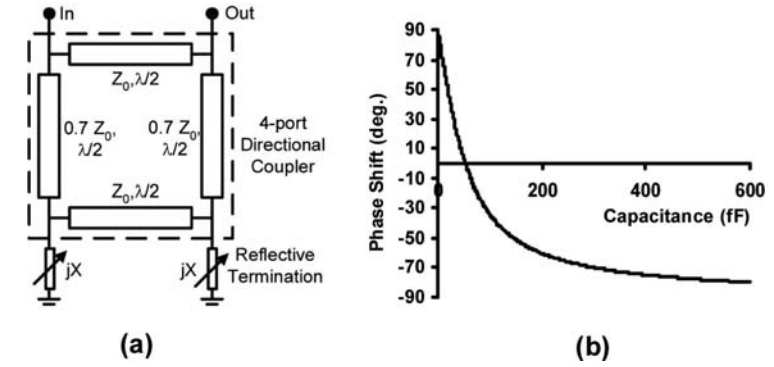

Fig. 7.15 (a) Reflection-type phase shifter (RTPS). The directional coupler in this case is implemented as a branchline 3dB 90° coupler. (b) RTPS phase shift as a function of termination capacitance.

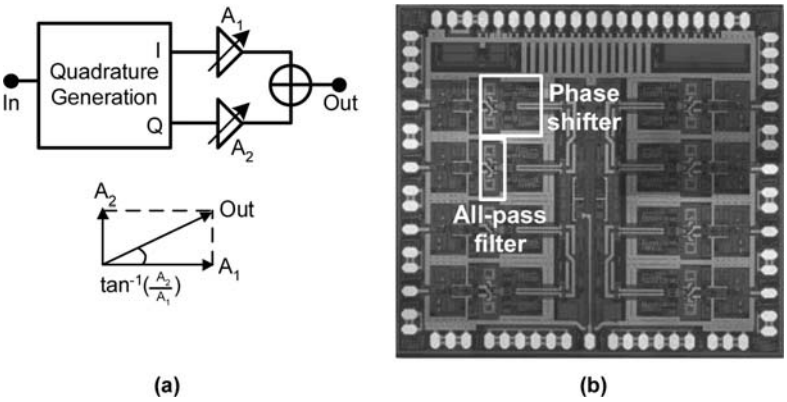

Fig. 7.16 (a) The vector-summing phase shifter (b) Chip microphotograph of an 8-element, 6-18GHz, phased-array receiver implemented in a 0.18μm SiGe process (©IEEE 2007).

The final phase shifter discussed in this subsection is the *vector-summing phase shifter*, illustrated in Fig. 7.16(a). The input RF signal is split into two components of equal power and 90° phase difference using a quadrature generation block. The two components are then amplified with variable weights using variable-gain amplifiers and combined. If A_1 and A_2 are the wieghts imparted to the 0° and 90° components, the phase of the output is $\tan^{-1}\frac{A_2}{A_1}$. Through appropriate choice of A_1 and A_2, it is possible to achieve an arbitrary phase at the output while maintaining a constant small signal gain. This phase shifter is also called a *phase interpolator*, because, in effect, an interpolation is performed between the 0° and 90° components. Other names include *Polar Modulator* and *Cartesian Combiner*.

The quadrature generation block can be implemented in a number of ways. Examples include the 90° hybrid coupler and quadrature all-pass filters (QAF). In [14], the authors report an 8-element phased-array receiver front-end that employs QAF-based phase interpolators as broadband phase shifters. A second-order all-pass network is used to generate the quadrature signals and 4 bits of variation is achieved in the phase shifter. The chip microphotograph of the 6-18GHz phased-array receiver is shown in Fig. 7.16(b). Other published works that employ this phase shifter include a 1GHz implementation in 1998 [15], a 2.4GHz system [16] and a 60GHz phased array [17].

Being an active phase shifter, the linearity performance is poor and a large power consumption is usually required to achieve a high dynamic range.

7.4.2 LO Phase-shifting

Fig. 7.17 displays the LO phase-shifting architecture for phased arrays. Since the mixing of the RF signal with the LO essentially results in a subtraction of their phases, phase-shifting of the LO of each signal path is equivalent to phase-shifting the RF signal. The advantage of this architecture over the RF phase-shifting approach is that the phase-shifters are removed from the RF signal path. As a result, the nonlinearity, loss and the noise performance of the phase-shifters no longer have a direct impact on the system performance. However, as is depicted in Fig. 7.17, strong, in-band interferers are cancelled only after the combining point, which occurs after the downconversion mixers. As a result, the mixers must have sufficient dynamic range to withstand the interferers, which usually requires a large power dissipation.

Any of the RF phase shifters presented in the previous subsection may be used in the LO path to phase shift the LO signal for each channel. In general, the performance requirements on LO-path phase shifters are more relaxed when compared to RF-path phase shifters, and hence they can be expected to consume less area/power. Other techniques, including tuned ring oscillators and coupled oscillator arrays, are also available for this architecture.

The delay-phase approximation is inherent in the LO phase-shifting architecture as the LO is a single tone and cannot compensate for the delay progression of the received signals over a wide bandwidth.

7.4.2.1 Tuned Ring Oscillators

Tuned ring oscillators can be used to generate the multiple LO phases required for this architecture [18],[19]. The tuned ring oscillator consists of a number of amplification stages, with each cell comprised of a transconducting gain cell driving a resonant load. Fig. 7.18(a) illustrates an N-element CMOS tuned ring oscillator where the transconducting gain cell is realized as a differential pair. Prior to the closing of the ring, a phase inversion is introduced. To ensure that the total phase-shift in the ring equals 0, each element must now sustain a phase-shift of $\frac{180^o}{N}$ across itself. Thus, the

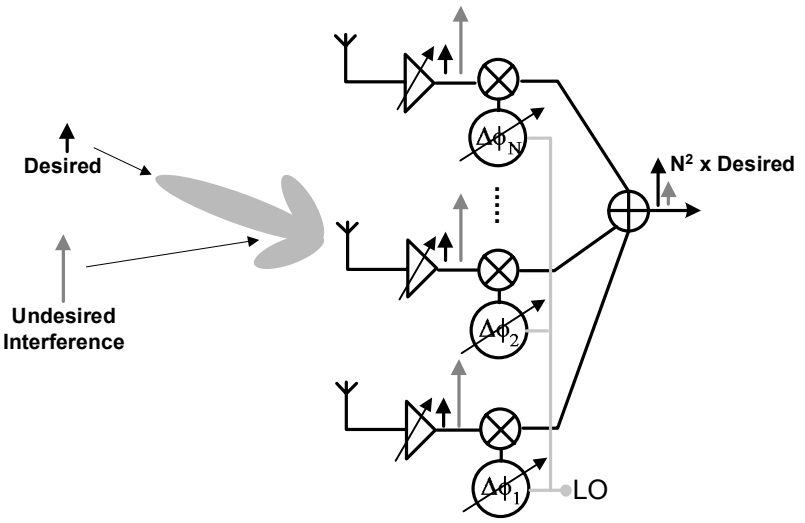

Fig. 7.17 The LO phase-shifting Architecture

different element outputs represent different phases of the oscillation frequency in steady-state. Fig. 7.18(b) depicts the different element outputs of an 8-element tuned ring, with the inter-element phase shift being $\frac{180^o}{8} = 22.5^o$. It should be noted than in an N-element tuned ring, not N but $2N$ LO phases are available, spanning the entire $0^o - 360^o$ range. This is because, due to the differential nature of the tuned ring, each element inherently offers a phase *and* its inverse.

The oscillation frequency of the tuned ring does not coincide with the center frequency of the resonant loads. In fact, the tuned ring must operate off the center frequency of the resonant loads so that each element may provide the requisite phase shift. This leads to a deterioration in oscillation amplitude and hence, phase noise, as the impedance presented by a resonant load is maximum at its center frequency. The extent of this deterioration is dependent on the inter-element phase shift, which is inversely proportional to N, the number of elements. For a detailed discussion on the phase noise of the tuned ring oscillator and design guidelines, the reader is referred to [20].

A practical challenge in the use of tuned ring oscillators is the routing of the element outputs to the different antenna signal paths. Fig. 7.18(c) depicts the chip microphotographs of a 4-channel 24GHz transmitter in 0.13μm CMOS [19] and an 8-channel 24GHz receiver in 0.18μm SiGe [18]. The phase distribution network tends to occupy significant chip area, and can be subtantially lossy. This increases the current requirements on the oscillator buffers to maintain the desired LO amplitude. Furthermore, it is critical that the distribution network be perfectly symmetric so that symmetry of the phases is not disturbed. Design considerations for the phase distribution network may be found in [21].

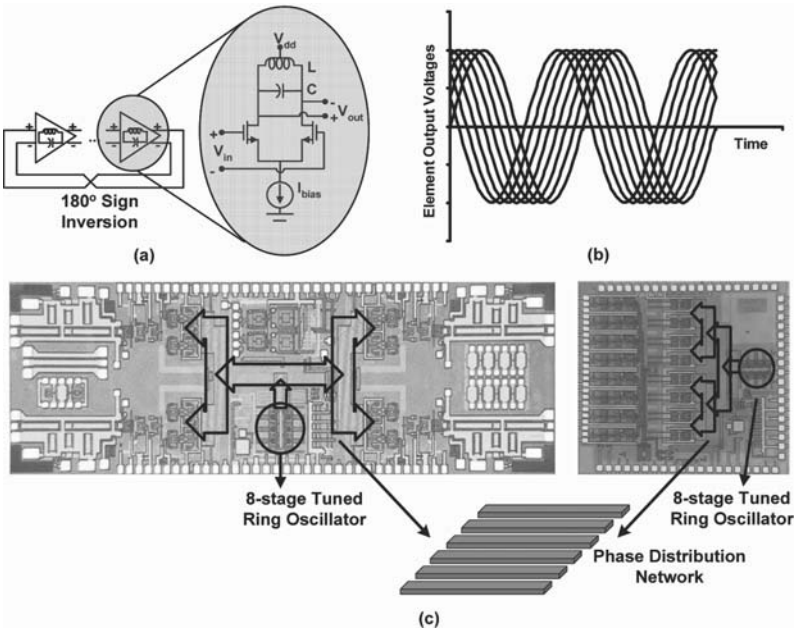

Fig. 7.18 (a) The tuned ring oscillator (b) Element voltages in an 8-element tuned ring oscillator (c) Chip microphotographs of a 4-element 24GHz phased array transmitter in a 0.18μm CMOS process ([19]) (©IEEE 2005) and an 8-element 24GHz phased array receiver in a 0.18μm SiGe process ([18]) (©IEEE 2004). Both employ an 8-element tuned ring oscillator in an LO phase-shifting architecture.

7.4.2.2 Coupled Oscillator Arrays

Another means of generating phase-shifted LO signals involves the coupling of multiple free-running oscillators together to form a *coupled oscillator array* (COA). The dynamics of COAs have been extensively studied in the past ([22], [23]), but the implementations have traditionally employed discrete, compound-semiconductor transistors. The usage of COAs for integrated, silicon-based phased arrays involves several design challenges and nuances.

The principle of operation of COAs is based on the concept of injection-locking, which was first dealt with in the electrical domain by Robert Adler [24]. When an electrical oscillator is injected with an external signal whose frequency is close to the free-running frequency of the oscillator, the oscillator becomes synchronized in frequency to the external signal. Fig. 7.19 depicts a traditional nMOS, cross-coupled, LC oscillator with an external signal injected into the LC tank in the current domain. If the free-running frequency of the LC oscillator is $\omega_0 = \frac{1}{\sqrt{LC}}$, and the frequency of the external signal is ω_{inj}, then the oscillator locks to ω_{inj} if the offset frequency $\Delta\omega_{inj} = |\omega_{inj} - \omega_0|$ lies within a locking range $\Delta\omega_{lock}$ given by

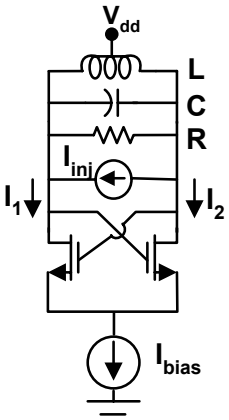

Fig. 7.19 Cross-coupled nMOS LC oscillator with an external signal injected into the LC tank in the current domain.

$$\Delta\omega_{lock} = \frac{\omega_0 \epsilon}{2Q}, \tag{7.11}$$

where Q, the Quality Factor of the LC tank, is given by $\frac{R}{\omega_0 L}$. ϵ is called the injection gain and is defined as the ratio of the amplitude of the injected current to the amplitude of the fundamental component of the oscillator's differential current $\frac{I_1 - I_2}{2}$. A larger injected current leads to a larger locking range. It should be noted, however, that this result assumes *weak* injection ($\epsilon << 1$). The phase difference $\Delta\phi$ between the locked oscillator and the injected signal is given by

$$\Delta\phi = \sin^{-1}\left(\frac{\omega_{inj} - \omega_0}{\Delta\omega_{lock}}\right). \tag{7.12}$$

When injection occurs at the free-running oscillation frequency, there is no phase difference. When injection is performed at the locking range boundaries, a 90^o phase difference is seen.

The concept of injection locking can be extended to a linear array of coupled oscillators with nearest-neighbour coupling, as depicted in Fig. 7.20(a). N free-running oscillators are arranged in a linear array and each oscillator is injected with the outputs of its nearest neighbours. In the circuit diagram of Fig. 7.20(a), the individual oscillators are implemented as LC oscillators with cross-coupled, nMOS negative-g_m cells and the outputs of the nearest neighbours are injected in the current domain using differential pairs. If all oscillators are identical with a center-frequency of ω_0 and an LC tank quality factor of Q, and the edge elements are detuned in frequency by $\Delta\omega$ as shown in Fig. 7.20(a), then the oscillator outputs become synchronized to a common oscillation frequency of ω_0 and exhibit a linear phase progression. The

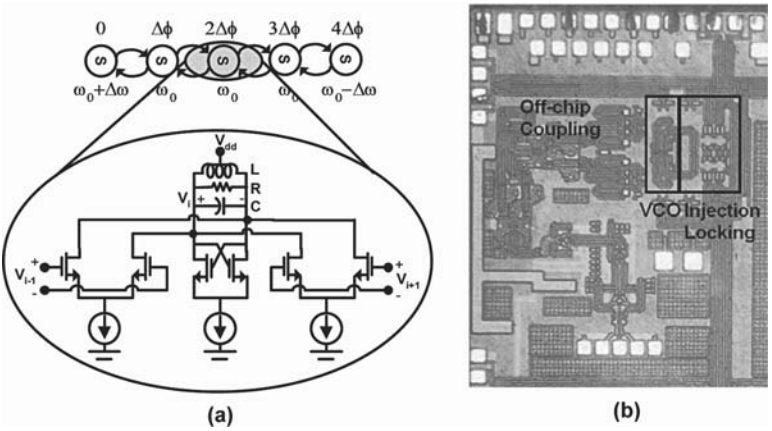

Fig. 7.20 (a) A linear array of coupled oscillators with nearest-neighbour coupling (b) Chip microphotograph of each transmitter element in the scalable, 60GHz phased array transmitter reported in [25] (©IEEE 2006). Injection locking is utilized only for the synchronization of multiple chips to a common reference. The phase shifts required for beam-steering are obtained from RF phase shifters.

successive phase difference $\Delta\phi$ is given by

$$\Delta\phi = \sin^{-1}\left(\frac{2Q\Delta\omega}{\omega_0\epsilon}\right), \tag{7.13}$$

where ϵ, called the coupling gain, is the ratio of the injected current amplitudes to the amplitude of fundamental current in the free-running oscillators. The presence of a *controllable*, linear phase progression at the outputs of the oscillators implies that each oscillator output needs to be routed to a single phased array channel for beam-steering. In other words, no phase distribution network is necessary. The mathematical formulation and basis for this linear phase progression may be found in [23]. It should be mentioned that, as was the case with injection locking, this behavior is predicated on the assumption of *weak* injection ($\epsilon << 1$).

The main challenge in the implementation of silicon-based, integrated phased arrays employing COAs is the sensitivity of COAs to element mismatches and process variations. If the center-frequencies of the oscillators deviate from the nominal value of ω_0 due to process variations and mismatches, the linear phase progression is disturbed. If the deviations are large, the oscillators may not even lock to each other. The case of a single oscillator locked to an external injected signal may be taken to illustrate the level of sensitivity. For a nominal center frequency of 60GHz, an injection gain of 0.1 and a Quality Factor of 15, which is typical for silicon processes at these frequencies, the injection locking range may be computed to be 200 MHz from (7.11). Therefore, a shift in the center frequency of the LC tank by 200

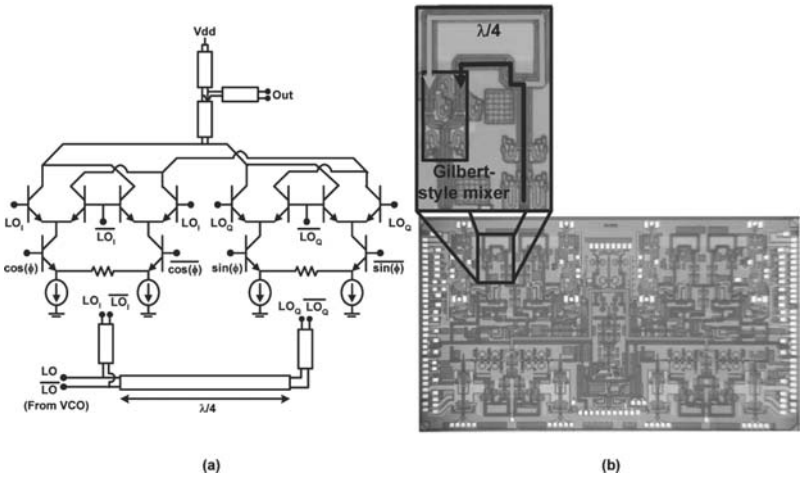

Fig. 7.21 (a) Circuit diagram of the local LO path Phase Interpolators used in [26] (b) Chip microphotograph of the 77GHz, 4-element phased array transceiver reported in [26] (©IEEE 2006).

MHz can prevent locking from occuring. Even if the center-frequency variations are largely below 200 MHz, the phase shift between the locked oscillator and injection reference would vary significantly. In [25], the authors report a scalable, 60GHz phased-array transmitter that employs injection locking only for the synchronization of multiple chips to a common reference. The phase shifts required for beam-steering are obtained from RF phase shifters. The chip microphotograph of this transmitter is depicted in Fig. 7.20(b). The design and use of calibration circuitry that can detect and correct on-chip variations is an interesting line of research that could render COAs a viable option.

7.4.2.3 LO Path Phase Interpolators

In [26], the authors report a 77GHz 4-element phased array transceiver employing an LO phase-shifting architecture, and the phase-shifting of the LO is accomplished through *local* phase interpolators. The circuit diagram of the local phase interpolators is shown in Fig. 7.21(a), and the chip microphotograph of the transceiver is depicted in Fig. 7.21(b). The quadrature LO signals are generated using a quarter-wavelength transmission line and the weights for the quadrature components are applied through doubly-balanced, Gilbert-type mixers. The weighted quadrature signals are then combined in current domain.

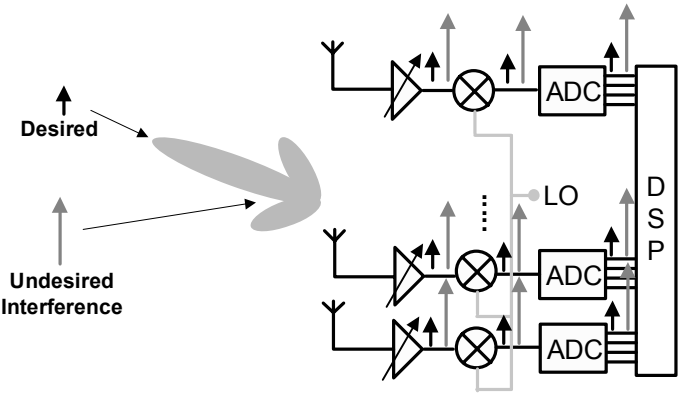

Fig. 7.22 The Digital Array Architecture

7.4.3 Digital Arrays

In the digital array architecture, which is depicted in Fig. 7.22, each phased-array channel is digitized using an Analog-to-Digital Converter (ADC) and the bits of all channels are then processed using a Digital Signal Processing unit (DSP), where the spatial filtering is performed. Therefore, strong intereferers get spatially cancelled only after digital signal processing, and hence the RF mixer and ADC of each channel and the DSP unit must have sufficient dynamic range to handle the interferers. Furthermore, virtually the entire RF chain is replicated for each channel. These two factors result in a rather power-hungry design.

The main advantage of the digital array is its versatility. A wide variety of complex, signal-processing algorithms can be implemented using DSP units. Such phased arrays are also called *smart antennas* and are extensively used in the cellular-phone industry. These algorithms allow the smart antenna to distinguish among desired signals, multipath and interfering signals, as well as to calculate their directions of arrival. In addition, smart antennas can adaptively update their beam patterns, so as to track the desired signal with the beam's main lobe and track the interefers with nulls. Multi-beam and multiple-input-multiple-output (MIMO) functionality, which will be discussed in greater detail later in this chapter, can also be incorporated into smart antennas. For a tutorial on smart antennas and common signal processing algorithms that they employ, the reader is directed to [27].

7.4.4 Comparative View of the Conventional Architectures

Table 7.2 presents a summary and comparison of the different phased array architectures detailed in this section. The true-time delay elements allow timed arrays to

Table 7.2 Comparison of conventional phased array architectures.

Arch.	Phase Shifter	Bandwidth/ Data-rate	Interference Cancellation	Area	Power
	Trombone Line	High (Time Delay)	Moderate	High	Moderate
	Varactor-loaded Trans. Line	High (Time Delay)	Good	High	Low
	Switched Trans. Line	Moderate (Phase shift)	Good	High	Low
RF Path	High-pass/low-pass	Moderate (Phase shift)	Good	High	Low
Y]	RTPS	Moderate (Phase shift)	Good	High	Low
	Phase Interpolator	Moderate (Phase shift)	Moderate	Moderate	Moderate
	Multiphase LC Oscillator	Moderate (Phase shift)	Moderate	Moderate	Moderate
LO Path	Coupled Oscillator Array	Moderate (Phase shift)	Moderate	Moderate	Moderate
	LO-path Phase Interpolation	Moderate (Phase shift)	Moderate	Moderate	Moderate
BB Path	Digital Arrays	High	Poor	High	High

function over wide signal bandwidths, which implies high data rates for wireless communication applications and fine range resolution in radar. Phase-shifter based architectures on the other hand can operate only over moderate bandwidths. The all-passive RF phase shifters and delay elements exhibit the greatest interference cancellation ability. The active RF phase shifters, delay elements and LO phase-shifting architectures demonstrate only moderate interference rejection. A larger amount of power would need to be consumed in the building blocks for these architectures to withstand strong interferers. Digital arrays are the poorest in this regard, and an extremely large amount of power would need to be spent in boosting the dynamic range of the mixers and ADCs of each channel.

In terms of area, the RF phase shifters and delay elements tend to be the most demanding. An exception is the RF phase interpolator, which can be somewhat compact. It should be noted that the path-sharing architecture may be employed to alleviate the area requirement of an RF phase-shifting architecture. The LO phase-shifting architectures have moderate area requirements - the phase shifters in the LO path can often be implemented in a small area as their linearity and noise figure performances are not critical. However, the architecture does require a mixer for each channel, which increases the area requirement somewhat. The digital array architecture requires a large area despite the lack of phase shifters due to the need for a mixer and an ADC in each channel.

In terms of power consumption, the RF phase-shifting architectures are the most efficient, particularly when the phase shifters/delay elements are passive. This is

because the architecture only requires one mixer. However, it should be noted that if the phase shifter/delay element loss is high, RF amplification stages may be required which may increase the power consumption. The LO phase-shifting architectures have moderate power consumption requirements primarily because of the need for a mixer in each signal path. The power consumption of the mixers is often not negligible as they need to withstand strong, in-band interferers. The buffers needed to distribute the LO to the different channels also contribute to the power consumption. The digital Array architecture is the most power hungry of the three due to the need for high-dynamic-range mixers and ADCs in each channel.

7.5 The VPRO-PLL Phased Array Architecture

A more recently developed phased array architecture is the Variable-Phase Ring Oscillator (VPRO) and Phase-Locked Loop (PLL) architecture proposed by the authors of this chapter. The architecture was first introduced in [28] and is unlike the conventional architectures delineated in the previous section. The architecture eliminates key building blocks such as mixers, phase shifters and power splitters/combiners, allowing for compact and low-power implementations. This section gives a broad description of the principle of operation of the architecture[6].

7.5.1 VPRO Concept

At the core of the architecture lies the Variable-Phase Ring Oscillator or VPRO. The VPRO (Fig. 7.23(a)) consists of a number of elements connected in a ring configuration, with each element comprising a nonlinear gain block driving a tuned load. Fig. 7.23(b) shows a MOS implementation of each element, where the gain block is realized through a differential pair. The VPRO is similar to the conventional tuned ring oscillator discussed earlier in this chapter save for the fact that an electrically tunable phase-shifter is introduced in the ring. The phase boundary condition dictates that the total phase shift in the ring must be an integral multiple of 2π. Therefore, the phase shift across each element (from V_{i-1} to V_i) is given by $\Delta\phi = \frac{2k\pi - \Phi_{ext}}{N}$, $k \in Z$. Hence, an electrically tunable linear phase progression is established, which is the requirement for beam-steering. It must be noted that to sustain this phase shift across each element, the oscillator functions at a frequency that is off the LC center frequency. This depicted qualitatively in Fig. 7.23(c), which shows the oscillation frequencies for different inter-element phase shifts and an LC center frequency of 24GHz.

[6] Portions of this text are taken from [30], ((c) IEEE 2008).

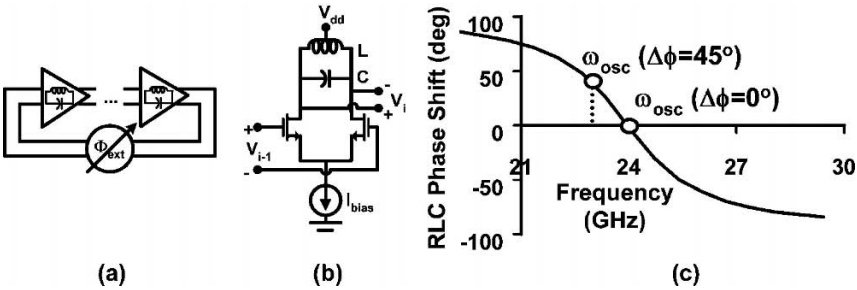

Fig. 7.23 (a) Block diagram of the Variable Phase Ring Oscillator (VPRO) (b) MOSFET-based differential pair implementation of a VPRO element (c) Dependence of VPRO oscillation frequency (ω_{osc}) on the inter-element phase shift ($\Delta\phi$).

7.5.2 Transmit Mode

The presence of a linear phase progression across the elements of the VPRO implies that, in the transmit mode, the output of each element can simply be connected to an antenna to accomplish beam-steering. No phase-distribution network is required. Fig. 7.24 shows the block diagram of the VPRO-PLL architecture in TX mode, with each element's output connected to a power amplifier and antenna.

As was mentioned before, when the external phase-shifter's setting is changed to steer the beam, the oscillation frequency of the VPRO changes as the phase shift across each tuned load changes. The incorporation of a PLL around the VPRO, shown in Fig. 7.24 with frequency dividers, phase-frequency detector (PFD), charge pump (CP) and a loop filter, ensures that the operating frequency remains constant while maintaining the desired phase progression.

The modulation of information onto the carrier may also be accomplished through the PLL. A signal injected in the current domain (I_{in}) into the loop filter in parallel with the charge pump's output current gets phase modulated (PM) onto the carrier as shown in Fig. 7.24. Fig. 7.24 also depicts the small signal model of the PLL, with K_{vco}, N_{div}, K_{PD} and $F(s)$ representing the VPRO tuning gain, frequency division ratio, PFD-CP gain and loop filter transfer function respectively. θ_{in} and I_{in} are the reference phase and injected modulation current respectively. The VPRO phase θ_{vpro} may be computed to be

$$\theta_{vpro}(s) = \frac{K_{PD}K_{vco}N_{div}F(s)}{sN_{div} + K_{PD}K_{vco}F(s)}\theta_{in}(s) + \frac{K_{vco}N_{div}F(s)}{sN_{div} + K_{PD}K_{vco}F(s)}I_{in}(s). \tag{7.14}$$

From the expression above, it is clear that the injected current gets directly translated to the phase of the VPRO through a transfer function. The bandwidth of the VPRO-PLL architecture in transmit-mode is limited by this transfer function.

This PLL-phase modulation approach is similar to the *translational loop* used extensively in polar transmitters for the GSM standard. The nonlinearity of the oscillator's K_{vco} profile can cause variations in the modulation gain and bandwidth

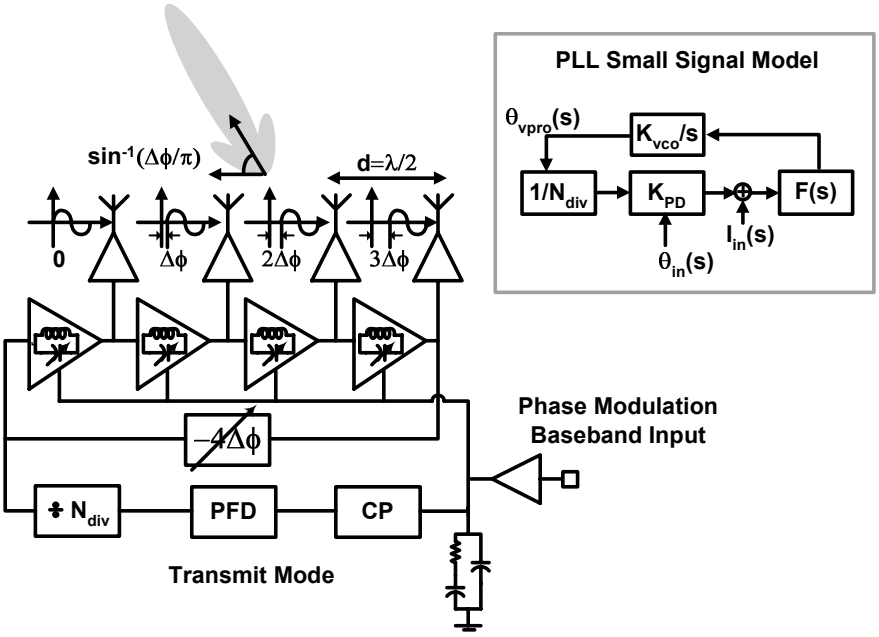

Fig. 7.24 Principle of operation of the VPRO-PLL architecture in transmit (TX) mode.

and self-calibration techniques have been developed for GSM polar transmitters to tackle this problem. Such techniques may be applied to the VPRO-PLL architecture as well. Support for amplitude modulation schemes, such as QAM, can also be introduced in a manner similar to GSM polar transmitters through the incorporation of RF, variable-gain ampifiers in each channel after the VPRO to provide envelope information to the signal.

7.5.3 Receive Mode

The block diagram of the VPRO-PLL architecture in receive mode is depicted in Fig. 7.25(a). The signals received by the antennas are amplified by LNAs and then are injected into each element of the VPRO in the current domain. The VPRO and PLL phase-shift and power-combine the received signals to accomplish phased-array spatial selectivity and down-convert the combined signal at the control voltage, thus fulfilling all the requirements of a phased-array receiver without employing explicit phase shifters, power combiners or mixers.

Consider an N-element generalization of the VPRO depicted in Fig. 7.25(a), with currents injected in shunt into every LC tank (Fig. 7.25(b)). The injected signals are assumed to be sinusoids with frequency ω_{inj} (close to the free-running frequency of the VPRO ω_{osc}) and a constant phase progression $\Delta\theta$ so that $I_{inj,i} = I_{inj}\cos(\omega_{inj}t +$

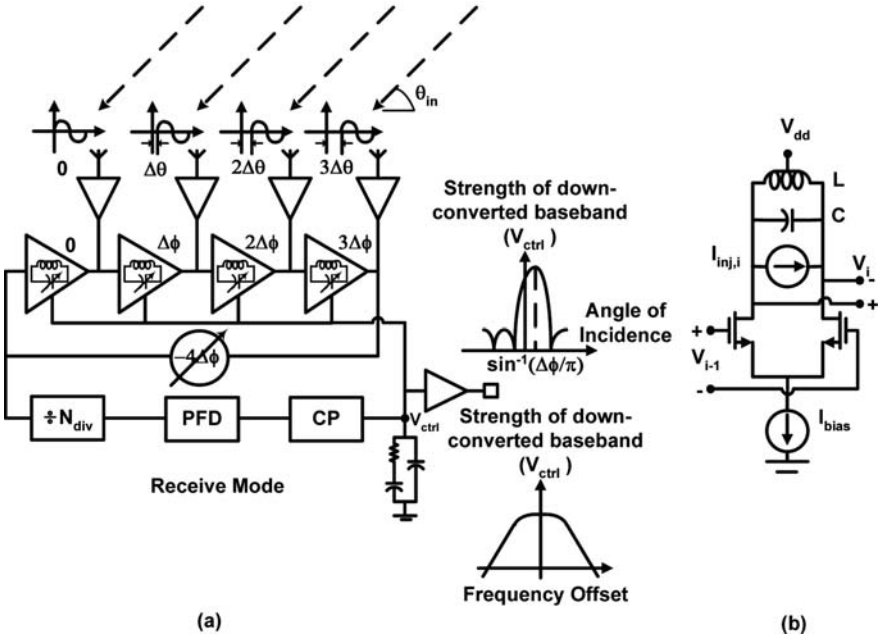

Fig. 7.25 (a) Principle of operation of the VPRO-PLL architecture in receive (RX) mode (b) Currents being injected into the LC tank of each element of the VPRO.

$(i-1)\Delta\theta$). As was noted in Section 7.2, $\Delta\theta$ is related to the angle of incidence θ_{in} (shown in Fig. 7.25(a)) as $\Delta\theta = \pi \sin\theta_{in}$. Like all eletrical oscillators, as was discussed in the injection-locking section earlier, the VPRO may lock to the frequency of the injected signals if that frequency lies within a *locking range*. In the case of the VPRO, the locking range may be determined to be

$$\Delta\omega_{lock} = \left(\frac{\omega_{osc}\epsilon(1+\tan^2\Delta\phi)}{2Q_{inj}+\tan\Delta\phi}\right)\left(\frac{\sin\frac{N}{2}(\Delta\theta-\Delta\phi)}{N\sin\frac{\Delta\theta-\Delta\phi}{2}}\right). \tag{7.15}$$

$Q_{inj} = \frac{R}{\omega_{inj}L}$ is the Quality Factor of the tuned loads at the injection frequency and $\epsilon = \frac{I_{inj}}{I}$ is the injection gain and is equal to the ratio of the injection amplitude (I_{inj}) to the amplitude of the fundamental current of each VPRO element (I). The second term in the expression for locking range ($\frac{\sin\frac{N}{2}(\Delta\theta-\Delta\phi)}{N\sin\frac{\Delta\theta-\Delta\phi}{2}}$) is identical to the array factor of a phased array of N elements, where $\Delta\phi$ is the progressive phase-shift introduced in the transmitter/receiver and $\Delta\theta$ is the progressive phase-shift suffered by the transmitted/received beam due to the path difference in air in the direction of interest. Hence, the VPRO exhibits intrinsic beam-forming tendencies which are

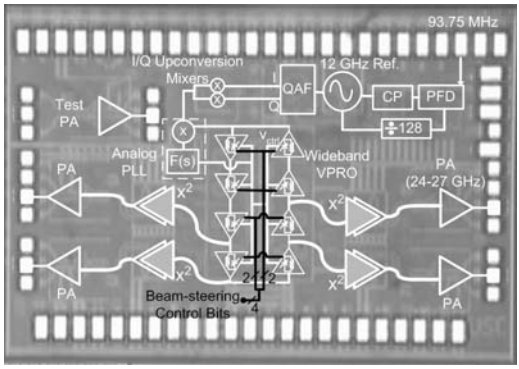

Fig. 7.26 Chip microphotograph of 24-27GHz, 4-channel, 0.13μm CMOS, UWB VPRO-PLL phased array transmitter [29] (©IEEE 2007).

manifested in its locking range. The constant multiplicative factor reduces to Adler's locking range result when all elements are in phase ($\Delta\phi = 0$).

When a VPRO stabilized by a PLL is subjected to external injection, the response is even more interesting. An oscillation is seen in the control voltage at the frequency difference between the injection frequency and the lock frequency of the PLL. In other words, the VPRO-PLL receiver downconverts the injected signals at the control voltage. This oscillation is a direct result of the fact that the injected signals attempt to pull the VPRO away from the PLL lock frequency and the PLL counteracts and attempts to restore it. The amplitude of the V_{ctrl} oscillation can be derived to be

$$\frac{|V_{ctrl}|}{I_{inj}} = \frac{\omega_{PLL}(1+\tan^2\Delta\phi)}{I(2Q_{inj}+\tan\Delta\phi)} \times \frac{\sin\frac{N}{2}(\Delta\theta-\Delta\phi)}{N\sin\frac{\Delta\theta-\Delta\phi}{2}} \times \left|\frac{K_{pd}F(j\Delta\omega_{inj})}{j\Delta\omega_{inj}N_{div}+K_{pd}K_{vco}F(j\Delta\omega_{inj})}\right|, \tag{7.16}$$

where ω_{PLL} is the lock frequency of the PLL and hence the operating frequency of the system. As mentioned before, I_{inj} is the amplitude of the current injected into each VPRO element and I is the amplitude of the fundamental current of each VPRO element. $\Delta\omega_{inj} = \omega_{inj} - \omega_{PLL}$ is the frequency difference between the injection frequency and the lock frequency of the PLL. N_{div}, K_{vco}, K_{pd} and $F(s)$ are the division ratio, VPRO tuning gain, phase-frequency detector gain and loop filter response respectively. From (7.16), the amplitude of the oscillation at V_{ctrl} shows phased-array spatial selectivity. Hence, full phased-array receiver functionality (downconversion with spatial power combining) is achieved by using V_{ctrl} as the output node. The received signal at V_{ctrl} is also directly proportional to the injected signal strength I_{inj}. This implies that the VPRO-PLL receiver has linear, small-signal gain, which is essential for amplitude-modulation schemes such as QAM.

From (7.16), the down-converted and spatially-combined signal at the control voltage has a frequency response that is governed by the PLL design parameters, such as N_{div}, K_{pd}, K_{vco} and $F(s)$. In general, the frequency response is low-pass for traditional loop-filters.

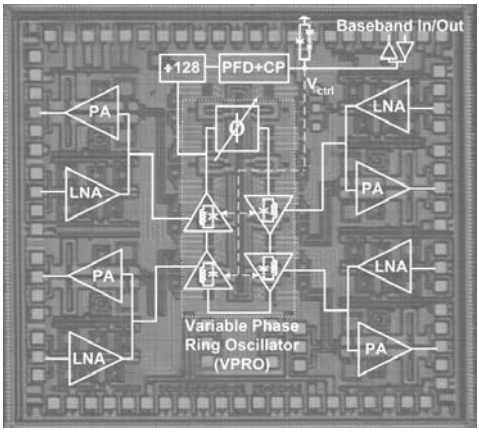

Fig. 7.27 Chip microphotograph of 24GHz, 4-channel, 0.13μm CMOS, VPRO-PLL phased array transceiver [28] (©IEEE 2007).

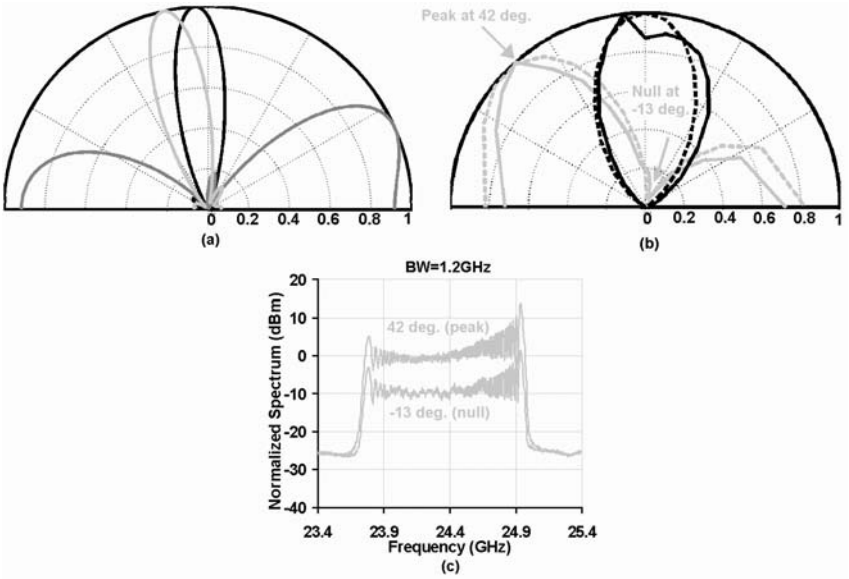

Fig. 7.28 (a) Measured 4-element, narrowband array patterns for the 4-channel, 24-27GHz, UWB phased array transmitter for selected array settings in polar coordinates (b) Measured 2-element, narrowband array patterns. The dashed lines represent the theoretical patterns (©IEEE 2007) (c) Combined UWB spectrum along the peak and null angles of transmission of a selected array setting when two elements are active (©IEEE 2007). The array setting is the same as the one used for the grey curve in the narrowband 2-element patterns.

Fig. 7.27 shows the chip microphotograph of the 24GHz, 4-channel, 0.13μm CMOS, VPRO-PLL phased array transceiver reported by the authors of this chapter in [28]. The VPRO is locked to a low-frequency reference in a divide-by-128 PLL. Due to the high division ratio, the frequency selectivity of the transmit and receive transfer functions is high, which makes the transceiver appropriate for narrowband operation. In [29], the authors report a 4-channel, 24-27GHz, UWB phased-array transmitter in 0.13μm CMOS based on the VPRO-PLL architecture (Fig. 7.26)[7]. In this UWB implementation, the VPRO is locked to an on-chip reference in a high-speed, dividerless, analog PLL which allows the architecture to support wideband phase and frequency modulation. The measured, *narrowband* array patterns of the UWB phased array transmitter are shown in Figs. 7.28(a) and 7.28(b) when four and two channels are active respectively. As is expected from (7.5), the beamwidth is reduced when four elements are active. It should be noted that these patterns are measured through on-wafer probing to eliminate the effects of packaging mismatches. Fig. 7.28(c) shows the combined spectrum along two different angles of transmission for two active channels when the transmitter emits a UWB signal with 1.2GHz of bandwidth. The two angles considered correspond to the expected peak and null locations for the selected array setting, which is the same setting as the one used for the light grey curve in Fig. 7.28(b). The combined spectrum is seen to be suppressed by atleast 10 dB in the null direction when compared to the peak. This verifies the UWB spatial selectivity of the array. For additional details on the VPRO-PLL architecture, including design guidelines and more measured results from the prototypes, the reader is directed to [30] and [31].

7.6 The Effect of Mismatch in Phased Arrays

The performance in the presence of channel mismatches is a critical parameter of any phased array. These variations result in amplitude and phase mismatches in the radiated/received signals and hence adversely affect the beam pattern [32],[33]. As an example, Fig. 7.29 shows the simulated array factor of a 4-element array in the presence of the deterministic amplitude and phase errors mentioned in the figure. The nominal beam-pointing direction is normal to the array, and the errors cause a deviation from this direction. The array also shows reduced peak gain and one of the sidelobe levels is higher. For reference, 15° of phase variation corresponds to approximately 100μm of length at 60GHz, assuming an effective dielectric constant of 4.

In this section, the effect of phase mismatches between the channels of a conventional RF phase shifting array is analyzed. Simple equations are presented in this chapter to quantify the effect of mismatches on various facets of array performance, including beam-pointing angle and sidelobe rejection ratio (SLRR). These mismatches arise from two possible sources. The first source is the intra-chip variation

[7] For 3GHz bandwidth and four array channels around a center frequency of 25.5GHz, a timed array implementation is not required.

that is inherent to any process technology. The second source, which is particularly pronounced at millimeter-wave frequencies, arises from packaging mismatches in the interface between the integrated phased array and the off-chip antennas.

7.6.1 Beam-pointing Error

For phased arrays that employ the delay-phase approximation and utilize half-wavelength-spaced antennas, the array factor of (7.3) can be rewritten as

$$AF(\Delta\phi, \theta_{in}) = \left(\frac{\sin \frac{N(\Delta\phi - \pi \sin\theta_{in})}{2}}{\sin \frac{\Delta\phi - \pi \sin\theta_{in}}{2}} \right)^2, \tag{7.17}$$

where $\Delta\phi$ is the phase progression introduced in the array. The beam-pointing angle can then be written as $\theta_m = \sin^{-1} \frac{\Delta\phi}{\pi}$.

In [32] and [33], the effect of channel mismatches on the beam-pointing angle of a conventional RF phase-shifting array is analyzed. The authors demonstrate that to first order, amplitude mismatches between phased array channels do not affect the beam-pointing angle, and only phase deviations need to be considered. The effect of phase errors on the beam-pointing angle can be summarized as

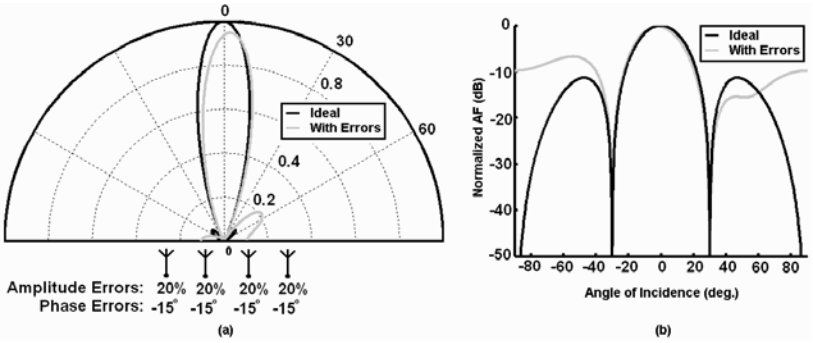

Fig. 7.29 (a) Sample 4-element array factor (normalized to the ideal peak array gain of 16) in the presence of amplitude and phase errors in polar coordinates (b) The same array factor plotted in the dB scale in Cartesian coordinates.

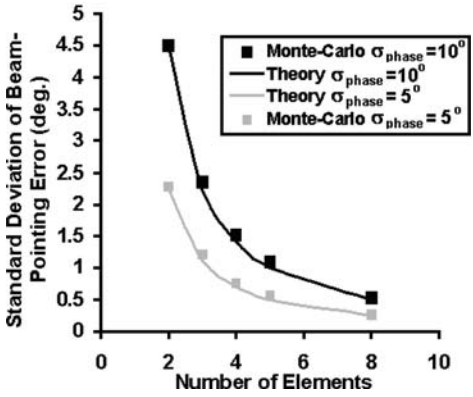

Fig. 7.30 Standard deviation of the beam-pointing error as obtained from (7.19) and 300-iteration Monte-Carlo simulations of a conventional RF-phase-shifting array with σ_{phase}=5° and 10°. The nominal phase shift of each channel is 0°, resulting in a nominal pointing angle that is normal to the array.

$$\Delta\theta_m \approx \frac{-\sum_{m=1}^{N}\sum_{n=1}^{N}(\delta_m - \delta_n)(m-n)}{\pi\cos\theta_m \frac{(N-1)N^2(N+1)}{6}}, \tag{7.18}$$

where $\Delta\theta_m$ is the beam-pointing error, θ_m is the beam-pointing angle in the absence of errors and δ_m is the phase error in the m^{th} phased array channel. This formula is derived for antennas that are half-wavelength apart, and considers only the linear terms of a Taylor Series expansion. For additional details on the formulation and derivation, the reader is directed to [33].

If each channel sustains phase errors that are small, independent and identically distributed with a distribution of $N(0,\sigma^2_{phase})$, the variance of the beam-pointing error can be computed from (7.18) to be

$$\sigma^2_{beam} = \frac{12\sigma^2_{phase}}{\pi^2\cos\theta^2_m(N-1)N(N+1)}. \tag{7.19}$$

Fig. 7.30 depicts σ_{beam} as obtained from (7.19) and 300-iteration Monte-Carlo simulations of a conventional RF phase-shifting array with σ_{phase}=5° and 10°. The nominal phase shift of each channel is 0°, resulting in a nominal pointing angle that

is normal to the array. It is interesting to note that from (7.19) and Fig. 7.30, the variance of the beam-pointing error is seen to fall at the rate of $\frac{1}{N^3}$ as N is increased.

7.6.2 Sidelobe Rejection Ratio

Sidelobes are a feature of all phased arrays. In the absence of errors, the locations of the main lobe, sidelobes and nulls in the array factor can be determined by differentiating (7.17) with respect to θ_{in} and setting the derivative equal to zero. The locations of the main lobe and the sidelobes are the solutions to

$$\tan\frac{N(\Delta\phi-\pi\sin\theta_{in})}{2}=N\tan\frac{\Delta\phi-\pi\sin\theta_{in}}{2}. \tag{7.20}$$

The trivial solution of $\Delta\phi=\pi\sin\theta_{in}$ corresponds to the main lobe. Solving this transcendental equation for the first or any other sidelobe is difficult. However, it is found that

$$\pi\sin\theta_{\rm lobe}\approx\Delta\phi\pm\phi_{N,lobe},\text{ where }\phi_{N,lobe}=\frac{2.929\pi}{N} \tag{7.21}$$

proves to be an excellent approximation for the location of the first sidelobes on either side of the main lobe. The sidelobe rejection ratio ($SLRR$), defined as the ratio of the power of the main lobe to the power of these first sidelobes, can now be computed as [8]

$$SLRR_0=\frac{N^2}{AF(\Delta\phi,\theta_{\rm lobe})}=\frac{N^2\sin^2(\frac{\phi_{N,lobe}}{2})}{\sin^2(\frac{N\phi_{N,lobe}}{2})}. \tag{7.22}$$

In order to determine the $SLRR$ in the presence of channel mismatches, the array factor in the presence of mismatches is written as

$$AF_{err}(\Delta\phi,\theta_{in},A_1..A_N,\delta_1..\delta_N)=\left|\sum_{i=1}^{N}(1+\frac{\Delta A_i}{A})e^{j((i-1)(\Delta\phi-\pi\sin\theta_{in})+\delta_i)}\right|^2, \tag{7.23}$$

where $\frac{\Delta A_i}{A}=\frac{A_i-A}{A}$ is the normalized amplitude error of each element, δ_i is the phase error of each element and $\Delta\phi$ is the array's phase progression. The deterioration in the $SLRR$ due to small amplitude and phase errors can be determined using a Taylor Series as

$$AF_{err}(\Delta\phi,\theta_{\rm lobe},A_1..A_N,\delta_1..\delta_N)=AF(\Delta\phi,\theta_{\rm lobe})+$$
$$\sum_{k=1}^{N}\frac{dAF_{err}}{d\delta k}_{|\text{all}\delta_i,\Delta A_i=0}\delta_k+\sum_{k=1}^{N}\frac{dAF_{err}}{d\Delta A_k}_{|\text{all}\delta_i,\Delta A_i=0}\Delta A_k. \tag{7.24}$$

[8] The subscript of 0 signifies that mismatches and process variations are absent.

The derivatives in the equation shown above may be computed from (7.23), and are found to be

$$\frac{dAF_{err}}{d\delta k}_{|\text{all}\delta_\text{i},\Delta\text{A}_\text{i}=0} = \frac{2\sin\frac{N\phi_{N,lobe}}{2}\sin\left((k-\frac{N+1}{2})\phi_{N,lobe}\right)}{\sin\frac{\phi_{N,lobe}}{2}}, \tag{7.25}$$

$$\frac{dAF_{err}}{d\Delta A_k}_{|\text{all}\delta_\text{i},\Delta\text{A}_\text{i}=0} = \frac{2\sin\frac{N\phi_{N,lobe}}{2}\cos\left((k-\frac{N+1}{2})\phi_{N,lobe}\right)}{A\sin\frac{\phi_{N,lobe}}{2}}. \tag{7.26}$$

If amplitude errors are absent and the channel phase errors are small, independent and identically distributed with a distribution of $N(0,\sigma^2_{phase})$, the variance of $AF_{err}(\Delta\phi,\theta_{\text{lobe}})$ can be computed from (7.24) to be

$$\sigma^2_{AF_{err}(\Delta\phi,\theta_{\text{lobe}})} = 2\sigma^2_{phase}\frac{\sin^2\frac{N\phi_{N,lobe}}{2}}{\sin^2\frac{\phi_{N,lobe}}{2}}\left(N-\frac{\sin N\phi_{N,lobe}}{\sin\phi_{N,lobe}}\right). \tag{7.27}$$

The standard deviation of the $SLRR$ ($\sigma^2_{SLRR}=\frac{N^2}{AF_{err}(\Delta\phi,\theta_{\text{lobe}})}$) can then be computed to be

$$\sigma^2_{SLRR} = 2N^4\sigma^2_{phase}\frac{\sin^6\frac{\phi_{N,lobe}}{2}}{\sin^6\frac{N\phi_{N,lobe}}{2}}\left(N-\frac{\sin N\phi_{N,lobe}}{\sin\phi_{N,lobe}}\right). \tag{7.28}$$

Fig. 7.31(a) depicts σ_{SLRR} as obtained from (7.28) and 300-iteration Monte-Carlo simulations of a conventional RF phase-shifting array with σ_{phase}=2.5° and 5°. The nominal phase shift of each channel is 0°. For large array sizes, from (7.28), $\sigma_{SLRR}\approx\frac{138.6\sigma_{phase}}{\sqrt{N}}$ and hence reduces with an increase in array size. Fig. 7.31(b) presents another visualization, depicting the theoretical 1-σ confidence interval for the $SLRR$ in dB-scale.

7.6.3 Implications on Array Packaging

As was discussed earlier in this chapter, there are two fundamental reasons that motivate the use of phased arrays in commercial wireless applications and radar. The first includes the increase in the transmitted power and the improvement in SNR at the receiver, which alleviate link budget requirements. The second is the improved directionality of the wireless link, which minimizes spatial interference and multipath effects. For applications that wish to harness the former, the accuracy of the beam-pointing angle is of importance as an error in the direction of transmission/reception would deteriorate the link budget. On the other hand, in environments where spatial interference and multipath effects dominate, the sidelobe rejection ratio is a critical parameter. The analyses and simulations in this section indicate that channel mismatches have a greater impact on sidelobe rejection than beam-pointing angle for

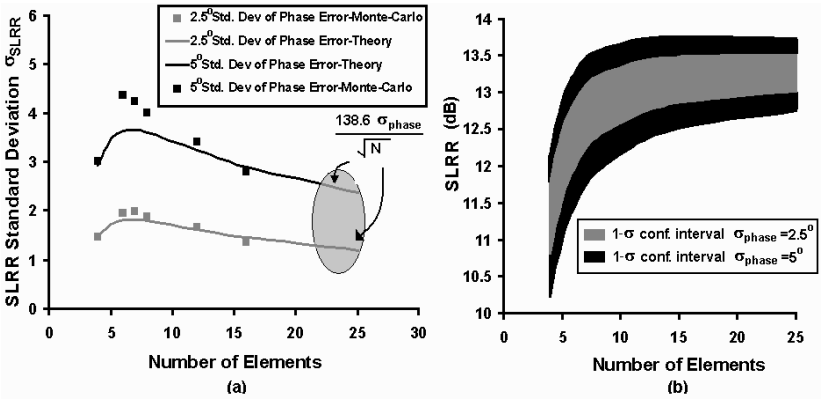

Fig. 7.31 (a) Standard deviation of the $SLRR$ in a conventional RF phase-shifting array as obtained from (7.28) and Monte-Carlo simulations. The nominal beam-pointing angle is normal to the array. (b) Theoretical 1-σ confidence interval for the SLRR.

typical array sizes and mismatch values. This implies that packaging is a greater concern for applications that are dominated by interference and multipath effects. Accurate, robust and repeatable packaging techniques, especially for multiple antenna systems, have yet to be developed at millimeter-wave frequencies. Techniques such as flip-chip antenna bonding [34] and on-chip antennas [35] show promise in combating this problem.

7.6.4 Array Calibration

The mismatch between multiple channels, induced by process, packaging, or connection to the antennas, as well as channel-to-channel signal coupling deteriorates the antenna array performance and is often calibrated in high performance military-type phased arrays. Process mismatches aside, a phase error of ±15° at millimeter-wave frequencies corresponds to a few tens of microns length variation of a wirebond, printed circuit board traces, chip-antenna connections, or antennas themselves if implemented off-chip. Variations of this order, even if calibrated at the time of manufacturing, might occur during the lifetime of the system. In order to realize robust silicon-based single-chip antenna arrays for commercial communication and sensing applications, on-chip testing and calibration techniques may be developed that measure the deterioration of array performance and appropriately correct the amplitudes and phases. In a communication system, measurement of array performance can be done at the system level where the gains and phases are adjusted to maximize the SNR. In a sensing array such as the automotive radar application, calibration through

sending a training sequence between the transmitter and receiver, e.g., smart antenna concepts, is not possible. Calibration techniques similar to [42],[43] that rely on the mutual coupling between the array antenna elements may be utilized, although the effect of on-chip coupling though the substrate must be considered as well.

7.7 Quantization Error in Phased Arrays

Practical phase shifters or delay elements have a finite number of settings and hence yield a discrete set of phases/delays. As a result, the steering angles achievable in practical phased arrays are also quantized. This section analyzes the implications of this quantization.

Fig. 7.32 depicts an N-element, RF phase-shifting, homodyne, phased array receiver with quadrature downconversion and half-wavelength-spaced antennas. The variable phase-shifters for each signal path are assumed to be controlled by n digital control bits, giving rise to 2^n phase-shift settings. For example a 3-bit phase-shifter can sustain shifts of -180^o, -135^o, 90^o ... 135^o, corresponding to a phase-shifting resolution of $\Delta\phi_{res}$=$\frac{360^o}{2^n} = 45^o$ and a beam-steering resolution of $\Delta\theta_{res} = \sin^{-1}\frac{\Delta\phi_{res}}{\pi} = \sin^{-1}\frac{1}{2^{n-1}} = 14.48^o$

An incoming QAM signal of the form $i(t)\sin(\omega t) + q(t)\cos(\omega t)$ is assumed, where $i(t)$ and $q(t)$ are the in-phase (I) and quadrature (Q) information signals. The I and Q LO signals are assumed to be $\sin(\omega t)$ and $\cos(\omega t)$ respectively, and the RF phase-shifter Φ_k is set to $(k-1)\Delta\phi$ (with $\Delta\phi$ set to the discrete phase difference closest to the incoming phase difference of $\pi\sin\theta_{in}$). The final combined signals in the I and Q channels can be determined to be

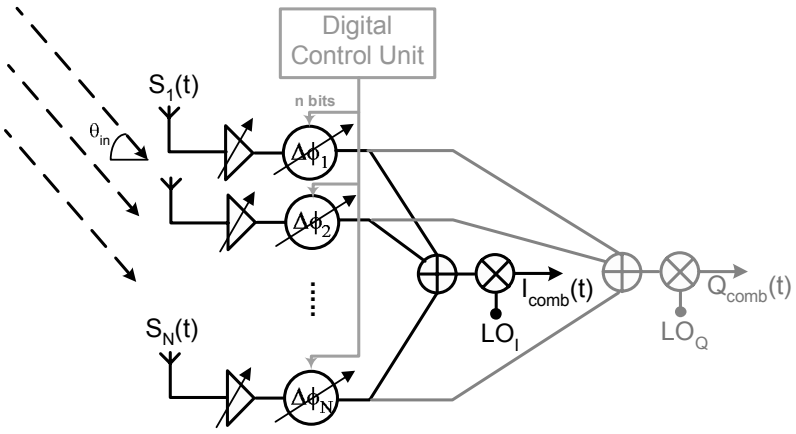

Fig. 7.32 N-element RF phase-shifting homodyne phased array receiver with quadrature downconversion.

$$I_{comb}(t) = \frac{i(t)}{2}\sqrt{AF(\Delta\phi, \theta_{in})}, \tag{7.29}$$

$$Q_{comb}(t) = \frac{q(t)}{2}\sqrt{AF(\Delta\phi, \theta_{in})}. \tag{7.30}$$

where AF is the array factor defined in (7.17). A number of assumptions are implicit in the above equations. The second harmonics produced by the mixers are assumed to be filtered out. Secondly, the bandwidth of the information signal is assumed to be small compared to the carrier frequency to eliminate the Array-induced ISI effect. Finally, if the discrete phase-shifter settings are not able to perfectly compensate for the delay in free space ($\Delta\phi \neq \pi \sin\theta_{in}$), the recovered constellation is rotated due to leakage of I into the Q channel and Q into the I channel. This systematic rotation is assumed to be undone in the receiver.

When the discrete phase-shifter settings are not able to perfectly compensate for the delay in free space, $AF(\Delta\phi, \theta_{in}) < N^2$, the peak array power gain, causing the receiver to show reduced gain and hence, reduced SNR. This is a direct result of the fact that the direction of arrival of the incoming signal and the beam-pointing angle are mismatched. The resultant SNR degradation can be quantified as

$$SNR = SNR_o \times \frac{AF(\Delta\phi, \theta_{in})}{N^2}, \tag{7.31}$$

where SNR_o is the SNR in the absence of the effect of discrete phases, and includes the input SNR, receiver front-end noise figure (NF) and the 10log(N) phased array improvement[9].

The SNR reduction can be related to a degradation in the Error Vector Magnitude (*EVM*) as

$$EVM = \frac{1}{\sqrt{SNR}} = \frac{1}{\sqrt{SNR_o}} \times \frac{N}{\sqrt{AF(\Delta\phi, \theta_{in})}}. \tag{7.32}$$

Fig. 7.33(a) shows the theoretical *EVM* degradation factor, *i.e.*, the $\frac{N}{\sqrt{AF}}$-term in (7.32), as a function of the angle of incidence for 4- and 8-element arrays, with 3- and 4-bit phase-shifting in each case. A Simulink simulation of an 8-element quadrature RF phase-shifting homodyne receiver with 3-bit phase-shifters receiving a 16-QAM input is also included. SNR_o is set to be 33.2dB (corresponding to, for instance, an input SNR of 30.2dB and a front-end NF of 6dB, along with the 10log(8) array SNR improvement), resulting in EVM_o=1.5%.

As can be seen in Fig. 7.33(a), the maximum degradation in *EVM* occurs when the progressive phase-shift of the incoming wave in space lies right between the phase-shifting resolution of the receiver. This maximum degradation can be computed to be

$$\left(\frac{EVM}{EVM_o}\right)_{max} = \frac{N \sin\frac{\Delta\phi_{res}}{4}}{\sin\frac{N\Delta\phi_{res}}{4}}. \tag{7.33}$$

[9] The 10log(N) SNR improvement assumes that each antenna picks up uncorrelated noise from the surroundings. It is also true when the receiver front-end NF dominates over the input noise, as the front-end noise would be uncorrelated between different signal paths.

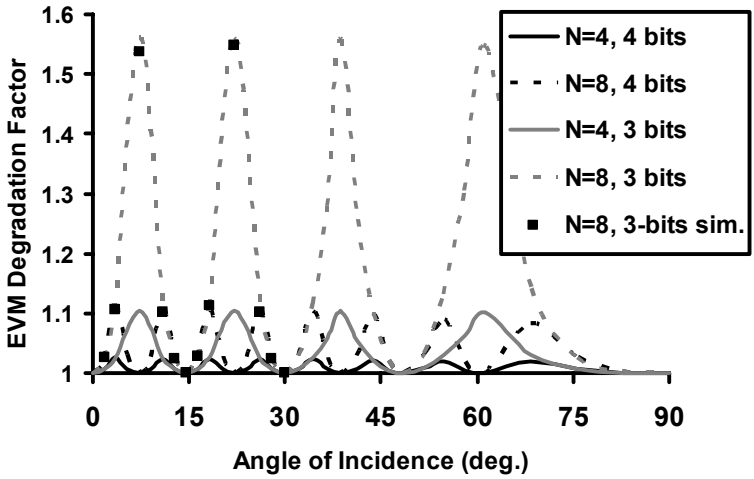

Fig. 7.33 *EVM* degradation due to discrete phases as a function of the incidence angle, phase-shifter bits and number of elements N. A Simulink simulation of a 16-QAM input incident on a 8-element quadrature RF phase-shifting homodyne receiver with $SNR_o = 33.2dB$ and 3-bit phase-shifters is also shown.

As N, the number of elements, is increased, for a fixed phase-shifting resolution, the maximum *EVM* degradation increases as the beam becomes narrower, resulting in a higher gain and SNR penalty when the incoming direction and the beam-pointing angle are mismatched. This effect is reflected in Fig. 7.33(a). Therefore, for a practical phased array, the choice of the number of phase-shifter bits is governed by N and the desired upper bound on *EVM* degradation, with a larger number of bits required for larger arrays.

7.8 Multi-Beam Antenna Arrays

Military radars have been the major application of antenna arrays. In these applications, it is highly desirable to locate and track multiple targets simultaneously. Mechanical steering of multiple directional antennas, each for one target, is not possible in many applications such as airborne radars. Antenna arrays with enough degrees of freedom in the amplitude and delay (phase) of each RF path can form and scan multiple simultaneous beams. A linear combination of narrowband RF signals with different phase shifts and amplitudes can form beams at the desired directions. Given a narrowband signal, the most general case is to incorporate independent amplitude and phase control in each RF path [10]. The phase shifted and amplified

[10] It should be reminded again that in a narrowband system, phase shifting the RF signal can be done in the local oscillator path as well.

(or attenuated) signals are not all combined, since multiple outputs corresponding to different beam angles are needed. Rather, these signals are all down converted to baseband independently. The baseband signals are then converted to a digital data stream and processed appropriately to provide the information coming from multiple spatial angles. This is often referred to as digital beam-forming. Access to all RF signals independently and processing them in the digital domain not only creates multiple simultaneous beams, but also is used in advanced Adaptive Space Time Array Processors to increase the signal-to-clutter ratio. When the array size is large, converting all the phase shifted and amplified RF signals to baseband independently requires much area (I/O signals) and power consumption not only in the analog to digital data conversion, but also in the digital signal processor (digital beam former). Independent access to all elements' amplitudes and phases is usually not required to achieve the desired number of independent beams. Therefore, it is common to divide a larger array to smaller sub-arrays, say with a size of 4x4 in a 2D array. Within a sub-array, each RF path has an independent phase and amplitude control; but, all signals are finally combined. In other words, only the combined signals within the sub-arrays are down-converted to baseband for further processing. The appropriate size of the sub-array depends on the system requirements such as the total number of desired beams, array size, and also the signal bandwidth.

Multiple beams can be formed in the RF domain as well. As discussed before, a linear delay (or phase) progression between different RF paths creates a beam at a particular angle. In a standard phased array, this delay (phase) progression is adjusted electronically. If multiple delays or phases are created simultaneously, multiple beams can be formed in the RF domain simultaneously. This is simply illustrated in Figure 7.34. An example of a modular multi-beam array based on this straight forward implementation is given in [36]. In order to form k independent beams in an n-element array, $k \times n$ phase shifters and variable gain amplifiers are needed.

The main advantage of multiple beam formation in the RF domain is that interference signals are cancelled at the front end prior to down-conversion and conversion to digital bits due to the spatial selectivity of the RF beam-former. This reduces the dynamic range and hence the power consumption of RF mixers and data converters. In principle, each output of a multi-beam RF beam-former can be connected to a separate transceiver allowing for processing of signals from all spatial segments simultaneously (spatial filter bank). However, in many applications, this capability is not required, especially, as it comes at the expense of chip area and power consumption of several transceivers. Oftentimes, only a few simultaneous beams are sufficient at any time to improve the system robustness and functionality. If not all the created angles in the RF beam-former are needed at a given time, fewer number of transceivers (up/down-converters, ADCs/DACs) can be turned on. Alternatively, an RF beam selector can choose the appropriate outputs of the multi-beam RF array processor and feed them to a few transceivers in this Switched-Beam Multi-Beam array. The disadvantage of an RF multi-beam approach, if implemented in the straight forward manner as shown in Figure 7.34, is the larger area of multiple RF variable true time delay elements (phase shifters) and power combiners. Figure 7.35 com-

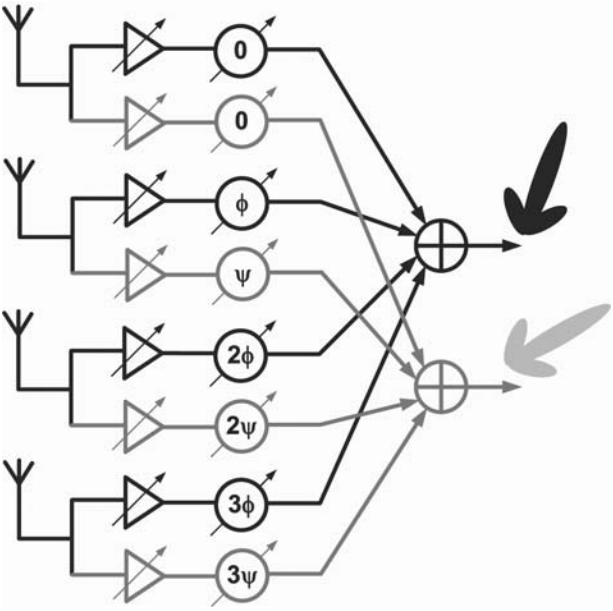

Fig. 7.34 A phased array that generates multiple beams through the usage of additional delay elements/phase shifters.

pares the RF Beam-Forming versus the Digital Beam-Forming architectures in a multi-beam array.

The fact that for a given incident angle, the time delay (phase shift) difference between adjacent elements is constant can be used to create multi-beam architectures with fewer number of area-hungry variable time delay elements. The most famous two have been proposed by Butler [37] (Fig. 7.37) and Blass [38] (Fig. 7.37) for narrowband and wideband arrays, respectively. Both of these solutions were developed assuming discrete component implementations and are not necessarily optimum for integration in a small chip size.

Recently, Chu has proposed an architecture where multiple beams are formed in the RF domain in a small area [39]. Chu's implementation relies on true time delay elements and hence can be used for both wideband and narrowband arrays (phased arrays and timed arrays). The basic principle behind the architecture is shown in Figure 7.38 where two antenna elements are connected to the two ends of a transmission line[11]. At any point along the transmission line, signals that are received by either of the antennas will face a delay proportional to the length of line from their corresponding antennas to the measured point. The delay difference between these signals dictates the incident angle. For instance, both received signals

[11] The effect of loading and reflections are ignored in the discussions for simplicity. These are taken care of in the actual implementation [39].

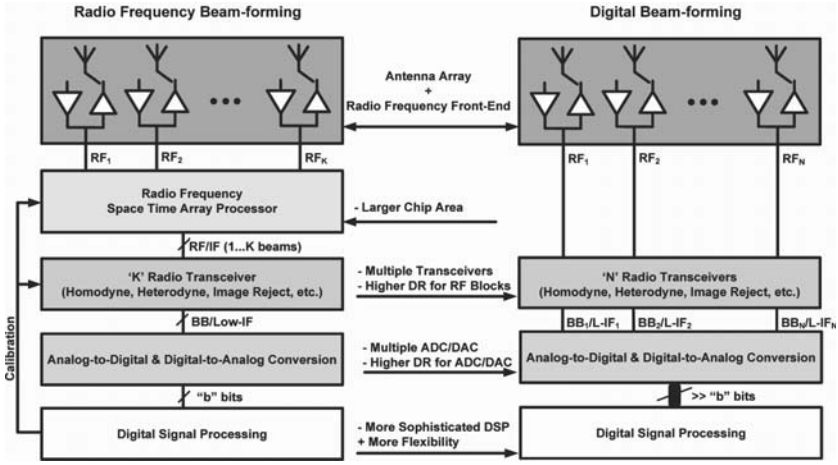

Fig. 7.35 A comparison of RF beamforming and Digital beamforming architectures for multi-beam arrays.

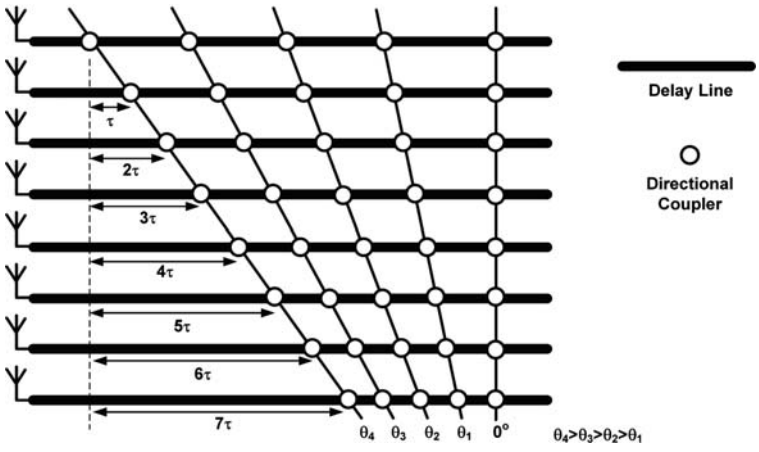

Fig. 7.36 The Blass matrix for wideband multi-beam arrays.

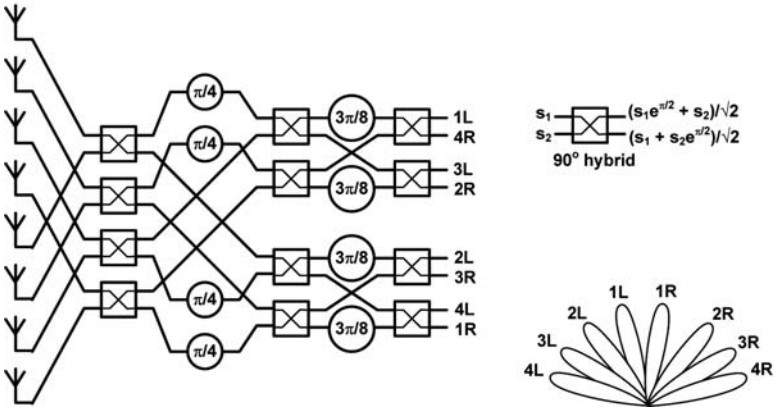

Fig. 7.37 The Butler matrix for narrowband multi-beam arrays.

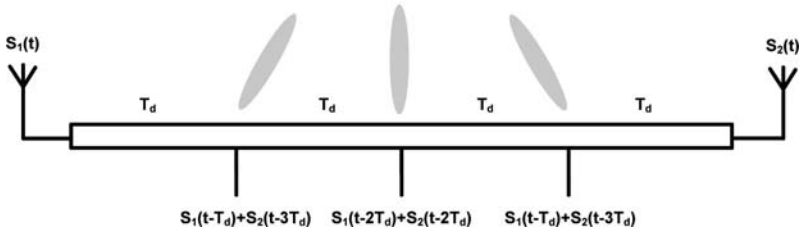

Fig. 7.38 Chu's architecture for RF multi-beam arrays.

reach the middle point with equal delay. Hence, the middle point corresponds to the beam that is normal to the plane of antennas. In this simplified example, it is clear that using a single delay line with several tap points, each corresponding to a different incident angle, leads to a much more compact realization compared with both Blass and Butler architectures. In [39], the authors report a 2D version of the array where 7×7 simultaneous beams are formed in an array with 2×2 elements. The architecture can be extended to $2N \times 2N$ antenna elements and $K \times K$ simultaneous beams.

It is also worth commenting on the possible advantages of a multi-beam array for wireless communication. Transmitting multiple data streams for different angles at the base station of a cellular system increases the communication capacity. At millimeter waves, creating multiple beams at the receiver has certain advantages as well. One of the major impediments in realizing millimeter wave wireless communica-

tions has been the poor link robustness due to the ease in obstructing the line of sight. Phased arrays can somewhat help by steering the beam away in an attempt to find an alternative communication path through reflections. Alternatively, a multi-beam array at the transmitter and receiver can be used to create several parallel communication channels, some perhaps through reflections, to improve the link robustness. The decision to design a multi-beam array versus a single-beam scanning array in millimeter waves mostly depends on the application and involves the usual tradeoff between reliability, performance, cost, and power consumption.

7.9 Antenna Arrays and Multiple Input Multiple Output (MIMO) Transceivers

Spatial diversity utilizing multiple spaced antennas is an attractive way to increase the signal-to-noise ratio and hence enhance the Shannon channel capacity. In a statistically fading environment, the received signal varies rapidly as the distance between the transmitter and receiver is altered by a fraction to a few wavelengths[12] [44]. Spatially separated antennas can be used to extract more information and effectively increase the higher data rate. If multiple receiving antennas are sufficiently spaced apart, their received signal levels are almost independent in a statistically fading channel. A decision circuit can simply pick the antenna with the highest received SNR (selection diversity) or more optimally it can combine the complex weighted received signals[13] from all the antennas to achieve the maximum possible SNR (maximal ratio combining). The receiver architecture for such diversity systems will be similar to those already discussed for beam-forming arrays; although, the algorithm to set the complex weights (amplitudes and phases) will be different. In the previously discussed beam forming schemes, the goal has been to create a line-of-sight between the transmitter and receiver in order to maximize the transmit power efficiency, increase the receive SNR, and spatially filter the interference signals. In diversity systems, the goal is to maximize the received SNR in a highly scattering environment with little or no line-of-sight between the transmitter and receiver.

Similarly, in a statistically fading environment, transmitted signals from spatially separated antennas experience independent channels as they reach the receiver. If channel properties from each transmitting antenna to the receiver are known, the transmitter can shape the signal that is fed into each antenna in such a way that the received signals add coherently. Even in the case where the communication channel is not known to the transmitter, by transmitting different signals from various antennas over time, a larger SNR at the receiver can be achieved in the so-called Space-Time Coding schemes [45]. As a more general case, we can imagine multiple-input multiple-output, MIMO, systems with 'M' transmitting antenna elements and 'N'

[12] The minimum required distance between the antennas that results in independent (uncorrelated) communication channels is a function of size, shape, and number of scattering objects and their distance to the antennas. This typically varies from a few tenths to a few wavelengths.

[13] Complex weight assumes narrowband signals.

receiving antenna elements. Assuming independent communication channels from each transmitting antenna to a receiving antenna, it can be shown that besides the achieved diversity gain, the capacity of a MIMO system increases with the number of antenna elements. Although some space time codes require only delay-and-sum processing or a linear combination of complex weighted signals at the receiver, but many advanced codes require other forms of processing on the received signals. In this case, each antenna must be accompanied by an independent transceiver and all the processing is done at baseband. Whether space-time coding is attractive for the wireless communication applications envisioned at millimeter waves or not is still unclear. In many scenarios, the distance between the transmitter and receiver is short and LOS can easily be created though beam-forming. Moreover, at millimeter waves, the overall SNR will be dominated by the receiver's NF and therefore a mere combining of signals from multiple parallel receivers will enhance the SNR in most cases. Given the fact that the most dominant rationale behind millimeter wave communication is the large user channel bandwidth ($>$ 1GHz), digital processing of multiple received signals does not appear to be power efficient. Therefore, the RF beam-forming architectures described in this chapter will likely be more suitable.

7.10 Concluding Remarks

Over the past few years, silicon based integrated millimeter wave systems have generated great research interest due to their advantages in offering high data rate in wireless communications and high resolution in radar and imaging systems at a lower cost. Various forms of multi-antenna systems provide a plethora of solutions for wireless communications, radar, and imaging systems. Millimeter waves offer more bandwidth for ultra high data rate wireless communications and better resolution for radar and imaging systems, while reducing the required size of integrated systems in a multi-antenna configuration. Integration of a complete multi-antenna system in silicon results in substantial improvements in cost, size, and reliability and provides numerous opportunities to perform on-chip signal processing and conditioning.

There have already been several successful university demonstrations of integrated phased array receivers, transmitters, and transceivers at 24GHz and 77GHz over a relatively short span of five years [18],[19],[26],[35],[28],[29]. In addition, an integrated beam-former at 60GHz has been reported [8]. This beam-former chip can be added to existing millimeter wave receiver or transmitter chipsets to provide spatial selectivity and improve sensitivity.

Silicon based integrated wideband timed array transceivers are more recent efforts [5],[6] where most of the focus has been on frequencies below 15GHz. Integrated broadband beam-formers at microwaves and millimeter waves have been reported. However, they provide a constant phase shift, and not a constant group delay, between adjacent elements and are not appropriate for signals with instantaneously wide bandwidth. An impulse-based ultra-wideband automotive radar array operating at

22GHz - 29GHz is one example where timed array transceivers may be needed instead of conventional phased arrays.

Packaging and antenna design, already key elements and research topics in a low cost realization of millimeter wave systems, are even more important in the context of transceiver arrays. There is an ongoing debate on the issue of off-chip versus on-chip antennas [35]. In the context of arrays, the advantages of on-chip antennas are lower chip-antenna interconnect loss, more robustness to variations, and ease of system integration. However, on-chip antennas are not efficient due to the loss of silicon substrate or the small distance between the metal layers in on-chip patch antennas when the silicon substrate is shielded. Plus, the cost of silicon area used for on-chip antennas is not negligible. Off-chip antenna arrays necessitate a low cost, robust, and preferably symmetric chip-antenna interconnect scheme. Low cost integration of the silicon chips with efficient antenna arrays is one of the areas that deserves more research. Low cost testing and calibration of integrated transceiver arrays for commercial applications are other important areas that need to be addressed.

Overall, with applications in a variety of sectors including commercial, space, military, healthcare, environmental, and pure scientific discoveries, millimeter wave and broadband silicon based multiple-antenna integrated systems constitute a rich area of research for some more years to come.

References

1. P. K. Bondyopadhyay, “The first application of array antenna", in *2000 IEEE International Conference on Phased Array Systems and Technology*, May 2000, pp. 29-32.
2. D. Parker and D. C. Zimmerman, “Phased arrays - part II:implementations, applications and future trends," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 688-698 , March 2002.
3. T. Yao, M. Gordon, K. Yau, M. T. Yang, S. P. Voinigescu, “60-GHz PA and LNA in 90-nm RF-CMOS," in *2006 IEEE RFIC Symposium Digest of Technical Papers*, June 2006.
4. E. Grass, F. Herzel, M. Piz, Y. Sun and R. Kraemer, “Implementation aspects of Gbit/s communication system for 60 GHz band," in *Proceedings of the 14th Wireless World Research Forum (WWRF 14)*, July 2005.
5. J. Roderick, H. Krishnaswamy, K. Newton and H. Hashemi, “Silicon-Based Ultra-Wideband Beam-Forming," *IEEE Journal of Solid State Circuits*, vol. 41, no. 8, pp. 1726-1739, Aug. 2006.
6. Ta-Shun Chu, J. Roderick, H. Hashemi, “A 4-Channel UWB Beam-Former in 0.13μm CMOS using a Path-Sharing True-Time-Delay Architecture," in *ISSCC Digest of Technical Papers*, vol. 50, Feb. 2007, pp. 426-613.
7. C. Cao, K. K. O, “Millimeter-wave voltage-controlled oscillators in 0.13μm CMOS technology," *IEEE Journal of Solid State Circuits*, vol. 41, no. 6, pp. 1297-1304, June 2006.
8. A. Natarajan, B. Floyd and A. Hajimiri, “A Bidirectional RF-Combining 60GHz Phased-Array Front-End," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, vol. 50, Feb. 2007, pp. 202-597.
9. Byung-Wook Min and Gabriel M. Rebeiz, “Ka-Band BiCMOS 4-Bit Phase Shifter with Integrated LNA for Phased Array T/R Modules," in *2007 IEEE/MTT-S International Microwave Symposium Digest*, pp. 479-482, June 2007.
10. M. Morton, J. P. Comeau, J. D. Cressler, M. Mitchell and J. Papapolymerou, “Sources of Phase Error and Design Considerations for Silicon-Based Monolithic High-Pass/Low-Pass Microwave Phase Shifters," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 12, pp. 4032-4040, Dec. 2006.
11. T. M. Hancock, G. M. Rebeiz, “A 12-GHz SiGe phase shifter with integrated LNA," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 3, part 1, pp. 977-983, March 2005.
12. C. T. Charles and D. J. Allstot, “A 2-GHz Integrated CMOS Reflective-type Phase Shifter with 675° Control Range," in *Proceedings of the 2006 IEEE International Symposium on Circuits and Systems*, May 2006, pp. 381-384.
13. H. Zarei and D. J. Allstot, “A low-loss phase shifter in 180 nm CMOS for multiple-antenna receivers," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb. 2004, pp. 392-534.
14. Kwang-Jin Koh and Gabriel M. Rebeiz, “An X- and Ku-Band 8-Element Linear Phased Array Receiver," in *Proceedings of the 2007 IEEE Custom Integrated Circuits Conference*, Sep. 2007, pp. 761-764.
15. M. Chua and K. Martin, “1 GHz Programmable Analog Phase Shifter for Adaptive Antennas,” in *Proceedings of the 1998 IEEE Custom Integrated Circuits Conference*, May 1998, pp. 11-14.
16. A. Afsahi, A. Behzad, S. Au, R. Roufoogaran and J. Rael, “An Area and Power Efficient Phase Shifter + Mixer Circuit Applied to WLAN System,"’ in *2007 IEEE Radio Frequency Integrated Circuits Symposium Digest of Technical Papers*, June 2007, pp. 357-360.
17. S. Alalusi and R. Brodersen, “A 60GHz Phased Array in CMOS," in *Proceedings of the 2006 IEEE Custom Integrated Circuits Conference*, Sep. 2006, pp. 393-396.
18. Xiang Guan, H. Hashemi and A. Hajimiri, “A fully integrated 24-GHz eight-element phased-array receiver in silicon," *IEEE Journal of Solid State Circuits*, vol. 39, no. 12, pp. 2311-2320, Dec. 2004.
19. A. Natarajan, A. Komijani and A. Hajimiri, “A fully integrated 24-GHz phased-array transmitter in CMOS," *IEEE Journal of Solid State Circuits*, vol. 40, no. 12, pp. 2502–2514, Dec. 2005.

20. H. Krishnaswamy and H. Hashemi, “A rigorous phase noise analysis of tuned ring oscillators," in *2007 IEEE Radio and Wireless Symposium Digest of Technical Papers*, Jan. 2007, pp. 43-46.
21. H. Hashemi, Xiang Guan, A. Komijani, A. Hajimiri, “A 24-GHz SiGe phased-array receiver - LO phase-shifting approach," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 2, pp. 614-626, Feb 2005.
22. K. D. Stephan, “Inter-injection locked oscillators for power combining and phased arrays," *IEEE Transactions on Microwave Theory and Techniques*, vol. MTT-34, pp. 1017-1025, Oct. 1986.
23. P. Liao, R. A. York, “A new phase-shifterless beam-scanning technique using arrays of coupled oscillators," *IEEE Transactions on Microwave Theory and Techniques*, vol. 41, no. 10, pp. 1810-1815, Oct. 1993.
24. R. Adler, “A study of locking phenomena in oscillators," *Proceedings of the IRE*, vol. 34, pp. 351-357, June 1946.
25. J.F. Buckwalter, A. Babakhani, A. Komijani and A. Hajimiri, “An integrated subharmonic coupled-oscillator scheme for a 60-GHz phased-array transmitter," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 12, part 2, pp. 4271-4280, Dec. 2006.
26. A. Natarajan, A. Komijani, X. Guan, A. Babakhani and A. Hajimiri, “A 77-GHz Phased-Array Transceiver With On-Chip Antennas in Silicon: Transmitter and Local LO-Path Phase Shifting," *IEEE Journal of Solid State Circuits*, vol. 41, no. 12, pp. 2807-2819, Dec. 2006.
27. M. Chryssomallis, “Smart antennas," *IEEE Antennas and Propagation Magazine*, vol. 42, no. 3, June 2000.
28. H. Krishnaswamy and H. Hashemi, “A Fully Integrated 24GHz 4-Channel Phased-Array Transceiver in 0.13μm CMOS Based on a Variable-Phase Ring Oscillator and PLL Architecture," in *ISSCC Digest of Technical Papers*, vol. 50, Feb. 2007, pp. 124-591.
29. H. Krishnaswamy and H. Hashemi, “A 4-Channel 24-27 GHz UWB Phased Array Transmitter in 0.13µm CMOS for Vehicular Radar," in *Proceedings of 2007 IEEE Custom Integrated Circuits Conference*, Sep. 2007, pp. 753-756.
30. H. Krishnaswamy and H. Hashemi, “A Variable-Phase Ring Oscillator and PLL Architecture for Integrated Phased Array Transceivers," submitted to the *IEEE Journal of Solid State Circuits*.
31. H. Krishnaswamy and H. Hashemi, “A 4-Channel 24-27 GHz UWB Phased Array Transmitter in 0.13µm CMOS," submitted to the *IEEE Journal of Solid State Circuits*.
32. K. R. Carver, W. K. Cooper and W. L. Stutzman, "Beam-pointing errors of planar-phased arrays," *IEEE Transactions on Antennas and Propagation*, vol. 21, no. 2, pp. 199-202, March 1973.
33. J. Shen and W. Pearson, "The phase error and beam-pointing error in coupled oscillator beam-steering arrays," *IEEE Transactions on Antennas and Propagation*, vol. 53, no. 1, pp. 386-393, Jan. 2005.
34. U. R. Pfeiffer, J. Grzyb, D. Liu, B. Gaucher, T. Beukema, B. A. Floyd, and S. K. Reynolds, "A chip-scale packaging technology for 60-GHz wireless chipsets," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 8, pp. 3387-3397, Aug. 2006.
35. A. Babakhani, X. Guan, A. Komijani, A. Natarajan and A. Hajimiri, "A 77-GHz Phased-Array Transceiver With On-Chip Antennas in Silicon: Receiver and Antennas," *IEEE Journal of Solid State Circuits*, vol. 41, no. 12, pp. 2795-2806, Dec. 2006.
36. G. Estep, R. Gupta, T. Hampsch, M. Zaharovits, L. Pryor, C. Chen, A. Zaghloul and F. Assal, “A C-Band Beam-forming Matrix for Phased-array Antenna Applications," in *IEEE MTT-S International Microwave Symposium Digest*, vol. 3, May 1995, pp. 1225-1228.
37. J. Butler and R. Lowe, “Beam-Forming Matrix Simplifies Design of Electronically Scanned Antennas," *Electronic Design*, pp. 170-173, April 1961.
38. J. Blass, “Multidirectional Antenna: A New Approach to Stacked Beams," in *IRE International Conference Record*, vol. 8, part 1, 1960.
39. T. Chu and H. Hashemi, “A CMOS UWB Camera with 7x7 Simultaneous Active Pixels," submitted to *ISSCC 2008*.
40. R. Jee-Youl B. Kim, and I. Sylla, “A new low-cost RF built-in self-test measurement for system-on-chip transceivers,” *IEEE Transactions on Instrumentation and Measurement*, vol. 55, no. 2, pp. 381-388, April 2006.

41. R. Staszewski, I. Bashir, and O. Eliezer, "RF built-in self test of a wireless transmitter," *IEEE Transactions on Circuits and Systems II*, vol. 54, no. 2, pp 186-190, February 2007.
42. A. Fenn, D. Temme, W. Delaney, and W. Courtney, "The development of phased-array radar technology," *Lincoln Laboratory Journal*, vol. 12, no. 2, pp. 321-340, 2000.
43. H. Aumann, A. Fenn, and F. Willwerth, "Phased array antenna calibration and pattern prediction using mutual coupling measurements," *IEEE Transactions on Antennas and Propagation*, vol. 37, no. 7, pp. 844-850, July 1989.
44. T. Rappaport, *Wireless Communications: Principles and Practice*, Prentice Hall, 1996.
45. S. M. Alamouti, "A Simple Transmit Diversity Technique for Wireless Communications," *IEEE Journal on Selected Areas in Communications*, vol. 16, no. 8, pp. 1451-1458, October 1998.