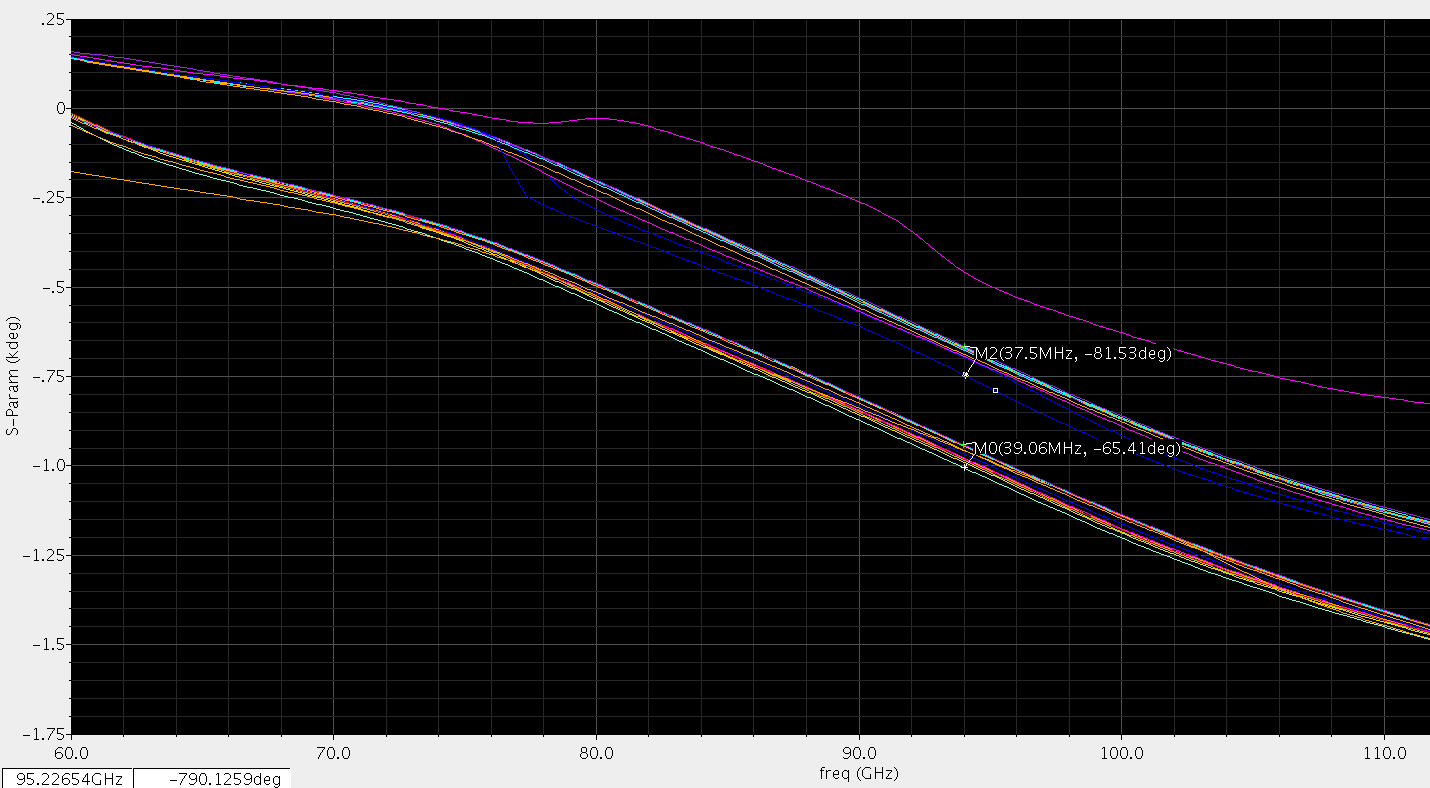
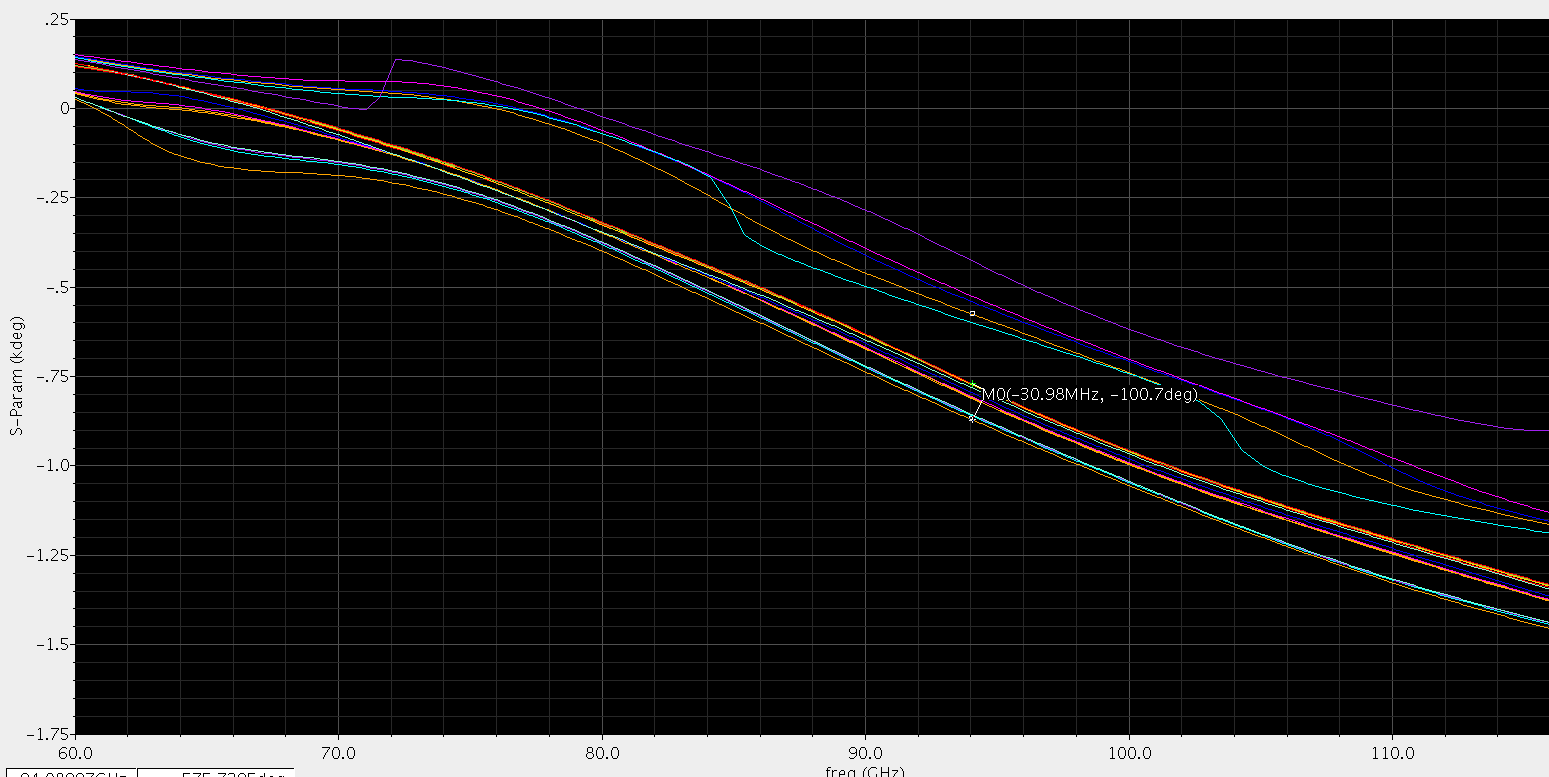
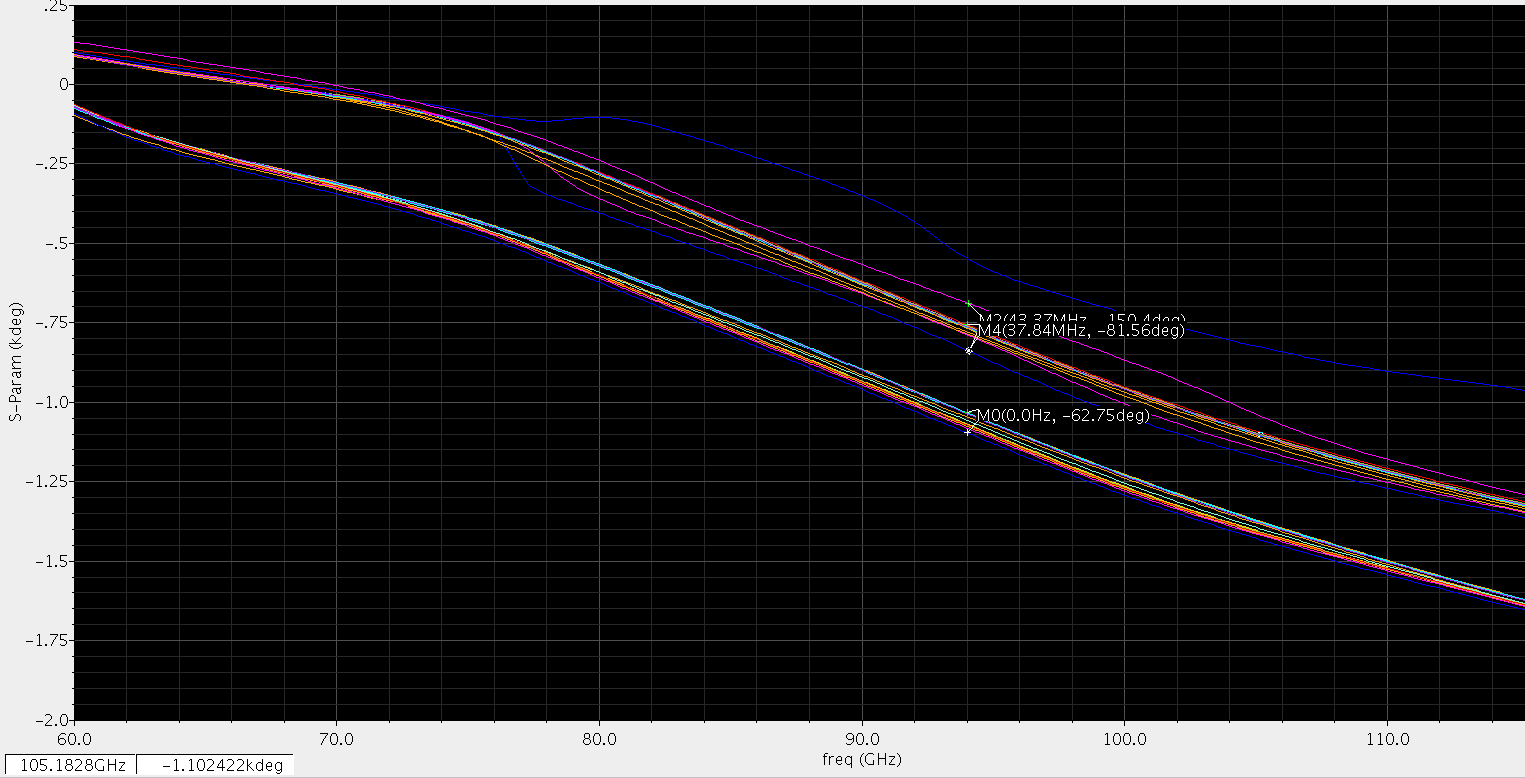
When path1 and path 3 is on,



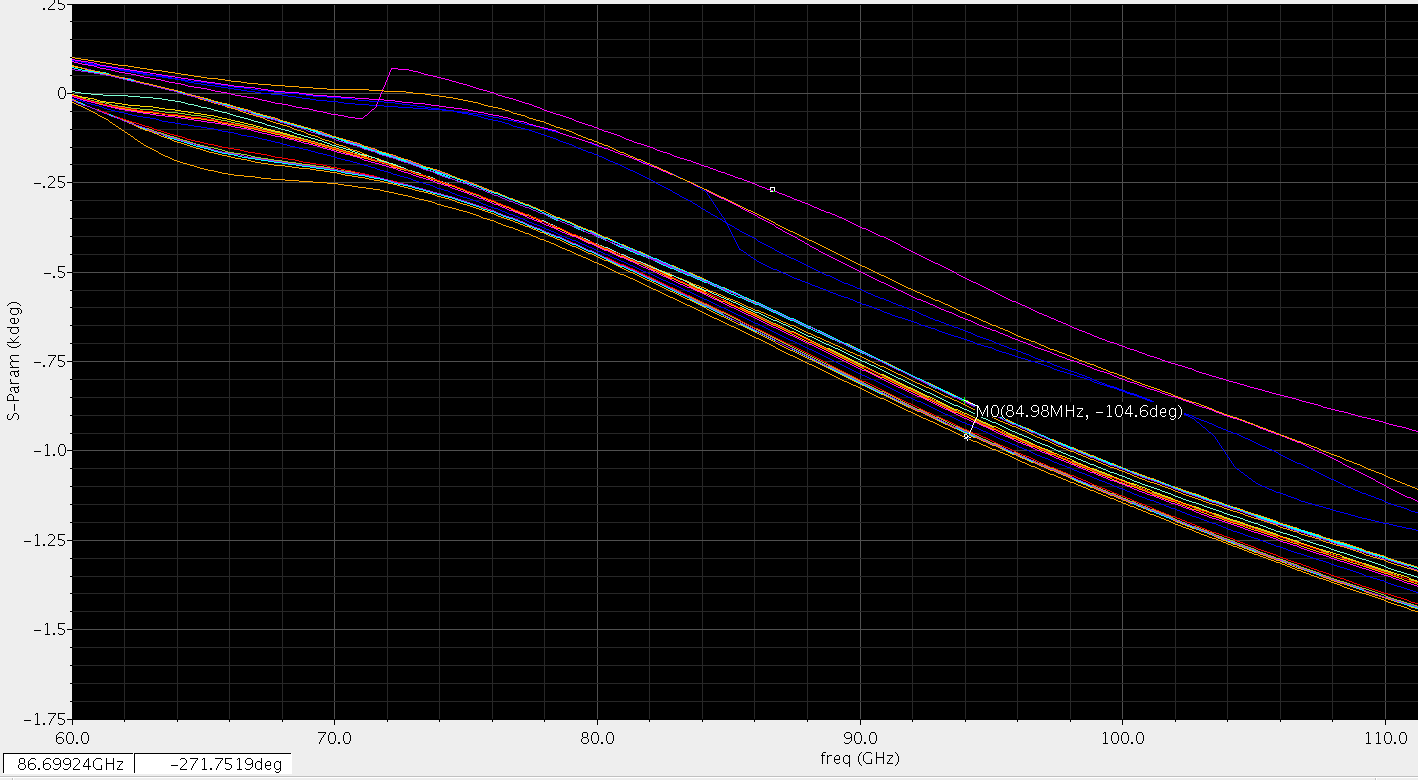
Path1 and path4 on



Path2 path 3 on

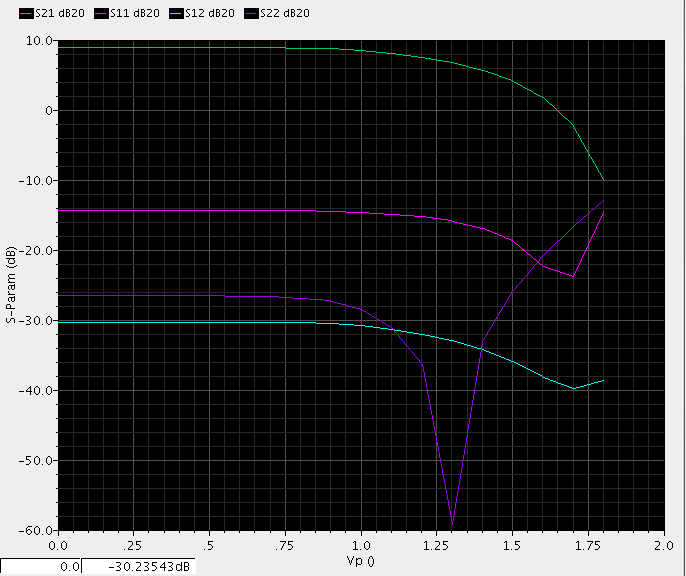


Path 2 and path 4 is ON

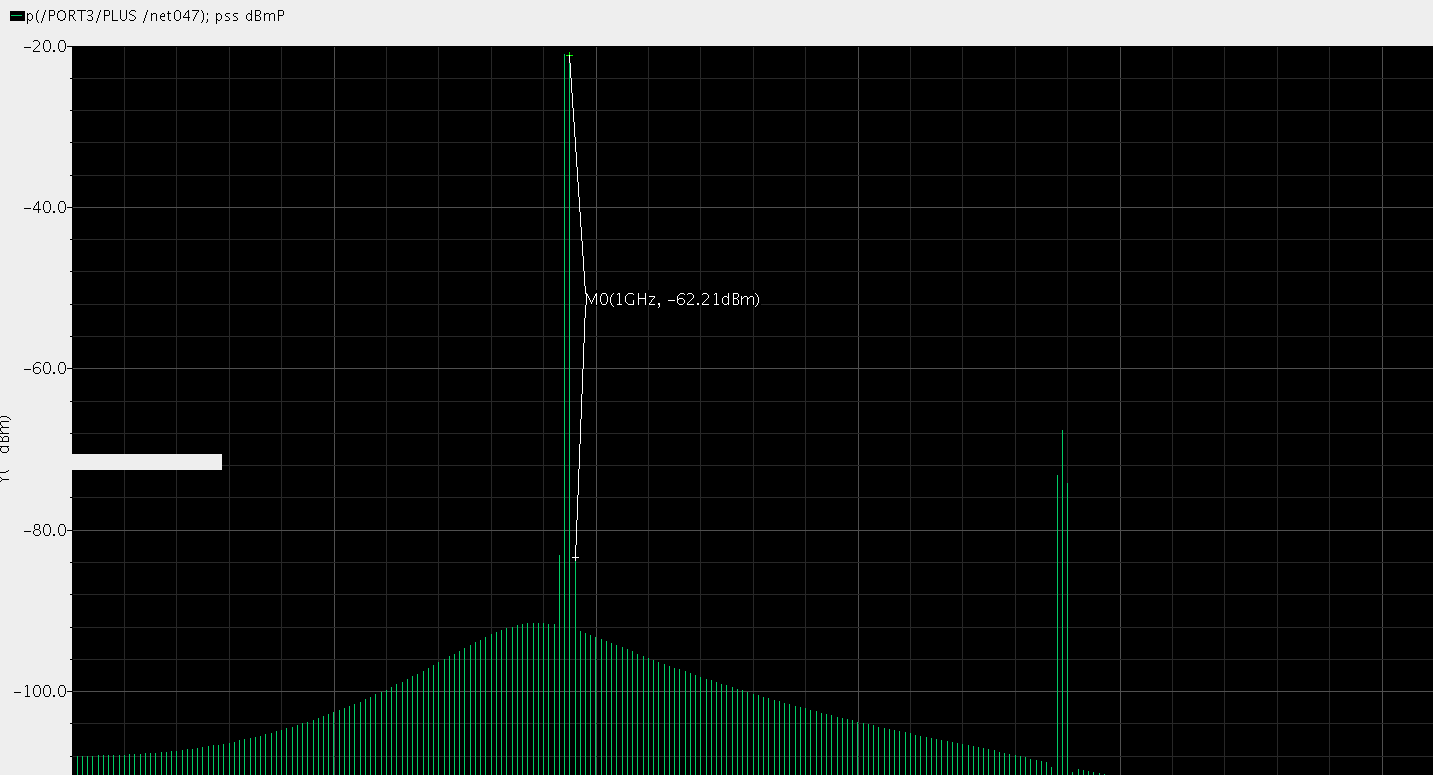


Using PMOS as controller:

Gate of PMOS voltage change of the excluded PMOS device,nf is 7.2db



PSS analysis:



When path 1 and path 3 is ON



When path 1 path 4 ON



When path 2 and path 3 ON



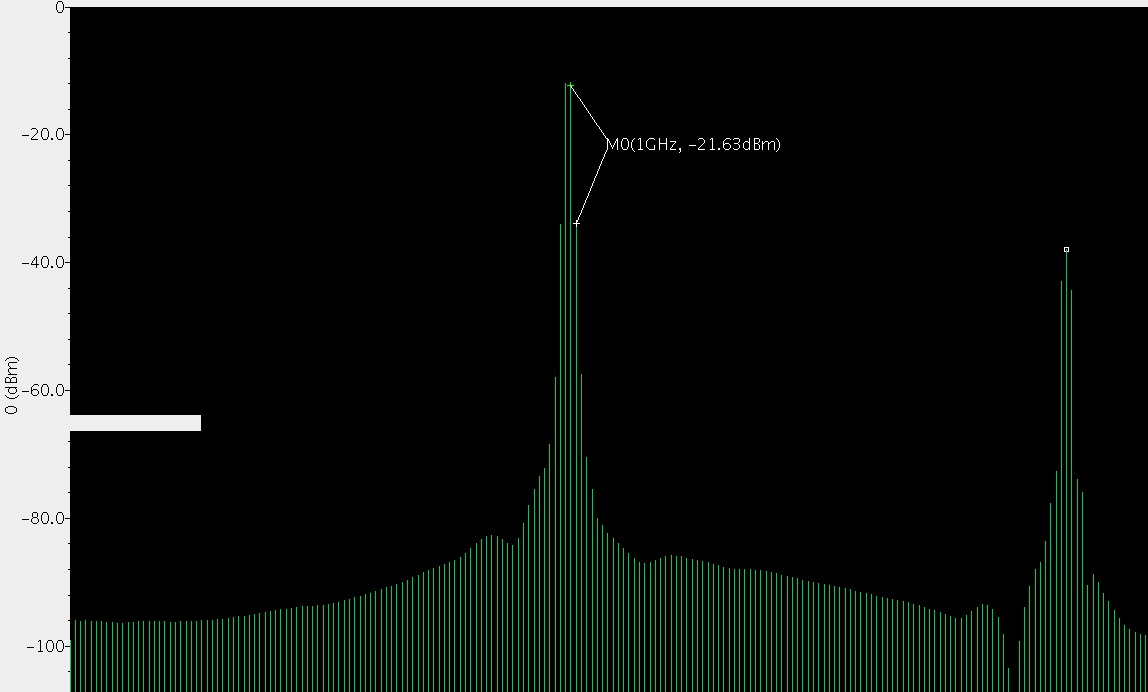
Path3 path 2 on

When vi and vq are both 1.8V then S21=1.54db

When vi=0 and vq=1.8V s21 is 19db

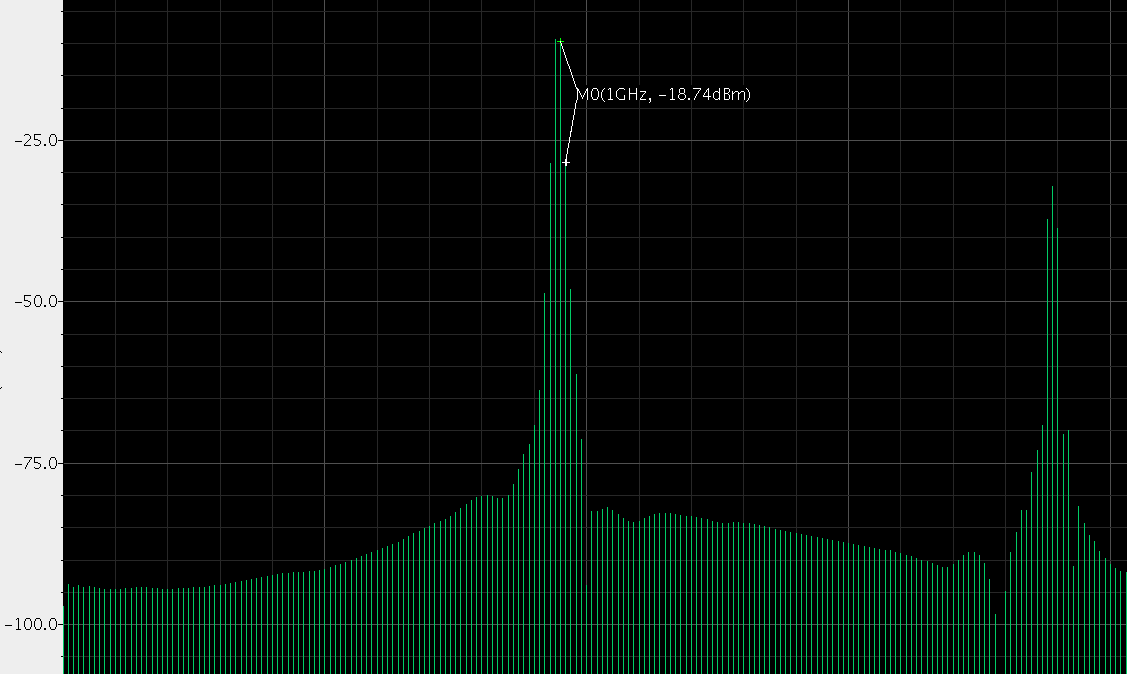
When vi=1.8 vq=0 s21 18.3db

PSS simulation od phase array when vc and vq is zero

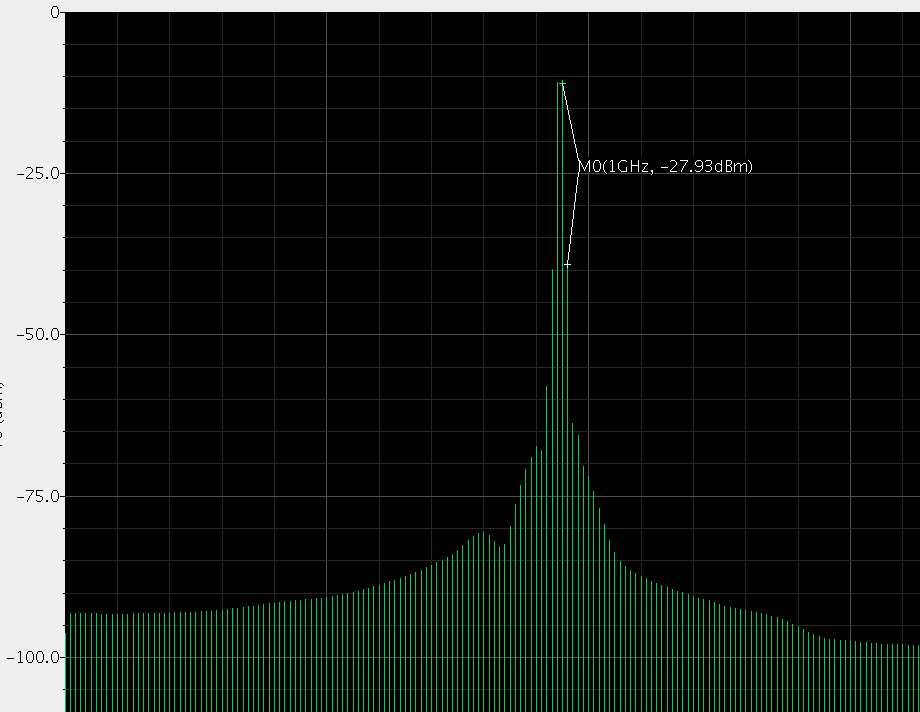


With V=2.5V when vc on vq off

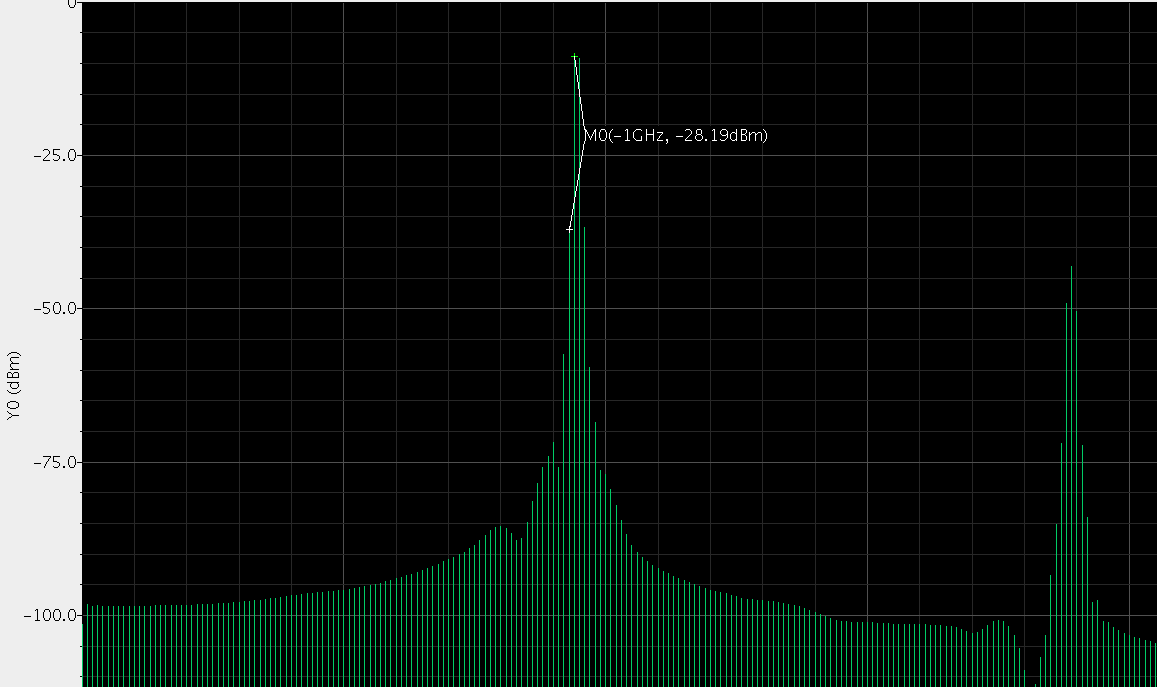
When vc and vq are 0V worst



When r=10 ohm at the emitter of Qmain



When vc=1 and vq=2.1V



When vc=1.5 and vq=2.1V

