Chapter 3
Inductive DC-DC Converter Topologies

The focus of this work is on the design and implementation of monolithic inductive DC-DC converters into standard CMOS IC technologies. Therefore, a more extensive discussion on inductive converter topologies is provided in this chapter. This involves obtaining insight into the basic operation principles of the different converter topologies and a comparison of a selection of these topologies. Thus allowing the determination the fundamental and intrinsic advantages and drawbacks of the different converter topologies, with the aim towards monolithic integration. These advantages and drawbacks may well differ from converter topologies that are not intended for monolithic integration, as the on-chip area requirement and available devices are much more restricted. Please note that a full coverage on inductive type DC-DC converter topologies is not intended and that merely the most promising and practical converter topologies are discussed.

The primary classes of non-galvanically separated step-down, step-up and step-up/down inductive converter topologies are discussed. These topologies are categorized according to their non-inverting voltage conversion range in the respective Sects. 3.1, 3.2 and 3.3. This categorization differs from the traditional one in the sense that only positive output voltages are considered, as the on-chip conversion towards negative voltages is omitted in this work. The converters of each of the three categories are compared in terms of their circuit topology, their basic operation and their area requirement. The comparison of the area requirement is conducted by means of SPICE-simulations.

The derived classes of DC-DC converter topologies, such as galvanically separated converters and resonant converters, are addressed in Sect. 3.4. Topology variations on the primary classes of converter topologies, incorporating multi-phase converters and Single-Inductor Multiple Output (SIMO) converters, are discussed in Sect. 3.5. Finally, the chapter is concluded in Sect. 3.6.

3.1 Step-Down Converters

Inductive DC-DC step-down converters are used to convert the input voltage U_{in} to a lower output voltage U_{out}. The application principle of DC-DC step-down con-

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verters in battery-operated systems is explained in Sect. 1.2.2. In this section five different ideal inductive DC-DC step-down converter topologies are discussed and compared with one another. This is done in view of monolithic integration, where the occupied area of the converter is a crucial parameter that is to be minimized for cost reasons. The topologies explained in this section are:

- The buck converter
- The bridge converter
- The three-level buck converter
- The buck^2 converter
- The Watkins-Johnson converter

The dominant parameters, which determine the required converter area, are the values of the passives: the inductor(s) and capacitor(s). Because ideal inductive DC-DC converters are lossless, as explained in Sect. 2.3, the power conversion efficiency η_{SW} is not a suitable parameter for a comparison. In contrast, the output voltage ripple ΔU_{out} is not infinitesimal for ideal inductive DC-DC converters, having finite values for L, C and f_{SW}. Indeed, in the previous Sect. 2.3.3 it is deduced, for a boost converter example, that the dependency of ΔU_{out} includes several input and output parameters of the converter. This is formally described by (2.65) and (2.74), for CCM and DCM respectively. Thus, different ideal step-down converter topologies can be designed for equal specifications, including ΔU_{out}, allowing them to be compared by means of the required values of the passives and indirectly by their required area.

In Sect. 2.3.3 it is mathematically proven that the capacitance of the output capacitor C of a boost converter is always a determining parameter for ΔU_{out}, the evidence that this is true for all inductive DC-DC converters is trivial. Thus, by keeping the input and output parameters of the converter constant, except for the capacitance of C, the value of C can be determined for the different topologies having the same specifications. The parameters which are kept constant and their values are listed in Table 3.1. These values are chosen such that they are in the same order of magnitude as the values used in real monolithic implementations, which can be verified in Chap. 6.

The calculations for this comparison are executed through SPICE simulations only, except for the buck converter for which the calculations are also performed by means of the small-ripple approximation, charge-balance and volt-second balance. This allows for validating these calculation methods through simulations. These simulations and calculations allow for an area-driven comparison, which is mandatory for monolithic integration. However, the required area is not the sole property that needs to be taken into account when choosing a topology. Therefore, a brief circuit-level discussion is given for each converter topology.

3.1.1 Buck Converter

The circuit of an ideal buck-converter, shown in Fig. 3.1(a), is explained more in detail than the other DC-DC step-down converter topologies, because this converter

Table 3.1 The input and output parameters, together with their values, used to compare different DC-DC step-down converter topologies

Input/output parameter	Value
Input voltage U_{in}	2 V
Output voltage U_{out}	1 V
Output voltage ripple ΔU_{out}	50 mV
Total inductance L_{tot}	10 nH
Switching frequency f_{SW}	100 MHz
Output power 1 P_{out_1}	1 mW
Load resistance 1 R_{L_1}	1 kΩ
Output power 2 P_{out_2}	10 mW
Load resistance 2 R_{L_2}	100 Ω
Output power 3 P_{out_3}	100 mW
Load resistance 3 R_{L_3}	10 Ω
Output power 4 P_{out_4}	1 W
Load resistance 4 R_{L_4}	1 Ω

is the base of many of the implementations, discussed in Chap. 6. First the principle of operation for CCM is explained. In this CM the current $i_L(t)$ through the inductor L always has a positive, finite value and it is described in two phases:

1. *The inductor charge phase* Φ_1: The equivalent circuit for Φ_1, shown in Fig. 3.1(b), is achieved by closing SW_1 and opening SW_2 for a certain on-time t_{on}. During Φ_1 L is charged in series with C and R_L by U_{in}, causing $i_L(t)$ to increase from its minimal value I_{L_min} to its maximal value I_{L_max}, as shown in Fig. 3.2. When $i_L(t)$ becomes larger than the output current $i_{out}(t)$, C is also

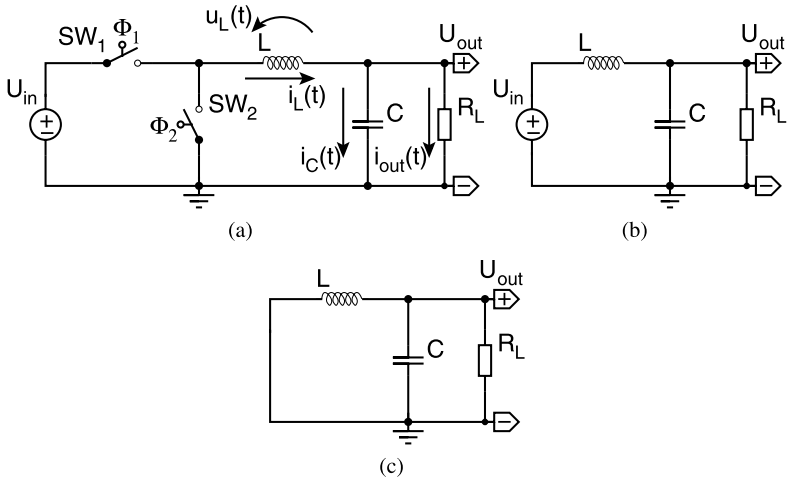

Fig. 3.1 **(a)** The circuit of an ideal buck DC-DC converter. **(b)** The equivalent circuit of the inductor charge phase and **(c)** the inductor discharge phase

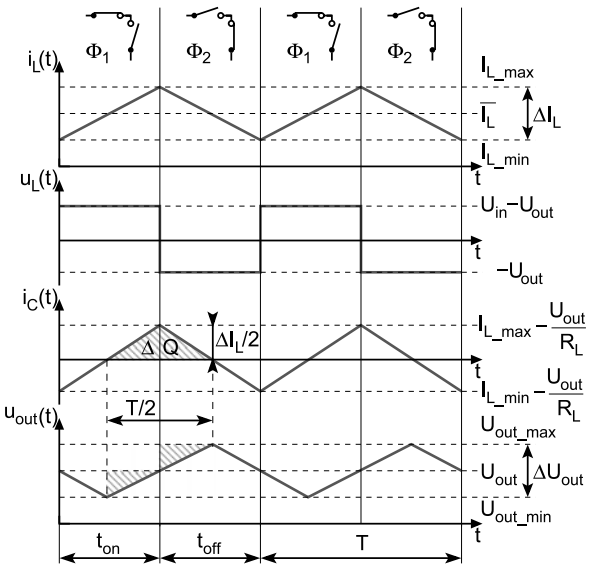

Fig. 3.2 The linearized $i_L(t)$, the linearized $u_L(t)$, the linearized $i_C(t)$ and the linearized $u_{out}(t)$ as a function of time, for an ideal buck DC-DC converter in CCM

being charged. Before this point R_L is powered through C and afterwards R_L is powered through U_{in}, because the DC-component of $i_L(t)$ flows through R_L.

2. *The inductor discharge phase* Φ_2: The equivalent circuit for Φ_2 is shown in Fig. 3.1(c), which is achieved by opening SW_1 and closing SW_2 for a certain off-time t_{off}. During Φ_2 L is discharged into C and R_L, causing $i_L(t)$ to decrease from I_{L_max} to I_{L_min}, as shown in Fig. 3.2. During the first part of Φ_2, $i_L(t)$ is larger than $i_{out}(t)$, causing C to be further charged by L and R_L to be powered by the DC-component of $i_L(t)$. After this first part of Φ_2, R_L is powered by discharging L and C.

Because L is not discharged in series with U_{in}, it can intuitively be seen that U_{out} will always be lower than U_{in}. For CCM this is confirmed by (3.1), which gives the voltage conversion ratio $k(\delta)$. It is observed that, similar to an ideal boost converter, $k(\delta)$ only depends on the duty-cycle δ for CCM. This relation is plotted by the black curve in the upper graph of Fig. 3.4.

$$k(\delta) = \delta \tag{3.1}$$

In DCM $i_L(t)$ varies between a finite, positive value and zero. The operation of an ideal DC-DC buck converter in this CM consists of three phases:

1. *The inductor charge phase* Φ_1: The equivalent circuit for Φ_1, shown in Fig. 3.1(b), is achieved by closing SW_1 and opening SW_2 for a certain on-time t_{on}. During Φ_1 L is charged in series with C and R_L by U_{in}, causing $i_L(t)$ to increase from zero to its maximal value I_{L_max}, as shown in Fig. 3.3. From the point where $i_L(t)$ becomes larger than the output current $i_{out}(t)$ C is also being charged. Before this point R_L is powered through C and after this point R_L is powered through U_{in}, because the DC-component of $i_L(t)$ flows through R_L.

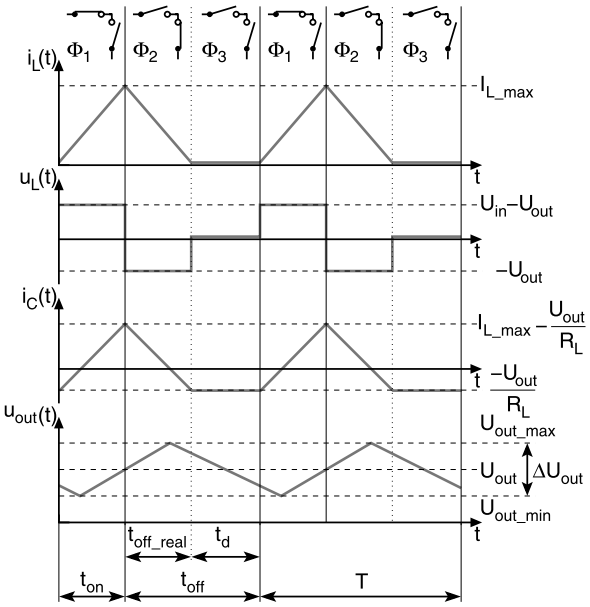

Fig. 3.3 The linearized $i_L(t)$, the linearized $u_L(t)$, the linearized $i_C(t)$ and the linearized $u_{out}(t)$ as a function of time, for an ideal buck DC-DC converter in DCM

2. *The inductor discharge phase* Φ_2: The equivalent circuit for Φ_2 is shown in Fig. 3.1(c), which is achieved by opening SW_1 and closing SW_2 for a certain real off-time t_{off_real}. During Φ_2 L is discharged into C and R_L, causing $i_L(t)$ to decrease from I_{L_max} to zero, as can be seen in Fig. 3.2. During the first part of Φ_2 $i_L(t)$ is larger than $i_{out}(t)$, causing C to be further charged by L and R_L to be powered by the DC-component of $i_L(t)$. After this first part of Φ_2 R_L is powered by both discharging L and C.
3. *The dead-time phase* Φ_3: The equivalent circuit for Φ_3 consists of the series connection of C and R_L, which is achieved by both opening SW_1 and SW_2 for a certain dead-time t_d. This prevents $i_L(t)$ from becoming negative, thereby shorting C to the ground.

For of a buck converter in DCM $k(\delta)$ can be calculated analogue to a boost converter, which is explained in Sect. 2.3.3, yielding (3.2). The graphical representation of $k(\delta)$ for DCM is plotted by the gray curves of the upper graph in Fig. 3.4, for different values of $(2L)/(R_L T)$.

$$k(\delta) = \frac{2}{1 + \sqrt{1 + \frac{4\frac{2L}{R_L T}}{\delta^2}}} \tag{3.2}$$

The CB is calculated similar to a boost converter and it is defined by (3.3). When this condition is true, the buck converter operates in CCM.

$$\frac{2L}{R_L T} > 1 - \delta \tag{3.3}$$

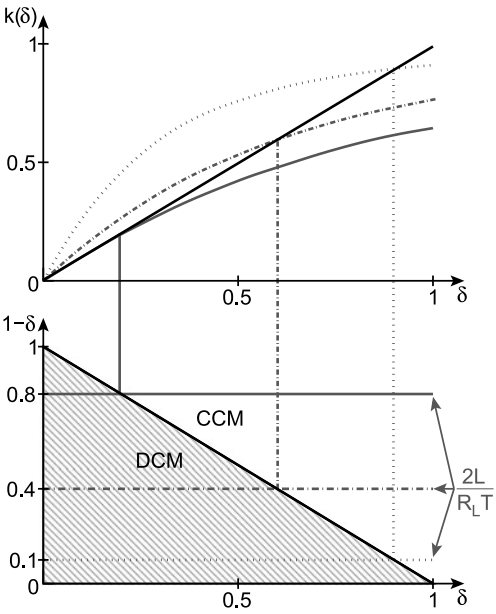

Fig. 3.4 The *upper graph* shows $k(\delta)$ as a function of δ, where the *black curve* is valid for CCM and the *gray curves* for DCM. In the *lower graph* the *black curve* shows the boundary between the two CMs and the *gray curves* illustrate three numerical examples. These graphs are valid for an ideal DC-DC buck converter

This boundary is plotted by the black curve of the lower graph in Fig. 3.4. The gray curves in this graph denote the three different values of $(2L)/(R_L T)$: 0.1, 0.4 and 0.8, for which $k(\delta)$ is plotted in the upper graph. It is observed that the buck converter will have the tendency to work in CCM for higher inductance values L, lower load resistance values R_L (higher loads) and shorter switching periods T (higher frequencies f_{SW}). When $(2L)/(R_L T)$ reaches a value that is higher than one, the converter will always operate in CCM.

The method explained in Sect. 2.3.3 for the calculation of the output voltage ripple ΔU_{out} of a boost converter is not applicable for the buck converter, because L is a part of the output filter. As a consequence, the waveform of U_{out} will be continuous, rather than piecewise linear as illustrated in Figs. 3.2 and 3.3. Therefore, an alternative method, based on the charge balance of C, is used to calculate ΔU_{out}.

This method is explained for the buck converter in CCM. The current $i_L(t)$ is divided over $i_C(t)$ and $i_{out}(t)$, as shown in Fig. 3.1(a). When the converter operates in steady-state the net change in $u_{out}(t)$ is zero, hence the DC-component of $i_C(t)$ is also zero. This implies that the DC-component of $i_L(t)$ flows through R_L. The AC-component of $i_L(t)$ entirely flows through C and is equal to the current ripple ΔI_L through L, as shown in Fig. 3.2. ΔI_L is calculated through (3.4), where the unknown mean output voltage $\overline{U_{out}}$ can be substituted by the known parameters of (3.1).

$$\begin{aligned} \Phi_1 : 0 \rightarrow t_{on} \quad &\Longrightarrow \quad \frac{di_L(t)}{dt} = \frac{U_{in} - \overline{U_{out}}}{L} \\ &\Longrightarrow \quad \Delta I_L = \frac{U_{in} - \overline{U_{out}}}{L} t_{on} = \frac{U_{in} - \delta U_{in}}{L} t_{on} \end{aligned} \tag{3.4}$$

In Fig. 3.2 it can also be seen that the positive portion of $i_C(t)$ causes u_{out} to rise and vice versa. This is due to the fact that the injected positive charge change ΔQ into C causes ΔU_{out}, which follows from (3.5).

$$\Delta U_{out} = \frac{\Delta Q}{C} \tag{3.5}$$

This positive portion of $i_C(t)$ always has a duration of $T/2$ because the DC-component of $i_C(t)$ is zero and because the waveform of $i_C(t)$ is symmetrical, implying that the amplitude of $i_C(t)$ is equal to $\Delta I_L/2$. With this knowledge ΔQ can be calculated as the area underneath the positive portion of $i_C(t)$, yielding (3.6).

$$\Delta Q = \int_0^{\frac{T}{2}} i_C(t)\,dt = \frac{\frac{\Delta I_L}{2} \cdot \frac{T}{2}}{2} \tag{3.6}$$

Finally, ΔU_{out} for CCM is found by substituting (3.6) into (3.5), which yields (3.7).

$$\Delta U_{out} = \frac{(\delta - \delta^2)T^2 U_{in}}{8CL} = \frac{t_{on}t_{off}U_{in}}{8CL} \blacksquare \tag{3.7}$$

It can be seen that ΔU_{out} is inversely proportional to both the values of C and L, which is due to the fact that they are both part of the output filter. There is also a linear dependency on T, following from the fact that T influences ΔI_L, which in-turn influences ΔU_{out}. Remarkably, ΔU_{out} is not dependent on R_L, because of the fact that ΔU_{out} is only dependent on ΔI_L, which is in-turn not influenced by R_L.

The method for calculating ΔU_{out} can also be used for DCM, yielding (3.8).

$$\Delta U_{out} = \frac{U_{in}(L\overline{U_{out}} + R_L t_{on}(\overline{U_{out}} - U_{in}))^2}{2CLR_L^2\overline{U_{out}}(U_{in} - \overline{U_{out}})} \tag{3.8}$$

Similar dependencies on parameters as in (3.7) are observed in (3.8). The parameter $\overline{U_{out}}$ can be substituted by the small-ripple approximation for U_{out}, given by (3.2), which is not performed here to minimize the complexity. The dependency on t_{off} is not explicitly visible in (3.8), nevertheless this follows from the dependency on $\overline{U_{out}}$. In addition ΔU_{out} is dependent on R_L in DCM, which is not the case for CCM. This is due to the dead-time period t_d where the converter is idle and C is being discharged through R_L, thereby lowering $u_{out}(t)$.

Table 3.2 shows the results of the SPICE simulations for the ideal buck converter, in order to comply with the specification of Table 3.1, for four different P_{out}. The two remaining degrees of freedom, namely the capacitance of C and δ, are provided together with t_{off_real} and the CM. As expected, the required capacitance, for equal L, f_{SW}, U_{in} and U_{out}, increases upon an increasing P_{out}. Also, the required δ in DCM, to maintain U_{out}, increases upon an increasing P_{out}. This follows from the fact that in DCM U_{out} is dependent on R_L. Although not explicitly shown in Table 3.2, it is noted that both the equations for $k(\delta)$, (3.1) and (3.2), and both the equations for ΔU_{out}, (3.7) and (3.8), yield exactly the same results as obtained with the SPICE-simulations of the ideal DC-DC buck converter.

To conclude the discussion on the ideal DC-DC buck converter possible benefits (✔) and drawbacks (✘), in view of monolithic integration, are provided:

Table 3.2 The SPICE-simulations results for the required capacitance C, to comply with the specifications of Table 3.1, of an ideal DC-DC buck converter, for four different output powers P_{out}. The required duty-cycle δ and the CM are also provided

P_{out}	C	δ	t_{off_real}	CM
1 mW	0.19 nF	3.15%	0.315 ns	DCM
10 mW	1.6 nF	10%	1 ns	DCM
100 mW	9.5 nF	31.5%	3.15 ns	DCM
1 W	12.5 nF	50%	5 ns	CCM

✔ Both the switches have one terminal connected to a fixed potential: SW_1 to U_{in} and SW_2 to the ground *GND* of the circuit. This is beneficial for the implementation of the switches with MOSFETs, which are switched on and off by controlling the gate voltage relative to the source voltage (see Sect. 1.3.1).
✔ Only one inductor and capacitor is used, which can be beneficial for the area requirement of the converter.
✔ The output current $i_{out}(t)$ is continuously provided by L, in CCM. Thus, no current-peaks are fed to the output which would increase ΔU_{out} for real output capacitors, having a finite parasitic series resistance (*ESR*) and parasitic series inductance (*ESL*). Although the current delivered by L in DCM for the output is not continuous, no sudden transients occur in it. This follows from the fact that the output filter consists of both and inductor and a capacitor.
✔ The converter delivers a non-inverted U_{out}, of which the *GND*-references of in- and output are physically connected with each other. This would otherwise cause problems in standard CMOS-technologies, where the substrate is connected with the *GND*-potential.
✘ The input current through U_{in} is discontinuous, having a negative impact on the overall performance of a real converter due to non-zero parasitic input resistances and inductances. Therefore, real implementations might require an additional on-chip decouple capacitor, resulting in an increasing overall area requirement.
✘ CCM is only reached for a sufficiently high P_{out}. Therefore, the advantage of the continuous output current is lost for low values of P_{out}.

3.1.2 Bridge Converter

The circuit of an ideal bridge DC-DC converter is shown in Fig. 3.5. This converter is capable of delivering a positive or a negative U_{out}, of which the absolute value is always lower than U_{in}. This is confirmed by (3.9), which shows that $k(\delta)$ is only dependent on δ for CCM. The calculation method to obtain (3.9) is explained in Sect. 2.3.3. The equation and explanation for DCM is omitted, as this provides limited added value.

$$k(\delta) = 2\delta - 1 \tag{3.9}$$

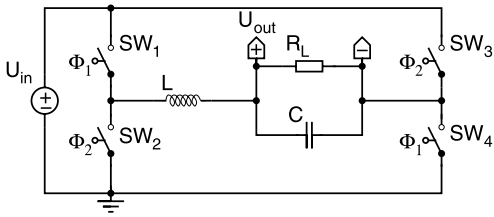

Fig. 3.5 The circuit of an ideal bridge DC-DC converter

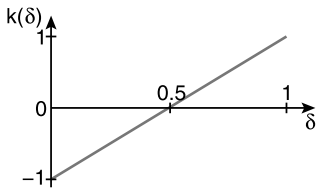

Fig. 3.6 The voltage conversion ratio $k(\delta)$ as a function of the duty-cycle δ, for a bridge converter in CCM

The graphical representation of (3.9) is illustrated in Fig. 3.6, where $k(\delta)$ is shown as a function of δ. It is observed that $k(\delta)$ becomes positive for values of δ larger than 50%. This discussion is limited to this region only, because on-chip negative voltages are rarely used. It can be intuitively understood that the operation of the converter in the negative region of $k(\delta)$ is dual to the positive region of $k(\delta)$.

The basic operation of the bridge converter in CCM, with a positive U_{out}, consists of the following two phases:

1. *The inductor charge phase* Φ_1: During Φ_1 SW_1 and SW_4 are closed while SW_2 and SW_3 are opened, for a time t_{on}. The positive U_{in} is applied over the series connection of L and C. This causes the, already flowing, current through L to increase, thereby charging both L and C and providing power to R_L.
2. *The inductor discharge phase* Φ_2: During Φ_2 SW_1 and SW_4 are closed while SW_2 and SW_3 are opened, for a time t_{off}. The negative $-U_{in}$ is applied over the series connection of L and C. This causes the current through L to decrease, thereby inverting the current through C for powering R_L.

In DCM a third phase occurs where the current through L becomes zero a the end of Φ_2. At this point SW_2 and SW_3 are also opened, preventing the current trough L from becoming negative and discharging C. This results in a certain t_d, during which the converter is idle.

The results of the SPICE simulations for the ideal bridge converter, in order for it to comply with the specifications of Table 3.1, are listed in Table 3.3. It is observed that in order to maintain ΔU_{out} constant, the required capacitance of C increases upon an increasing P_{out}. This results in a larger required capacitance compared to ideal buck converter. Also, the δ-range is larger for the ideal bridge converter than for the buck converter, for the same P_{out}-range.

The discussion on the ideal DC-DC bridge converter is concluded with its possible benefits and drawbacks:

Table 3.3 The SPICE-simulations results for the required capacitance C, to comply with the specifications of Table 3.1, of an ideal DC-DC bridge converter, for four different output powers P_{out}. The required duty-cycle δ and the CM are also provided

P_{out}	C	δ	t_{off_real}	CM
1 mW	0.19 nF	3.85%	0.125 ns	DCM
10 mW	1.69 nF	12.1%	0.405 ns	DCM
100 mW	11.5 nF	38.5%	1.3 ns	DCM
1 W	19 nF	75%	2.5 ns	CCM

✔ The four switches have one of their terminals connected to a fixed potential: SW_1 and SW_3 to U_{in}, SW_2 and SW_4 to GND. This simplifies the drive circuits for the MOSFETs gates, which will be used to implement the switches.
✔ In CCM L provides a continuous current to the output, avoiding current peaks through C and the output. These would cause ΔU_{out} to increase, due to the ESR and ESL of a non-ideal C.
✔ In CCM the current drawn from U_{in} is continuous. Thus, the on-chip U_{in} will be less influenced by the voltage drop over parasitic resistance and inductances at the input. In DCM the current draw from U_{in} will not be continuous, however there are also no sudden current steps. This is in contrast to a buck converter.
✘ Four switches are required, implying more area, a more complex driver and increased conduction and switching losses, compared to the buck converter.
✘ The output cannot be referred to the GND of the converter, which is associated with the chip's substrate. The on-chip circuitry to be supplied with the converter's output will therefore not be allowed to have a substrate reference. This can be a problem in standard CMOS IC technologies, where the bulk and source of a standard n-MOSFET are physically inextricably connected to the substrate.
✘ It shows that the bridge converter requires a larger output capacitance C than a buck converter, to obtain the same ΔU_{out}. This difference is minimal at low values of P_{out}, nevertheless it becomes significant at high values of P_{out}.
✘ CCM is only reached for a sufficiently high P_{out}. Therefore, the advantage of the continuous output current is lost for low values of P_{out}.

3.1.3 Three-Level Buck Converter

Figure 3.7 shows the circuit of an ideal three-level buck[1] DC-DC converter. Multi-level DC-DC converters were originally introduced for high-voltage conversion applications [Mey92], nevertheless monolithic integration in a CMOS technology has been attempted [Vil08].

[1] Multi-level implementations are also possible for other DC-DC converter topologies, such as the bridge converter. These topology variants are however not discussed in this work, as they increase the complexity by adding switches and capacitors.

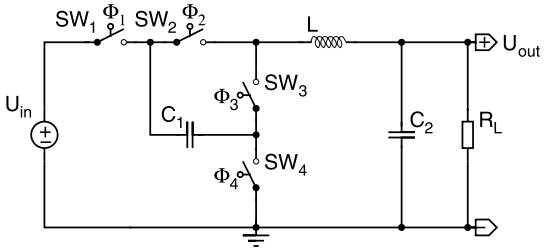

Fig. 3.7 The circuit of an ideal three-level buck DC-DC converter

The three-level buck converter is capable of converting U_{in} to a lower, non-inverted U_{out}. It can be proven that for CCM $k(\delta)$ is equal to that of a regular ideal buck converter, which is given by (3.1). The graphical representation of $k(\delta)$ as a function of time, is illustrated in Fig. 3.4 by the black curve in the upper graph.

The timing of the four switches in CCM is shown in Fig. 3.8(a) for $\delta < 0.5$ and in Fig. 3.8(b) for $\delta > 0.5$. The operation in CCM for $\delta < 0.5$ consists of the following four phases:

1. *The inductor charge, capacitor charge phase* Φ_1: During Φ_1 SW_1 and SW_3 are closed and SW_2 and SW_4 are opened, during a time t_{on}. Both L and C_1 are charged in series by U_{in}, thereby also charging C_2 and powering R_L.
2. *The first inductor discharge phase* Φ_2: During Φ_2 SW_3 and SW_4 are closed and SW_1 and SW_2 are opened, during a time $(t_{off} - t_{on})/2$. L is discharged through R_L and partially through C_2. C_1 is disconnected.
3. *The inductor charge, capacitor discharge phase* Φ_3: During Φ_3 SW_2 and SW_4 are closed and SW_1 and SW_3 are opened, during a time t_{on}. C_1 is discharged, thereby charging L, C_2 and R_L.
4. *The second inductor discharge phase* Φ_4: This phase is identical to Φ_2.

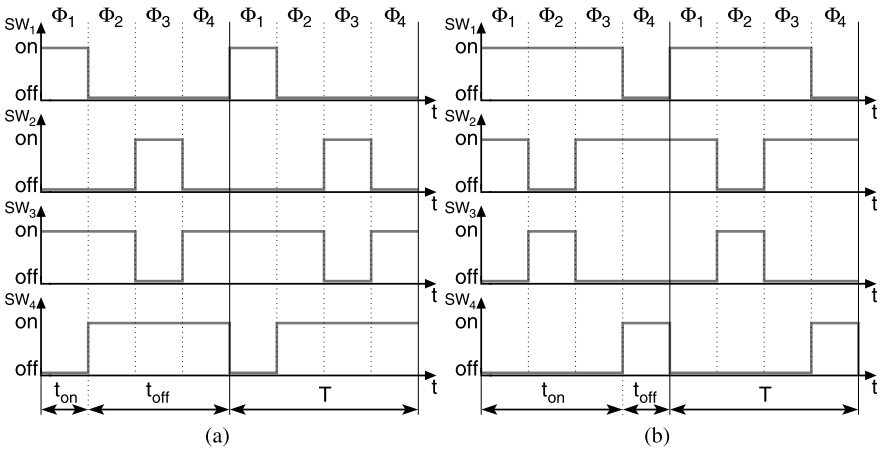

Fig. 3.8 **(a)** The timing of the four switches of an ideal three-level buck DC-DC converter in CCM, for $\delta < 0.5$ and **(b)** for $\delta > 0.5$

Table 3.4 The SPICE-simulations results for the required capacitances C_1 and C_2, to comply with the specifications of Table 3.1, of an ideal three-level buck DC-DC converter, for four different output powers P_{out}. The required duty-cycle δ and the CM are also provided

P_{out}	C_1	C_2	$C_{tot} = C_1 + C_2$	δ	t_{off_real}	CM
1 mW	0.3 nF	0.06 nF	0.36 nF	27%	0 ns	DCM
10 mW	0.5 nF	0.16 nF	0.66 nF	50%	5 ns	BCM
100 mW	5 nF	0 nF	5 nF	50%	5 ns	CCM
1 W	50 nF	0 nF	50 nF	50%	5 ns	CCM

The operation in CCM for $\delta > 0.5$ consists of the following four phases:

1. *The first inductor charge phase* Φ_1: During Φ_1 SW_1 and SW_2 are closed and SW_3 and SW_4 are opened, during a time $(t_{on} - t_{off})/2$. L is charged by U_{in}, thereby charging C_2 and R_L. C_1 is disconnected.
2. *The inductor discharge, capacitor charge phase* Φ_2: During Φ_2 SW_1 and SW_3 are closed and SW_2 and SW_4 are opened, during a time t_{off}. The series connection of U_{in}, C_1 and L causes L to be discharged and C_1 to be charged. The current from this series circuit powers R_L and also partially C_2.
3. *The second inductor charge phase* Φ_3: This phase is identical to Φ_1.
4. *The inductor discharge, capacitor discharge phase* Φ_4: During Φ_4 SW_2 and SW_4 are closed and SW_1 and SW_3 are opened, during a time t_{off}. The series connection of C_1 and L causes both of them to be discharged into R_L and partially into C_2.

It can be proven that the mean voltage over the flying capacitor C_1 is always $U_{in}/2$, for steady-state operation. It is also observed that the input node of the output filter can have three different voltage levels: *GND*, $U_{in}/2$ or U_{in}. Hence resulting in a three-level converter.[2] Please note that DCM is not considered in this discussion.

The results of the SPICE simulations for the ideal three-level buck converter, in order for it to comply with the specifications of Table 3.1, are listed in Table 3.4. The value of C_1 was chosen such that the voltage swing over it equals 100 mV. This value is chosen such that the voltage drop over each of the four switches is limited to $U_{out} + 10\%$. Assuming that U_{out} equals the nominal CMOS technology supply voltage, this allows for the switches to be implemented as single MOSFET transistors. When allowing a larger ripple voltage over C_1 the switches would have to be implemented as stacked transistors or thick-oxide devices, to cope with the high voltage. This assumption follows from realized DC-DC step-down designs, which will be elaborated upon in Chap. 6. The value of C_1 can also not be chosen to be smaller than 0.3 nF, because the resonance frequency of C_1 and L will approach the switching frequency f_{SW}. This would cause the current through L to become negative before the ending of the switching period, as explained in Sect. 2.3.2, which is undesired.

[2] A regular buck-converter is a two-level converter, because the voltage on the input node of the output filter can be either *GND* or U_{in}.

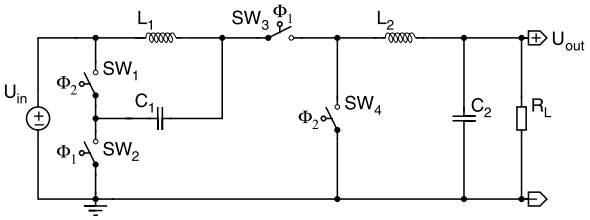

Fig. 3.9 The circuit of an ideal buck^2 DC-DC converter

It is observed that the converter requires no output capacitor C_2 for $P_{out} = 1$ W and $P_{out} = 100$ mW, which yields respective ΔU_{out} of 34 mV and 50 mV. However, for lower P_{out} a small value of C_2 is required. For the two largest P_{out} the converter operates in CCM and at $P_{out} = 10$ mW it operates at the boundary between the two CMs, which is also referred to as boundary condition mode (BCM). This is in contrast with a buck and bridge converter, which only tend to operate in CCM for the highest P_{out}. Therefore, the δ-range for this converter is smaller, for the same P_{out}-range.

To conclude this discussion the benefits and drawbacks of this converter are provided:

✔ In CCM L provides a continuous current to the output, relaxing the specifications of C_2. When the minimal P_{out} is large enough, C_2 can even be omitted.
✔ U_{out} is not inverted and referred to GND.
✔ CCM is maintained for a broad range of P_{out}, which is beneficial for ΔU_{out}.
✔ The total required capacitance C_{tot} is lower compared to a buck or bridge converter, at low values for P_{out}.
✘ SW_2 and SW_3 do not have a terminal which is connected to a fixed potential, implying a more complex driver is required.
✘ The mean voltage on C_1 tends to drift above U_{in} or GND, when the timing of the switches is not exactly as prescribed by Fig. 3.8. Thus a feedback mechanism to keep it in the safe-operating limits of the technology is required.
✘ The current drawn from U_{in} is discontinuous, likely causing the need for additional on-chip input decoupling.
✘ Four switches are required, requiring more area than the two switches of a buck converter, for similar conduction losses. These will also cause increased switching losses and a more complex driver.

3.1.4 Buck^2 Converter

The circuit of an ideal buck^2 DC-DC converter is shown in Fig. 3.9 [Mak91]. This converter converts U_{in} to a lower, non-inverted U_{out}. The relation between $k(\delta)$ and δ, for CCM, is given by (3.10), which shows the quadratic dependency. The explanation of the DCM is omitted in this dissertation.

$$k(\delta) = \delta^2 \tag{3.10}$$

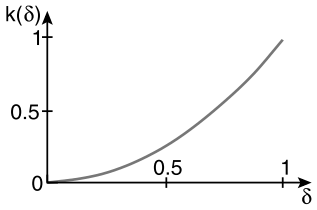

Fig. 3.10 The voltage conversion ratio $k(\delta)$ as a function of the duty-cycle δ, for an ideal buck^2 converter in CCM

The graphical representation of (3.10) is illustrated in Fig. 3.10. The buck^2 converter has an improved performance for low values of (δ), which is equivalent to large differences between the values of U_{in} and U_{out}, compared to a standard buck converter. This is due to the presence of two filters, each consisting of an inductor and capacitor, as opposed to one filter in a standard buck converter.

The operation of the buck^2 converter in CCM consists of the following two phases:

1. *The inductors charge phase* Φ_1: During Φ_1 SW_1 and SW_3 are closed and SW_2 and SW_4 are opened, during a time t_{on}. Both L_1 and L_2 are charged in series with U_{in}. L_2 also receives energy from C_1, thereby discharging C_1. At the output, C_2 is charged and R_L is powered from the current through L_2.
2. *The inductors discharge phase* Φ_2: During Φ_2 SW_2 and SW_4 are closed and SW_1 and SW_3 are opened, during a time t_{off}. L_1 is discharged through C_1, thereby charging C_1. L_2 is discharged through the output, thereby powering R_L through both C_2 and L_2.

In DCM SW_2 and SW_4 are opened when the respective currents through L_2 and L_4 become zero, which does not necessarily occurs simultaneously. This causes the whole converter, or either the part L_1–C_1 or the part L_2–C_2, to be idle for the remaining part of t_{off}.

Table 3.5 lists the results of the SPICE simulations for the ideal buck^2 converter, in order for it to comply with the specifications of Table 3.1. All the parameters are chosen such that the total required capacitance is minimized, with some restrictions. C_1 is chosen to be the smallest possible value, as it has less effect on ΔU_{out} than C_2. However, the capacitance of C_1 is inversely proportional to the voltage swing over SW_3 and SW_4. Thus, its minimum required value is limited such that $U_{SW_3} \leqslant 2 \cdot U_{in}$ and $U_{SW_4} \leqslant 2 \cdot U_{in}$. It can be proven that for the desired specifications of U_{in} and

Table 3.5 The SPICE-simulations results for the required capacitances C_1 and C_2, to comply with the specifications of Table 3.1, of an ideal buck^2 DC-DC converter, for four different output powers P_{out}. The required duty-cycle δ and the CM are also provided

P_{out}	C_1	C_2	$C_{tot} = C_1 + C_2$	δ	$t_{off\_real\_SW2}$	$t_{off\_real\_SW4}$	CM
1 mW	0.0035 nF	0.2 nF	0.2035 nF	3.5%	0.06 ns	0.24 ns	DCM
10 mW	0.035 nF	1.7 nF	1.735 nF	11%	0.22 ns	0.7 ns	DCM
100 mW	0.3 nF	10 nF	10.3 nF	33%	0.55 ns	2.4 ns	DCM
1 W	3 nF	10 nF	13 nF	74%	2.6 ns	2.6 ns	CCM

U_{out}, these values cannot be made significantly smaller. The inductances for L_1 and L_2, which respectively are 3 nH and 7 nH, are chosen such that the required specifications of Table 3.1 are met with the minimal total required capacitance.

From Table 3.5 it can be concluded that the required C_{tot} decreases with decreasing P_{out}. However, the difference between C_{tot} for $P_{out} = 1$ W and $P_{out} = 100$ mW is rather small. This is due to the fact that the converter switches from CCM to DCM. It is also observed that the required capacitance for C_1 is much smaller than for C_2.

Finally, the benefits and drawbacks of the buck[2] converter are:

✔ In CCM L_2 provides a continuous current to the output, relaxing the specifications of C_2.
✔ U_{out} is not inverted and referred to *GND*.
✘ The total required capacitance is quasi the same as for the buck converter.
✘ CCM is only reached at high P_{out}.
✘ Increased complexity, compared to the buck converter, due to four required switches and an additional inductor and capacitor.
✘ The voltage over SW_3 can easily reach $2 \cdot U_{in}$. When assuming that U_{out} is the nominal technology supply voltage, SW_3 would have to be implemented by means of four stacked standard transistors. This will cause increased conduction and switching losses and a will require a more complex driver.
✘ SW_3 does not have a terminal that is connected to a fixed voltage, causing the need for a more complex driver.
✘ The current drawn from U_{in} is discontinuous, likely causing the need for additional on-chip input decoupling.

3.1.5 Watkins-Johnson Converter

The circuit of an ideal Watkins-Johnson DC-DC converter, using one inductor and four switches, is shown in Fig. 3.11(a). The equivalent circuit, using two coupled inductors and two switches, is shown in Fig. 3.11(b). It can be proven that both circuits yield the same functionality, which is decreasing U_{in} or increasing and inverting it. This behavior, $k(\delta)$ as a function of δ, is formally described for CCM by (3.11), which is valid for both the versions of the converter.

$$k(\delta) = \frac{2\delta - 1}{\delta} \tag{3.11}$$

Figure 3.12 shows the plot of (3.11). It is observed that for $0 < \delta < 0.5$ the converter yields an inverting step-up function and that for $0.5 < \delta < 1$ the converter yields a non-inverting step-down function. Therefore, the Watkins-Johnson converter can be regarded as a step-up/down converter. However, the conversion towards negative voltages on-chip has virtually no applications. For this purpose the inverting step-up functionality will be neglected in this work, thereby only considering it as a step-down converter. Moreover, only the topology from Fig. 3.11(a) will

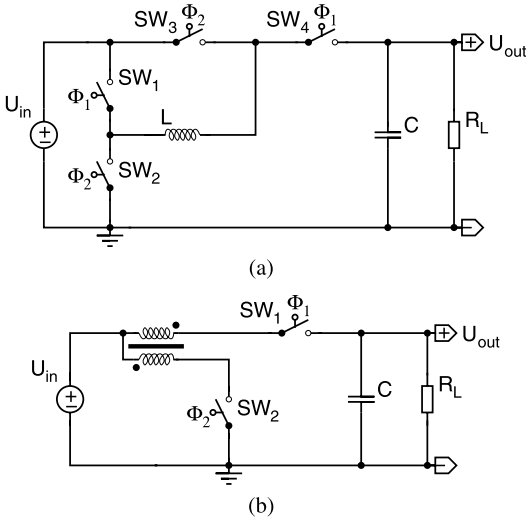

Fig. 3.11 **(a)** The circuit of an ideal Watkins-Johnson DC-DC converter, using an inductor and **(b)** using two coupled inductors

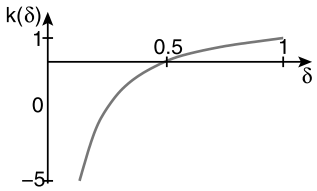

Fig. 3.12 The voltage conversion ratio $k(\delta)$ as a function of the duty-cycle δ, for a Watkins-Johnson converter in CCM

be discussed in this work, as the coupled inductors from the alternative topology would pose a difficulty for the overall comparison of DC-DC step-down converters.

The basic operation of the Watkins-Johnson converter in CCM, with a positive U_{out}, consists of the following two phases:

1. *The inductor charge phase* Φ_1: During Φ_1 SW_1 and SW_4 are closed and SW_2 and SW_3 are opened, during a time t_{on}. L is charged in series with C and R_L through U_{in}, thereby also charging C and providing power to R_L.
2. *The inductor discharge phase* Φ_2: During Φ_2 SW_2 and SW_3 are closed and SW_1 and SW_4 are opened, during a time t_{off}. L is discharged through U_{in} and simultaneously C is discharged through R_L.

In DCM SW_2 and SW_3 are opened at the end of Φ_2, preventing the current through L from becoming negative. This would cause C to be discharged through L and U_{in} during Φ_1. During the time when all the four switches are open the converter is idle.

The results of the SPICE simulations for the ideal Watkins-Johnson converter, in order for it to comply with the specifications of Table 3.1, are listed in Table 3.6. It is observed that at $P_{out} = 1$ W the required capacitance of C is about six times higher compared to the buck converter, in CCM. For low values of P_{out} the required capacitance of C has the same order of magnitude than for a buck converter.

Table 3.6 The SPICE-simulations results for the required capacitance C, to comply with the specifications of Table 3.1, of an ideal DC-DC Watkins-Johnson converter, for four different output powers P_{out}. The required duty-cycle δ and the CM are also provided

P_{out}	C	δ	t_{off_real}	CM
1 mW	0.19 nF	4.4%	0.22 ns	DCM
10 mW	1.7 nF	14%	0.7 ns	DCM
100 mW	12 nF	44.4%	2.22 ns	DCM
1 W	66 nF	66.6%	3.34 ns	CCM

To conclude the discussion on the ideal Watkins-Johnson DC-DC converter the possible benefits and drawbacks of this converter are provided:

✔ The four switches have one terminal which is connected to a fixed potential: SW_1 and SW_3 to U_{in}, SW_2 to GND and SW_4 to U_{out}. This simplifies the drivers of these switches.
✔ The output is not inverted and referred to the GND potential of the converter.
✘ In neither one of the CMs a continuous current is delivered to C and R_L. Thus, the parasitic ESL and ESR will cause ΔU_{out} to increase in real converters, putting more stringent specifications on C.
✘ In neither one of the CMs a continuous current is drawn from U_{in}. Moreover, the current through U_{in} is reversed in polarity, between Φ_1 and Φ_2. During Φ_2 current is fed into U_{in}, which is likely not to be allowed in the majority of applications. Therefore an on-chip decouple capacitor with a large capacitance will be required to cope with this current.
✘ The converter requires four switches. Compared to a buck converter, this implies that the driver logic will be more complex, the conduction and switch losses will increase and the required area will increase.
✘ At high P_{in} the converter requires a larger output capacitance C, compared to a buck converter.

3.1.6 Step-Down Converter Summary

The most significant properties and parameters of the five discussed step-down DC-DC converters topologies are summarized in Table 3.7. It is observed that the buck converter requires the smallest number of components: one inductor, one capacitor and two switches. Because it only uses two switches, it has the potential to achieve the highest power conversion efficiency, since these switches cause conduction and switching losses. This is especially the case for monolithic DC-DC converters, due to their high switching frequencies. These losses will be explained more into detail in Chap. 4, where an accurate model is proposed which takes all the significant losses into account. It can also be seen that none of the converter topologies provides a continuous current to the output filter in DCM, implying that more stringent

Table 3.7 The comparison of key properties and parameters of five types of step-down DC-DC converters, with respect to monolithic integration (✔ = yes, ✘ = no)

	Buck	Bridge	3-Level buck	Buck^2	Watkins-Johnson
# Switches	2	4	4	4	2–4
# Capacitors	1	1	2	2	1
# Inductors	1	1	1	2	1
Floating switches	✘	✘	✔	✔	✘
Inverted output	✘	✘	✘	✘	✘
Floating output	✘	✔	✘	✘	✘
Complex timing	✘	✘	✔	✔	✘
Continuous I_{out}	CCM	CCM	CCM	CCM	✘
Continuous I_{in}	✘	✘	✘	✘	✘
C_{tot} @ $P_{out} = 1$ mW	0.19 nF	0.19 nF	0.36 nF	0.2035 nF	0.19 nF
C_{tot} @ $P_{out} = 10$ mW	1.6 nF	1.69 nF	0.66 nF	1.735 nF	1.7 nF
C_{tot} @ $P_{out} = 100$ mW	9.5 nF	11.5 nF	5 nF	10.3 nF	12 nF
C_{tot} @ $P_{out} = 1$ W	12.5 nF	19 nF	50 nF	13 nF	66 nF

specifications will have to be set to the output filter. The comparison does not account for on-chip input decoupling, which is potentially necessary as none of the converter topologies draws a continuous supply current.

Figure 3.13 shows the required C_{tot} as a function of P_{out} for each of the five step-down DC-DC converter topologies, such that these converters meet the specifications of Table 3.1. In this comparison the buck converter also proves to be the best choice for monolithic integration for $P_{out} > 1$ W, where it requires the lowest C_{tot}. The buck^2 is the second best choice at high values of P_{out}, as its required amount of C_{tot} does not differ much from the buck converter. However, the buck^2 needs two additional switches. For $P_{out} < 100$ mW the required C_{tot} does not differ significantly amongst the converter topologies, except for the three-level buck converter. The latter converter requires about 50% less total capacitance than its counterparts, for low values of P_{out}. However, it requires four switches and also a quite complex timing scheme.

The emphasis of this work is on maximizing P_{out}, minimizing the total required area and maximizing η_{SW}. Therefore, the buck converter, and its variants, will be the converter of choice for the realizations in this work. The possible variations of this converter will be explained in Sects. 3.5.1 and 3.5.2.

3.2 Step-Up Converters

Inductive DC-DC step-up converters are used to convert the input voltage U_{in} to a higher output voltage U_{out}. The application principle of DC-DC step-up converters in battery-operated systems is explained in Sect. 1.2.2. In this section three different

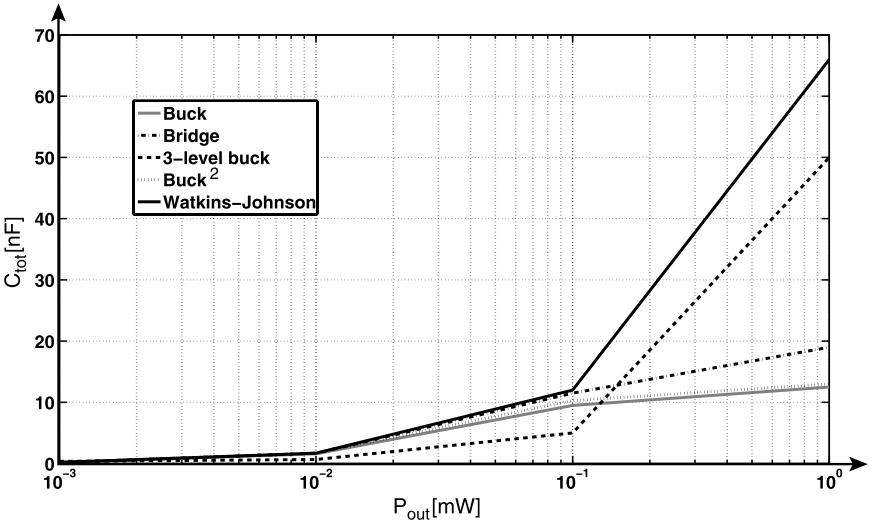

Fig. 3.13 The total required capacitance C_{tot} of five step-down DC-DC converter topologies as a function of the output power P_{out}. These values are obtained by means of SPICE-simulations, such that the five converters meet with the specifications of Table 3.1

ideal inductive DC-DC step-up converter topologies, are discussed and compared with one another. This is done in view of monolithic integration, where the occupied area of the converter is a crucial parameter that is to be minimized for cost-reasons. The topologies explained in this section are:

- The boost converter
- The current-fed bridge converter
- The inverse Watkins-Johnson converter

The comparison of DC-DC step-up converters will be performed analogue to the comparison of DC-DC step-down converters, by means of ΔU_{out}, as explained in Sect. 3.1. For this purpose, the different converter topologies are designed to meet with the specifications of Table 3.8, yielding the total required capacitance. The values of Table 3.8 are chosen in such a way that they are in the same order of magnitude as the values used in real implementations, which are discussed in Chap. 6.

The calculations for this comparison are executed through SPICE simulations only, except for the boost converter for which the calculations are also performed by means of the small-ripple approximation, charge balance and volt-second balance, which are discussed in Sect. 2.3.3. This allows for validating these calculation methods through simulations. These simulations and calculations will allow for an area-driven comparison, which is mandatory for monolithic integration. However, the required area is not the sole property that needs to be taken into account when choosing a topology. Therefore, a brief circuit-level discussion is also given for each converter topology.

Table 3.8 The input and output parameters, together with their values, used to compare different DC-DC step-up converter topologies

Input/output parameter	Value
Input voltage U_{in}	1 V
Output voltage U_{out}	2 V
Output voltage ripple ΔU_{out}	100 mV
Total inductance L_{tot}	10 nH
Switching frequency f_{SW}	100 MHz
Output power 1 P_{out_1}	1 mW
Load resistance 1 R_{L_1}	4 kΩ
Output power 2 P_{out_2}	10 mW
Load resistance 2 R_{L_2}	400 Ω
Output power 3 P_{out_3}	100 mW
Load resistance 3 R_{L_3}	40 Ω
Output power 4 P_{out_4}	1 W
Load resistance 4 R_{L_4}	4 Ω

3.2.1 Boost Converter

The circuit of an ideal boost DC-DC converter is shown in Fig. 2.18. The basic operation of this converter is already discussed as an example for calculation methods, in Sect. 2.3.3. These calculation methods where used to deduce $k(\delta)$ for continuous (2.62) and DCM (2.72) and also ΔU_{out} for continuous (2.65) and DCM (2.74).

The results of the SPICE simulations for the ideal boost converter, in order for it to comply with the specifications of Table 3.8, are listed in Table 3.9. It can be seen that the required capacitance of C in CCM is proportionally much larger than in DCM. This is due to the fact that the output filter solely consists of C and that the current delivered to the output is discontinuous. This discontinuous current causes large current transients at the transitions between Φ_1 and Φ_2. It is also observed that the converter only works in CCM at high values of P_{out}.

The discussion on the ideal DC-DC boost converter is concluded with its possible benefits and drawbacks for monolithic integration:

✔ Both switches have one terminal that is connected to a fixed potential: SW_1 to GND and SW_2 to U_{out}. This simplifies the drivers of the switches.

Table 3.9 The SPICE simulations results for the required capacitance C, to comply with the specifications of Table 3.8, of an ideal DC-DC boost converter, for four different output powers P_{out}. The required duty-cycle δ and the CM are also provided

P_{out}	C	δ	t_{off_real}	CM
1 mW	0.048 nF	3.15%	0.315 ns	DCM
10 mW	0.45 nF	10%	1 ns	DCM
100 mW	3.4 nF	31.5%	3.15 ns	DCM
1 W	25 nF	50%	5 ns	CCM

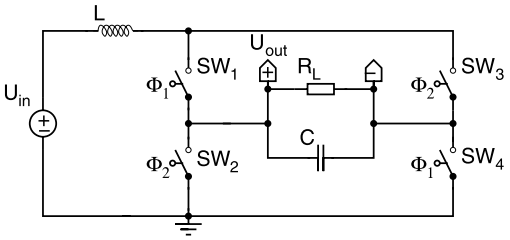

Fig. 3.14 The circuit of an ideal current-fed bridge DC-DC converter

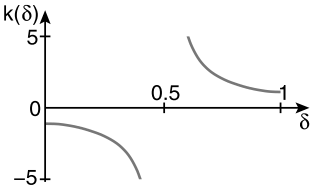

Fig. 3.15 The voltage conversion ratio $k(\delta)$ as a function of the duty-cycle δ, for a current-fed bridge converter in CCM

✔ This converter uses only one inductor and capacitor, which can be beneficial for its area requirement.
✔ In CCM the converter draws a continuous current from U_{in}, this relaxes the specifications for a potential on-chip decouple capacitor.
✔ The converter delivers a non-inverted U_{out}, referred to *GND* of the circuit.
✘ The current delivered to the output filter is always discontinuous, putting more stringent specifications to the output capacitor C.

3.2.2 Current-Fed Bridge Converter

The circuit of an ideal current-fed bridge DC-DC converter is shown in Fig. 3.14 [Sev79]. This converter is capable of converting U_{in} into a certain U_{out} of which the absolute value is equal or higher than U_{in}. This is formally confirmed for CCM by (3.12), which gives $k(\delta)$.

$$k(\delta) = \frac{1}{2\delta - 1} \tag{3.12}$$

The graphical representation of (3.12) is illustrated in Fig. 3.15, where $k(\delta)$ is plotted as a function of δ. The value of $k(\delta)$ is negative for $0 < \delta < 0.5$ and positive for $0.5 < \delta < 1$, in CCM. This discussion will only consider the latter case, because the generation of on-chip negative voltages is rarely used in practice.

The basic operation of the current-fed bridge converter in CCM and for positive values of $k(\delta)$, consists of the following two phases:

1. *The inductor discharge phase* Φ_1: During Φ_1 SW_1 and SW_4 are closed and SW_2 and SW_3 are opened, during a time t_{on}. This causes L to be discharged, thereby charging C and providing power to R_L.

Table 3.10 The SPICE simulations results for the required capacitance C, to comply with the specifications of Table 3.8, of an ideal DC-DC current-fed bridge converter, for four different output powers P_{out}. The required duty-cycle δ and the CM are also provided

P_{out}	C	δ	t_{off_real}	CM
1 mW	0.075 nF	3.8%	0.13 ns	DCM
10 mW	0.7 nF	12%	0.42 ns	DCM
100 mW	6.2 nF	39%	1.4 ns	DCM
1 W	37.5 nF	75%	2.5 ns	CCM

2. *The inductor charge phase* Φ_2: During Φ_2 SW_2 and SW_3 are closed and SW_1 and SW_4 are opened, during a time t_{off}. This causes L to be charged by U_{in}, thereby discharging C into R_L.

In DCM SW_1 and SW_4 are opened when the current through L becomes zero. This prevents the current through L from reversing and discharging C through L and U_{in}.

The results of the SPICE simulations for the ideal current-fed bridge converter, in order for it to comply with the specifications of Table 3.8, are listed in Table 3.10. In contrast to what might be expected from Fig. 3.15, δ does not increase upon decreasing values of R_L in DCM, for the same U_{out}. Furthermore, it is observed that the converter only operates in CCM at high values of P_{out}.

The discussion on the ideal DC-DC current-fed bridge converter is concluded with its possible benefits and drawbacks:

✔ In CCM the converter draws a continuous current from U_{in}, relaxing the specifications of a potential on-chip input decoupling capacitor.
✘ The current delivered by L reverses between Φ_1 and Φ_2, making it discontinuous. This puts more stringent specifications to C.
✘ The converter requires four switches, as opposed to the boost converter which only needs two switches. This will cause an increased area requirement and also increased conduction and switching losses.
✘ SW_1 and SW_3 do not possess a terminal that is connected with a fixed potential. Therefore, the complexity of the drivers for these switches will increase.
✘ The output cannot be referred to *GND*, which is associated with the chip's substrate. This is a drawback for the on-chip load circuits, which are referred to the substrate.
✘ It shows that the current-fed bridge converter requires a higher capacitance for C compared to a boost converter, thus a larger area will be required.

3.2.3 Inverse Watkins-Johnson Converter

The circuit of an ideal inverse Watkins-Johnson converter, implemented with an inductor and four switches, is shown in Fig. 3.16(a). The equivalent circuit of this

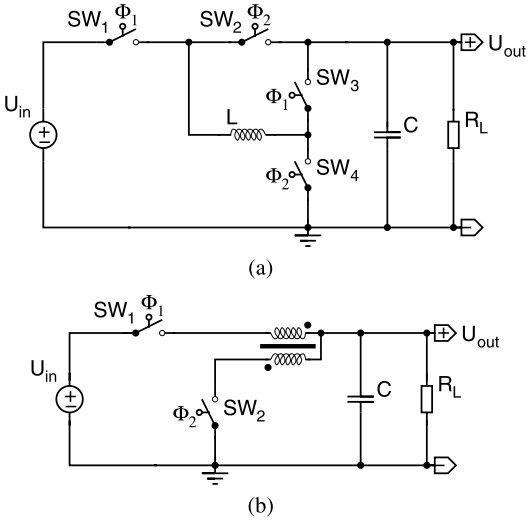

Fig. 3.16 **(a)** The circuit of an ideal inverse Watkins-Johnson DC-DC converter, using an inductor and **(b)** using two coupled inductors

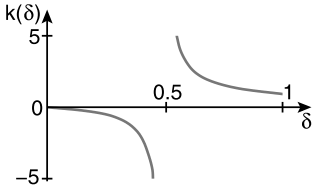

Fig. 3.17 The voltage conversion ratio $k(\delta)$ as a function of the duty-cycle δ, for an inverse Watkins-Johnson converter in CCM

converter, implemented with two coupled inductors and two switches, is shown in Fig. 3.16(b). In order to perform a fair and transparent comparison, only the implementation of Fig. 3.16(a) will be discussed in this work. The inverse Watkins-Johnson converter is capable of converting U_{in} in either a positive U_{out}, larger than U_{in}, or in a negative U_{out}, of which the absolute value can either be lower or higher than U_{in}. As a consequence the inverse Watkins-Johnson converter can be regarded as an inverting step-up/down converter or as a non-inverting step-up converter. In this work the latter case will be discussed. The formal description of $k(\delta)$ for CCM is given by (3.13).

$$k(\delta) = \frac{\delta}{2\delta - 1} \tag{3.13}$$

The graphical representation of (3.13) is illustrated by Fig. 3.17, where $k(\delta)$ is plotted as a function of δ. It shows that $0 < U_{out} < -\infty$ for $0 < \delta < 0.5$ and that $\infty < U_{out} < 1$ for $0.5 < \delta < 1$.

The basic operation of the inverse Watkins-Johnson converter in CCM, with a positive U_{out}, consists of the following two phases:

1. *The inductor discharge phase* Φ_1: During Φ_1 SW_1 and SW_3 are closed and SW_2 and SW_4 are opened, during a time t_{on}. This causes L to be discharged, thereby charging C and providing power to R_L.

Table 3.11 The SPICE simulations results for the required capacitance C, to comply with the specifications of Table 3.8, of an ideal DC-DC inverse Watkins-Johnson converter, for four different output powers P_{out}. The required duty-cycle δ and the CM are also provided

P_{out}	C	δ	t_{off_real}	CM
1 mW	0.01 nF	4.6%	0.24 ns	DCM
10 mW	0.9 nF	14.2%	0.71 ns	DCM
100 mW	8.2 nF	46%	2.3 ns	DCM
1 W	66 nF	66.6%	3.34 ns	CCM

2. *The inductor charge phase* Φ_2: During Φ_2 SW_2 and SW_4 are closed and SW_1 and SW_3 are opened, during a time t_{off}. This causes L to be charged by C, simultaneously C is also discharged into R_L.

In DCM SW_2 and SW_4 are opened when the current through L is zero. This prevents the current through L from becoming negative, which would cause energy from C to be fed back into U_{in}. The converter is idle during this period.

The results of the SPICE simulations, for the converter to comply with the specifications of Table 3.8, are listed in Table 3.11. The required capacitance of C is more than two times larger compared to a boost converter and also significantly larger than for a current-fed bridge converter.

The discussion on the ideal DC-DC inverse Watkins-Johnson converter is concluded with its possible benefits and drawbacks:

✔ Each of the four switches has one of its terminals connected to a fixed potential: SW_1 to U_{in}, SW_2 and SW_3 to U_{out} and SW_4 to GND, simplifying the drivers.
✔ U_{out} is non-inverting and referred to the GND of the converter.
✘ The $i_L(t)$ reverses polarity between Φ_1 and Φ_2, resulting in a discontinuous output current and setting more stringent limits to the specifications of C.
✘ The current drawn from U_{in} is not continuous. Therefore, an on-chip decouple capacitor is likely to be required.
✘ Unlike a boost converter, this converter requires four switches, resulting in an increased area requirement and also increased conduction and switching losses.
✘ This converter requires roughly two times the amount of output capacitance compared to a boost converter.

3.2.4 Step-Up Converter Summary

The most significant properties and parameters of the three discussed DC-DC step-up converter topologies are summarized in Table 3.12. It is observed that all the topologies require only one capacitor and inductor. The boost converter requires the smallest number of components by using only two switches, while the other two converters require four switches. Thus, the boost converter has the potential of achieving the highest power conversion efficiency, since each switch will cause

Table 3.12 The comparison of key properties and parameters of three types of DC-DC step-up converters, with respect to monolithic integration (✔ = yes, ✘ = no)

	Boost	Current-fed bridge	Inverse Watkins-Johnson
# Switches	2	4	4
# Capacitors	1	1	2
# Inductors	1	1	1
Floating switches	✘	✔	✘
Inverted output	✘	✘	✘
Floating output	✘	✔	✘
Complex timing	✘	✘	✘
Continuous I_{out}	✘	✘	✘
Continuous I_{in}	CCM	CCM	✘
C_{tot} @ $P_{out} = 1$ mW	0.048 nF	0.075 nF	0.01 nF
C_{tot} @ $P_{out} = 10$ mW	0.45 nF	0.7 nF	0.9 nF
C_{tot} @ $P_{out} = 100$ mW	3.4 nF	6.2 nF	8.2 nF
C_{tot} @ $P_{out} = 1$ W	25 nF	37.5 nF	66 nF

significant conduction and switching losses. Neither one of the converter topologies provide a continuous current to the output filter, thus putting more stringent specifications to the output capacitor. However, the boost converter, for instance, requires less capacitance than a buck converter in DCM (see Table 3.2), despite the fact that the buck converter delivers no sudden current transients to the output capacitor. This is due to the $U_{out} = 1$ V specification for step-down converters, compared to 2 V for step-up converters. This implies that the output current for the step-up converters is less, for the same P_{out}, relaxing the specifications on the output capacitance. The reason for choosing different specifications for step-down and step-up converters is that they should be closely related to the real implementations of these respective converters, as discussed in Chap. 6. These different specifications also imply that the step-up converters will demand a higher input current, as U_{in} is chosen 1 V, compared to 2 V for the step-down converters. Therefore, when this input current is discontinuous an on-chip decouple capacitor may be required, which is however not taken into account for this comparison. The specifications of this decouple capacitor for the boost converter and the current-fed bridge converter can be relaxed, compared to step-down converters, because their input current never shows steep transients.

Figure 3.18 shows the required C_{tot} is a function of P_{out} for each of the three DC-DC step-up converter topologies, such that these converters meet with the specifications of Table 3.8. It follows that the boost converter requires the smallest capacitance, followed by the current-fed bridge converter and the inverse Watkins-Johnson converter. The amount of required capacitance differs the most at $P_{out} > 10$ mW. For $P_{out} = 1$ mW the inverse Watkins-Johnson converter requires the lowest capacitance, of which the area will be insignificant compared to the two additional switches.

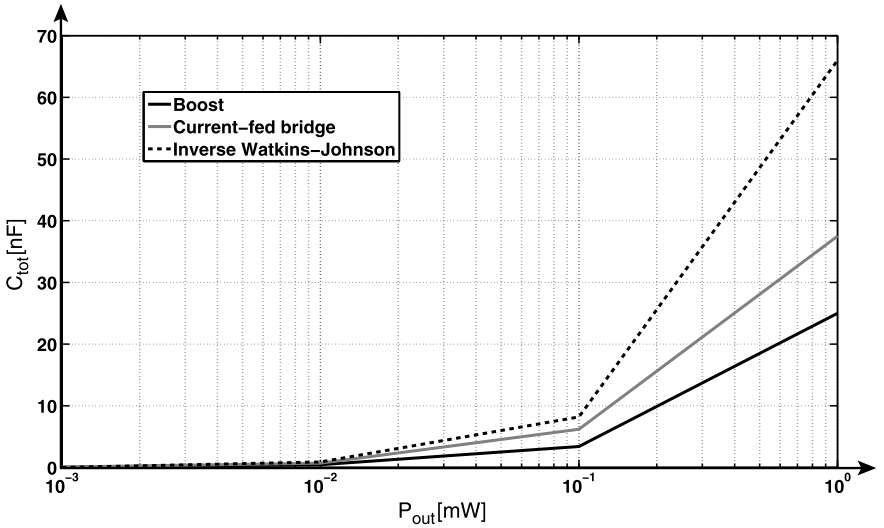

Fig. 3.18 The total required capacitance C_{tot} of three DC-DC step-up converter topologies as a function of the output power P_{out}. These values are obtained by means of SPICE-simulations, such that the three converters meet with the specifications of Table 3.8

As the emphasis of this work is to maximize P_{out}, minimize the required area and maximize η_{SW}, the boost converter is chosen for implementations in this work.

3.3 Step-Up/Down Converters

Inductive DC-DC step-up/down converters are used to convert the input voltage U_{in} to a higher or lower output voltage U_{out}. The application domain for DC-DC step-down converters is mostly situated in battery-operated systems, where the battery voltage is about equal to the required supply voltage of the application. In this section five different ideal inductive DC-DC step-up/down converter topologies are discussed and compared with one another. This is done in view of monolithic integration, where the occupied area of the converter is a crucial parameter that is to be minimized for cost-reasons. The topologies explained in this section are:

- The buck-boost converter
- The non-inverting buck-boost converter
- The Ćuk converter
- The SEPIC converter
- The Zeta converter

The comparison of DC-DC step-up/down converters will be performed analogue to the comparison of DC-DC step-down and step-up converters, by means of ΔU_{out}, as explained in Sect. 3.1. For this purpose, the different converter topologies are

Table 3.13 The input and output parameters, together with their values, used to compare different DC-DC step-up/down converter topologies

Input/output parameter	Value
Input voltage U_{in}	1 V
Output voltage U_{out}	1 V
Output voltage ripple ΔU_{out}	50 mV
Total inductance L_{tot}	10 nH
Switching frequency f_{SW}	100 MHz
Output power 1 P_{out_1}	1 mW
Load resistance 1 R_{L_1}	1 kΩ
Output power 2 P_{out_2}	10 mW
Load resistance 2 R_{L_2}	100 Ω
Output power 3 P_{out_3}	100 mW
Load resistance 3 R_{L_3}	10 Ω
Output power 4 P_{out_4}	1 W
Load resistance 4 R_{L_4}	1 Ω

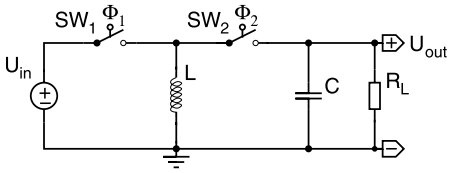

Fig. 3.19 The circuit of an ideal buck-boost DC-DC converter

designed to meet with the specifications of Table 3.13, yielding the total required capacitance C_{tot}. The calculations for this comparison are executed through SPICE simulations, allowing for an area-driven comparison which is mandatory for monolithic integration.

3.3.1 Buck-Boost Converter

The circuit of an ideal buck-boost DC-DC converter is shown in Fig. 3.19. This converter is capable of converting U_{in} into a negative U_{out}, of which the absolute value can either be lower or higher than U_{in}. The mathematical relation between $k(\delta)$ and δ for CCM is given by (3.14).

$$k(\delta) = -\frac{\delta}{1-\delta} \tag{3.14}$$

The graphical representation of $k(\delta)$ as a function of δ is illustrated in Fig. 3.20. It shows that for $0 < \delta < 0.5$, $0 < U_{out} < -1$ and for $0.5 < \delta < 1$, $-1 < U_{out} < -\infty$. Because the on-chip conversion to negative voltages is beyond the scope of this work, the buck-boost converter will not be taken into account for this comparison.

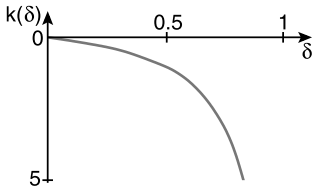

Fig. 3.20 The voltage conversion ratio $k(\delta)$ as a function of the duty-cycle δ, for an ideal buck-boost converter in CCM

3.3.2 Non-inverting Buck-Boost Converter

The circuit of an ideal non-inverting buck-boost DC-DC converter is shown in Fig. 3.21. This converter is capable of converting U_{in} in to a non-inverted U_{out}, which can be either lower or higher than U_{in}. The mathematical relation between $k(\delta)$ and δ for CCM is given by (3.15).

$$k(\delta) = \frac{\delta}{1-\delta} \tag{3.15}$$

The graphical representation of $k(\delta)$ as a function of δ is illustrated in Fig. 3.22. It shows that for $0 < \delta < 0.5$, $0 < U_{out} < 1$ and for $0.5 < \delta < 1$, $1 < U_{out} < \infty$.

The basic operation of the non-inverting buck-boost converter in CCM, with $U_{in} = U_{out}$, consists of the following two phases:

1. *The inductor charge phase* Φ_1: During Φ_1 SW_1 and SW_3 are closed and SW_2 and SW_4 are opened, during a time t_{on}. This causes L to be charged by U_{in} and simultaneously C is discharged through R_L.
2. *The inductor discharge phase* Φ_2: During Φ_2 SW_2 and SW_4 are closed and SW_1 and SW_3 are opened, during a time t_{off}. This causes L to be discharged through C and R_L, thereby providing power to R_L and charging C.

In DCM SW_2 and SW_4 are opened when the current through L becomes zero, during Φ_2. This prevents the current through L from becoming negative, which would cause C to be discharged.

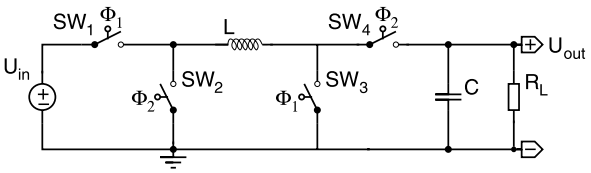

Fig. 3.21 The circuit of an ideal non-inverting buck-boost DC-DC converter

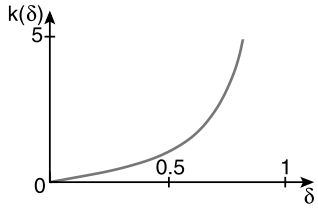

Fig. 3.22 The voltage conversion ratio $k(\delta)$ as a function of the duty-cycle δ, for an ideal non-inverting buck-boost converter in CCM

Table 3.14 The SPICE simulations results for the required capacitance C, to comply with the specifications of Table 3.13, of an ideal DC-DC non-inverting buck-boost converter, for four different output powers P_{out}. The required duty-cycle δ and the CM are also provided

P_{out}	C	δ	t_{off_real}	CM
1 mW	0.19 nF	4.47%	0.447 ns	DCM
10 mW	1.7 nF	14.1%	1.41 ns	DCM
100 mW	12 nF	44.7%	4.47 ns	DCM
1 W	98 nF	50%	5 ns	CCM

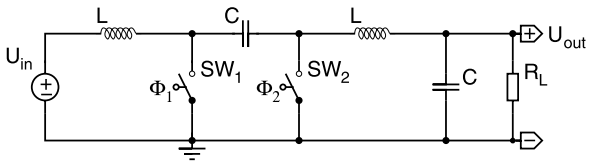

Fig. 3.23 The circuit of an ideal Ćuk DC-DC converter

The results of the SPICE simulations for the ideal non-inverting buck-boost converter, in order for it to comply with the specifications of Table 3.13, are listed in Table 3.14. It is observed that this converter requires a high output capacitance C, especially in CCM, compared to a buck or boost converter. This is due to the fact that the current delivered to the output by L is discontinuous and has a steep transient. This is similar to the boost converter, however as $U_{out} = 1$ V the output current in this case is larger compared to the boost converter, for the same P_{out}.

To conclude the discussion on the ideal DC-DC non-inverting buck-boost converter, a summary of the possible benefits and drawbacks is provided:

✔ The four switches have one terminal connected to a fixed potential: SW_1 to U_{in}, SW_2 and SW_3 to GND and SW_4 to U_{out}, which simplifies the driver circuits.
✔ The output of the converter is non-inverting and referred to GND.
✘ The current delivered by L to the output filter of the converter is always discontinuous, putting more stringent specifications to C.
✘ The current drawn from U_{in} is always discontinuous. Therefore, an on-chip decouple capacitor might be required.

3.3.3 Ćuk Converter

The circuit of an ideal Ćuk DC-DC converter is shown in Fig. 3.23. This converter is used for converting U_{in} into a negative U_{out} of which the absolute value is lower or higher than U_{in}. The mathematical relation between $k(\delta)$ and δ for CCM is identical to that of the buck-boost converter, which is given by (3.14). The graphical representation of (3.14) is illustrated in Fig. 3.20, where $k(\delta)$ is plotted as a function of δ.

The Ćuk converter will not be used for this comparison, as the on-chip conversion to negative voltages is not considered in this work.

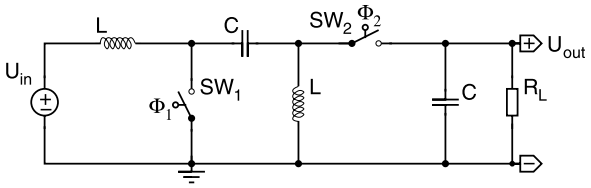

Fig. 3.24 The circuit of an ideal SEPIC DC-DC converter

3.3.4 SEPIC Converter

The circuit of an ideal DC-DC Single-Ended Primary-Inductance Converter (SEPIC) is shown in Fig. 3.24 [Mas77]. The SEPIC converter is capable of converting U_{in} into a non-inverted U_{out}, which has a lower or higher value than U_{in}. For CCM the relation between $k(\delta)$ and δ is identical to that of a non-inverting buck-boost converter, given by (3.15). The graphical representation of (3.15) is illustrated in Fig. 3.22, where $k(\delta)$ is plotted as a function of δ.

The basic operation of the SEPIC converter in CCM, with $U_{in} = U_{out}$, consists of the following two phases:

1. *The inductors charge phase* Φ_1: During Φ_1 SW_1 is closed and SW_2 is opened, during a time t_{on}. This causes L_1 and L_2 to be charged by U_{in} and C_1 respectively, thereby discharging C_1. Simultaneously, C_2 is discharged through R_L.
2. *The inductors discharge phase* Φ_2: During Φ_2 SW_2 is closed and SW_1 is opened, during a time t_{off}. This causes L_1 to discharge, thereby charging C_1 and C_2 and providing power to R_L. L_2 is also discharged, causing C_2 to be charged and R_L to be powered.

In DCM the currents through L_1 and L_2 do not stop flowing and are allowed to change polarity. This is not the case for all the converter topologies discussed until now, where the current through the inductor(s) stops flowing in DCM. In this mode SW_2 is opened at the moment when the currents through L_1 and L_2 are equal and flow towards the output. This prevents C_2 to be discharged through the inductors. When both switches are opened C_2 continues delivering power to R_L. Simultaneously, L_1, L_2, C_1 and U_{in} are series connected, forming a series LC-circuit as described in Sect. 2.3.2.

The results of the SPICE simulations for the ideal SEPIC converter, in order for it to comply with the specifications of Table 3.13, are listed in Table 3.15. All the parameters are chosen such that the total required capacitance is minimized, with the following restriction: the respective voltages over SW_1 and SW_2 are not allowed to rise above $3 \cdot U_{in}$. This restriction is made for the assumption that the converter will be implemented in a technology having U_{in} as nominal supply voltage. Therefore, SW_1 and SW_2 might be realized each by using three standard stacked-transistors, in total requiring six transistors. When comparing with the non-inverting buck-boost converter it can be seen that, when U_{in} is assumed to rise to some extend above the nominal technology voltage, also here six transistors are needed: two for SW_1 and SW_2 and one for SW_3 and SW_4. This restriction sets a lower limit for the capacitance

Table 3.15 The SPICE simulations results for the required capacitances C_1 and C_2, to comply with the specifications of Table 3.13, of an ideal SEPIC DC-DC converter, for four different output powers P_{out}. The required duty-cycle δ and the CM are also provided

P_{out}	C_1	C_2	$C_{tot} = C_1 + C_2$	δ	t_{off_real}	CM
1 mW	0.006 nF	0.19 nF	0.195 nF	2.1%	0.18 ns	DCM
10 mW	0.033 nF	1.8 nF	1.833 nF	7.5%	0.6 ns	DCM
100 mW	0.37 nF	16.5 nF	16.87 nF	25.5%	1.95 ns	DCM
1 W	2.5 nF	105 nF	107.5 nF	52.5%	4.75 ns	CCM

of C_1. The capacitance of C_2, on the other hand, is dominant for the value of ΔU_{out}. The inductances of L_1 and L_2 are respectively 3 nH and 7 nH. These values are chosen such that the total required capacitance C_{tot} is minimized.

From Table 3.15 it is concluded that the required C_{tot} is higher compared to a non-inverting buck-boost converter. This becomes more significant for high values of P_{out}.

To conclude the discussion on the ideal SEPIC DC-DC converter, a summary of the possible benefits and drawbacks is provided:

✔ The two switches each have one terminal connected to a fixed potential: SW_1 to *GND* and SW_2 to U_{out}. This simplifies the driver circuits for these switches.
✔ In CCM the input current is continuous, relaxing the specifications of the input decouple capacitor. In DCM the input current is also continuous, but it has a varying polarity. Thus, energy will be exchanged with U_{in}. However, as U_{in} may not be able to receive energy, the on-chip decouple capacitor should be dimensioned large enough to cope with this.
✔ The output is non-inverted and referred to the *GND* of the converter.
✘ The current delivered to the output filter is not continuous in neither CM, putting more stringent specifications to the output capacitor C_2.
✘ The total required capacitance C_{tot} is higher compared to a non-inverting buck-boost converter.
✘ In DCM two current-sensing is required for L_1 and L_2 in order to determine when the currents through L_1 and L_2 are equal.

3.3.5 Zeta Converter

The circuit of an ideal zeta[3] DC-DC converter is shown in Fig. 3.25. The zeta converter is capable of converting U_{in} into a non-inverted U_{out}, having either a lower or higher value than U_{in}. For CCM the relation between $k(\delta)$ and δ is given by (3.15), as it is equal to that of a non-inverting buck-boost converter. The graphical representation of (3.15) is shown in Fig. 3.22, where $k(\delta)$ is plotted as a function of δ.

[3]This converter is also referred to as inverse-SEPIC converter.

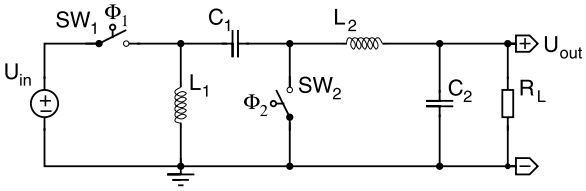

Fig. 3.25 The circuit of an ideal zeta DC-DC converter

The basic operation of the zeta converter in CCM, with $U_{in} = U_{out}$, consists of the following two phases:

1. *The inductors charge phase* Φ_1: During Φ_1 SW_1 is closed and SW_2 is opened, during a time t_{on}. This causes L_1 and L_2 to be charged by U_{in} and C_1 respectively, thereby discharging C_1. Simultaneously, C_2 is charged and R_L is powered by U_{in} and C_1.
2. *The inductors discharge phase* Φ_2: During Φ_2 SW_2 is closed and SW_1 is opened, during a time t_{off}. This causes L_1 to discharge, thereby charging C_1. Simultaneously, L_2 and C_2 are also discharged, powering R_L.

In DCM the currents through L_1 and L_2 do not stop flowing and are allowed to change polarity, analogue to the SEPIC converter. In this CM SW_2 is opened at the moment when the currents through L_1 and L_2 are equal and flow towards the output. This prevents C_2 to be discharged through L_2. When both switches are opened C_2 continues to deliver power to R_L. At the same time L_1, L_2, C_1 and C_2 are connected in series, forming an ideal series LC-circuit as described in Sect. 2.3.2. In this LC-circuit a continuous exchange of energy takes place until the next switch cycle commences.

The results of the SPICE simulations for the ideal SEPIC converter, in order for it to comply with the specifications of Table 3.13, are listed in Table 3.16. All the parameters are chosen such that the total required capacitance is minimized, with the following restriction: the respective voltages over SW_1 and SW_2 are not allowed to rise above $3 \cdot U_{in}$. This restriction is made for the assumption that the converter will be implemented in a technology having U_{in} as nominal supply voltage. Therefore, SW_1 and SW_2 might be realized each by using three standard stacked-transistors, in total requiring six transistors. When comparing with the non-inverting buck-boost converter it can be seen that, when U_{in} is assumed to rise to some extend above the nominal technology voltage, also here six transistors are needed: two for SW_1 and SW_2 and one for SW_3 and SW_4. This restriction sets a lower limit for the capacitance of C_1. The capacitance of C_2 on the other hand is dominant for the value of ΔU_{out}. The inductances of L_1 and L_2 are respectively 3 nH and 7 nH. These values are chosen such that the total required capacitance C_{tot} is minimized.

From Table 3.16 it can be concluded that the required C_{tot} is about five times lower compared to a non-inverting buck-boost converter and a SEPIC converter, for $P_{out} = 1$ W. The reason for this fact is that a constant current is being delivered to the output, as the converter operates in CCM. For lower P_{out} the required C_{tot} is in the same order of magnitude compared to a non-inverting buck-boost converter

Table 3.16 The SPICE simulations results for the required capacitances C_1 and C_2, to comply with the specifications of Table 3.13, of an ideal zeta DC-DC converter, for four different output powers P_{out}. The required duty-cycle δ and the CM are also provided

P_{out}	C_1	C_2	$C_{tot} = C_1 + C_2$	δ	t_{off_real}	CM
1 mW	0.006 nF	0.26 nF	0.266 nF	2.15%	0.18 ns	DCM
10 mW	0.033 nF	2.8 nF	2.833 nF	7.7%	0.6 ns	DCM
100 mW	0.37 nF	14 nF	14.37 nF	26%	1.95 ns	DCM
1 W	2.5 nF	19.5 nF	22 nF	52.5%	4.75 ns	CCM

and a SEPIC converter. This is due to the fact that despite the current delivered to the output is still continuous, it can change polarity because the converter works in DCM at lower values of P_{out}.

To conclude the discussion on the ideal DC-DC zeta converter, a summary of the possible benefits and drawbacks is provided:

✔ Each of the two switches each has one terminal connected to a fixed potential: SW_1 to U_{in} and SW_2 to *GND*. This simplifies the driver circuits for these switches.
✔ The current delivered to the output is continuous in both CMs, relaxing the specifications for the output capacitor C_2.
✔ The output is non-inverted and referred to the *GND* of the circuit.
✔ The total required capacitance C_{tot} is roughly five times less compared to a non-inverting buck-boost converter and SEPIC converter, for $P_{out} = 1$ W. This yields a huge area reduction for high values of P_{out}.
✘ The input current is discontinuous in both CMs, putting more stringent specifications to the on-chip input decoupling.
✘ In DCM current-sensing is required for L_1 and L_2, to determine when these currents are equal.

3.3.6 Step-Up/Down Converter Summary

Table 3.17 summarizes the most significant properties and parameters of the five discussed DC-DC step-up/down converter topologies. No simulation data of C_{tot} is provided for the buck-boost converter and Ćuk converter, because of the fact that they produce an inverted U_{out}. They are added to Table 3.17 for sake of completeness and are no longer considered in this comparison. The first trade-off to be made is the number of components: a non-inverting buck-boost converter requires four switches, one capacitor and one inductor, whereas the SEPIC converter and zeta converter require two switches, two capacitors and two inductors. In terms of the conduction and switching losses caused by the switches, this puts the potentially highest power conversion efficiency advantage at the SEPIC converter and the zeta converter. However, the SPICE-simulations are performed such that the maximal allowable voltage over the switches of the SEPIC converter and zeta converter is

Table 3.17 The comparison of key properties and parameters of five types of step-down DC-DC converters, with respect to monolithic integration (✔ = yes, ✘ = no)

	Buck-boost	Non-inv. buck-boost	Ćuk	SEPIC	Zeta
# Switches	2	4	2	2	2
# Capacitors	1	1	2	2	2
# Inductors	1	1	2	2	2
Floating switches	✘	✘	✘	✘	✘
Inverted output	✔	✘	✔	✘	✘
Floating output	✘	✘	✘	✘	✘
Complex timing	✘	✘	✔	✔	✔
Continuous I_{out}	✘	✘	✔	✘	✔
Continuous I_{in}	✘	✘	✔	✔	✘
C_{tot} @ $P_{out} = 1$ mW	–	0.19 nF	–	0.195 nF	0.266 nF
C_{tot} @ $P_{out} = 10$ mW	–	1.7 nF	–	1.833 nF	2.833 nF
C_{tot} @ $P_{out} = 100$ mW	–	12 nF	–	16.87 nF	14.37 nF
C_{tot} @ $P_{out} = 1$ W	–	98 nF	–	107.5 nF	22 nF

$3 \cdot U_{in}$. It is also assumed that the nominal technology supply voltage equals U_{in}, implying that a total of six transistors is required to implement these switches. This is the same amount needed for the non-inverting buck-boost converter. Therefore, it can be concluded that, as a first-order approximation, the conduction and switching losses will be similar for the three converter topologies. A drawback for the SEPIC converter and zeta converter is that they require current-sensing for both inductors in DCM, implying more complex timing and control circuitry. Finally, it is observed that the non-inverting buck-boost converter does not provide a continuous current at either the input or the output. In contrast, the SEPIC converter has a continuous input current and the zeta converter a continuous output current, implying that either the input decoupling capacitor or the output filter capacitor of these converters can have relaxed specifications.

The required C_{tot} as a function of P_{out}, for the non-inverting buck-boost converter, the SEPIC converter and the zeta converter in order to comply with the specifications of Table 3.13, is plotted in Fig. 3.26. It is readily observed that the zeta converter has the advantage for $P_{out} > 100$ mW, reaching up to a factor five at $P_{out} = 1$ W. At lower values of P_{out} the non-inverting buck-boost converter is advantageous. However, it does not provide a continuous input current, as does the SEPIC converter. When taking the associated input decouple capacitor into account this advantage may be lost.

The practical implementations of this work, discussed in Chap. 6, do not comprise step-up/down converters. At the time of writing (Q4 2010), this type of monolithic DC-DC converter has not been demonstrated in the literature.

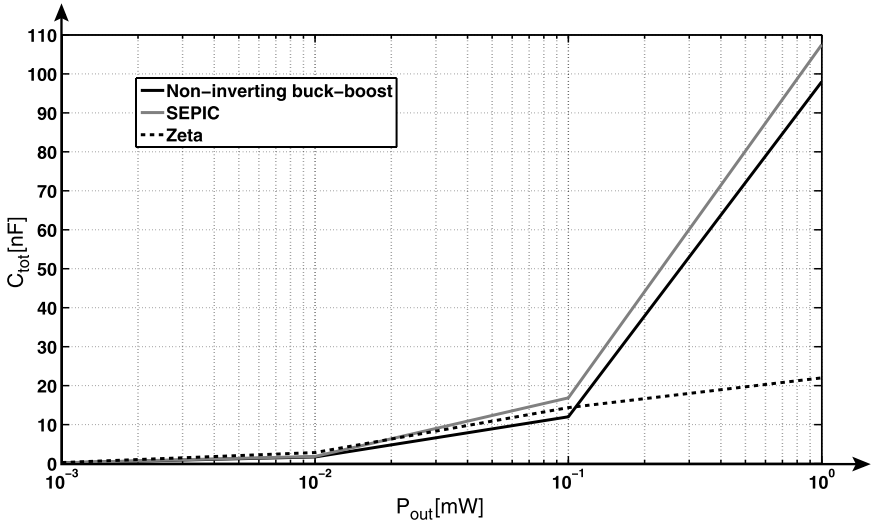

Fig. 3.26 The total required capacitance C_{tot} of three DC-DC step-up/down converter topologies as a function of the output power P_{out}. These values are obtained by means of SPICE-simulations, such that the three converters meet with the specifications of Table 3.13

3.4 Other Types of Inductive DC-DC Converters

From the primary classes of non-galvanically separated DC-DC converters, which are discussed in the respective Sects. 3.1, 3.2 and 3.3, two secondary classes of DC-DC converters can be derived. These are namely the galvanically separated DC-DC converters and the resonant DC-DC converters, of which a selection of commonly used circuit topologies is discussed in Sects. 3.4.1 and 3.4.2, respectively.

None of these DC-DC converter types have been practically realized in this work. Therefore, they will be subject to a brief discussion, giving the designer a sense of their potential for monolithic integration. A more general and conservative discussion on these converters can be found in [Eri04].

3.4.1 Galvanic Separated Converters

Galvanically separated DC-DC converters acquire a transformer to achieve galvanic[4] separation between the in- and output of the converter. This galvanic separation is required in most mains-operated[5] applications, as explained in Sect. 1.2.1, for the sake of safety.

[4]Named after the discoverer of galvanic electricity Luigi Galvani (1737–1798).

[5]For this purpose these converters are preceded by a (full-bridge) rectifier and smoothing capacitor.

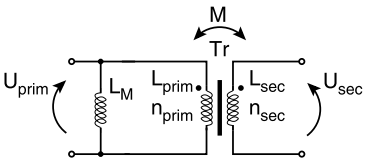

Fig. 3.27 The model of an ideal transformer *Tr*, together with its magnetizing inductance L_M

The calculation methods explained in Sect. 2.3.3 remain valid for galvanically separated DC-DC converters, providing the ideal model for a transformer is used. This model is shown in Fig. 3.27 and it consists of an ideal[6] transformer *Tr*, with n_{prim} and n_{sec} the respective number of primary and secondary winding turns, and a magnetizing inductance L_M. For the steady-state calculations L_M should comply with the volt-second balance and *Tr* merely converts the voltage over the primary winding U_{prim} into the secondary winding voltage U_{sec}. When assuming *Tr* to be ideal, this is done with the factor determined by the winding turn ratio n_{Tr}, as given by (3.16) and where L_{prim} and L_{sec} denote the respective inductances for the primary and the secondary winding.

$$U_{sec} = U_{prim} n_{Tr}|_{k_M=1} = U_{prim} \frac{n_{sec}}{n_{prim}}\bigg|_{k_M=1} = U_{prim} \sqrt{\frac{L_{sec}}{L_{prim}}}\bigg|_{k_M=1} \tag{3.16}$$

Monolithic transformers are feasible and can achieve fairly high magnetic coupling factors k_M in the order of 0.8–0.95 [Bio06]. k_M is calculated by (3.17), where M is the mutual inductance. The power conversion efficiency η_{Tr} of an ideal transformer, having no conduction or core losses, is proportional to k_M.

$$k_M = \frac{M}{\sqrt{L_{prim} L_{sec}}} \quad \text{with} \quad 0 \leqslant k_M \leqslant 1 \tag{3.17}$$

In the following sections a brief discussion is provided on some widely used galvanic separated DC-DC converter topologies, which are all derived from the primary class of DC-DC converters.

Derived Step-Down Converters

The circuit of an ideal forward DC-DC converter is shown in Fig. 3.30. It is derived from the buck converter, which is discussed in Sect. 3.1.1. The relation between $k(\delta)$ and δ for CCM is equal to that of the buck converter, given by (3.1), multiplied by ratio of the number of turns of the third and the first winding n_3/n_1, as stated in (3.22). The number of turns of the first and second winding are commonly made equal $n_1 = n_2$, limiting the maximal value of δ to 50%.

[6] A transformer is ideal when: $k_M = 1$ and $L_{prim}, L_{sec} \to \infty$.

☮ON COUPLED INDUCTORS

Figures 3.28(a) and (b) show the circuits for calculating the energy transfer of coupled inductors *Tr*, in the Laplace-domain. $i_{prim}(t)$ and $i_{sec}(t)$ are given by (3.18) and (3.19). The energy conversion efficiency $\eta_{Tr}(t)$ of *Tr* is given by (3.20). The steady-state energy E_{R_2} delivered to R_2 is given by (3.21).

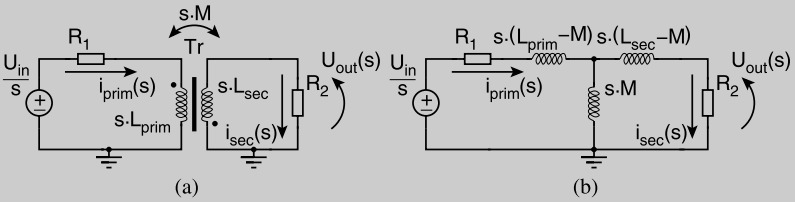

Fig. 3.28 **(a)** The circuit for calculating the energy transfer of *Tr* and **(b)** the equivalent T-circuit, both in the Laplace-domain

$$i_{prim}(s) = \frac{R_2 U_{in} + L_{sec} U_{in} s}{R_1 R_2 s + (L_{sec} R_1 + L_{prim} R_2) s^2 + (L_{prim} L_{sec} - M^2) s^3}$$

$$\Longrightarrow \quad i_{prim}(t) = \mathfrak{L}^{-1} i_{prim}(s) \tag{3.18}$$

$$i_{sec}(s) = \frac{M U_{in}}{R_1 R_2 + (L_{sec} R_1 + L_{prim} R_2) s + (L_{prim} L_{sec} - M^2) s^2}$$

$$\Longrightarrow \quad i_{sec}(t) = \mathfrak{L}^{-1} i_{sec}(s) \tag{3.19}$$

$$\eta_{Tr}(t) = \frac{E_{R_2}(t)}{E_{U_{in}}(t)} = \frac{\int_0^t U_{out}(t) i_{sec}(t)\, dt}{\int_0^t U_{in}(t) i_{prim}(t)\, dt} \tag{3.20}$$

$$E_{R_2} = \lim_{t \to \infty} \left(E_{R_2}(t) \right) = \frac{U_{in}^2}{R_1} \frac{M^2}{2(L_{sec} R_1 + L_{prim} R_2)} \tag{3.21}$$

$$k(\delta) = \frac{n_3}{n_1} \delta \quad \text{with} \quad \delta \leqslant \frac{1}{1 + \frac{n_2}{n_1}} \tag{3.22}$$

This converter is not particularly well suited for monolithic integration because of the fact that the transformer *Tr* requires three windings. This limits the number of metals-layers to be used in parallel for one winding, or it requires for the use of metals which are more close to the substrate. In this way the parasitic winding resistance and/or the parasitic substrate capacitance is increased, implying higher losses. In addition an inductor *L* is required at the output, increasing the area requirement of the converter causing additional losses.

Another galvanic separated variant of the buck converter is the full-bridge buck converter, of which the ideal circuit is shown in Fig. 3.31. The relation between $k(\delta)$ and δ in CCM is equal to that of the buck converter multiplied by n_{Tr}, as given by (3.23).

$$k(\delta) = n_{Tr} \delta \tag{3.23}$$

☮ON COUPLED INDUCTORS (CONTINUED)

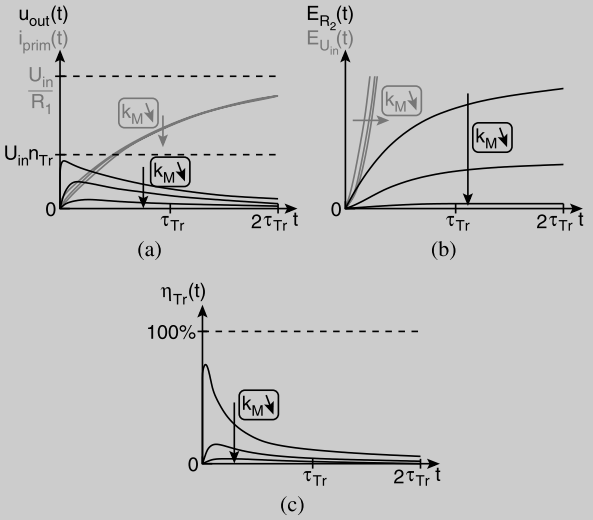

Fig. 3.29 **(a)** $i_{prim}(t)$ and $u_{out}(t)$, **(b)** $E_{U_{in}}(t)$ and $E_{R_2}(t)$ and **(c)** $\eta_{Tr}(t)$ as a function of time t, different values of coupling factor k_M

Figure 3.29(a) shows that $i_{prim}(t)$ roughly equal to (2.36), with $\tau_{Tr} = L_{prim}/R_1$. The maximal $u_{out}(t)$ occurs sooner and becomes larger for increasing k_M and is zero in steady-state. Figure 3.29(b) shows that $E_{U_{in}}(t)$ increases towards ∞, as i_{prim} keeps flowing. In steady-state $E_{R_2}(t)$ is defined by (3.21), which is proportional to k_M. Figure 3.29(c) shows that the maximum of $\eta_{Tr}(t)$ occurs sooner and becomes larger for higher values of k_M. Thus the primary winding of Tr should be disconnected from U_{in} at a certain fixed point in time, for obtaining the maximal $\eta_{Tr}(t)$.

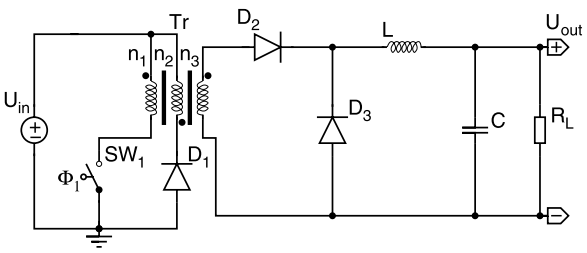

Fig. 3.30 The circuit of an ideal forward DC-DC converter

This converter exhibits a number of variants such as the half-bridge implementation, where SW_3 and SW_4 are replaced by capacitors, eliminating the need for D_3 and D_4. In this case a factor 0.5 is to be added in (3.23), as the voltage swing over the primary winding is only half of that of a full-bridge converter. The output recti-

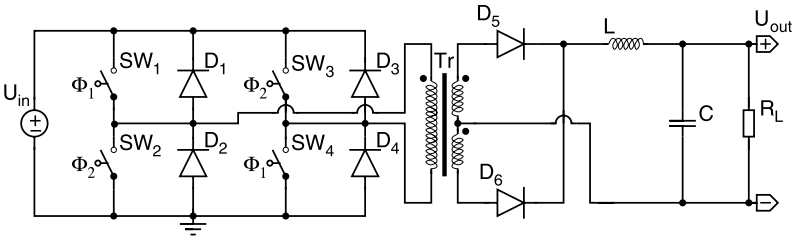

Fig. 3.31 The circuit of an ideal full-bridge buck DC-DC converter

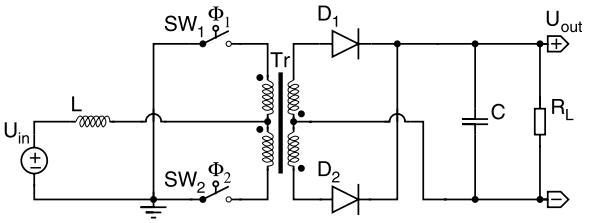

Fig. 3.32 The circuit of an ideal push-pull boost DC-DC converter

fier may also be implemented as a full-bridge rectifier, eliminating the need for the center-tapped secondary winding.

Due to the simplified transformer, compared to the forward converter, this converter has a better prospect towards monolithic integration. This is confirmed by [Del09], where a full-bridge variant with active full-bridge output rectification is implemented as a micro-converter. This micro-converter is only partly integrated on-chip and uses many non-standard techniques for passive integration such as: trench capacitors on silicon and micro-inductors/transformers with micro-machined magnetic cores.

Derived Step-Up Converters

The circuit of an ideal push-pull boost DC-DC converter is shown in Fig. 3.32. It is derived from the boost converter, which is discussed in Sect. 3.2.1. The relation between $k(\delta)$ and δ for CCM is equal to that of the boost converter, given by (2.62), multiplied by n_{Tr}, as stated by (3.24).

$$k(\delta) = n_{Tr} \frac{1}{1-\delta} \tag{3.24}$$

Similar to the full-bridge converter this converter has potential towards monolithic integration. However, no practical monolithic implementations have yet been reported in the literature.

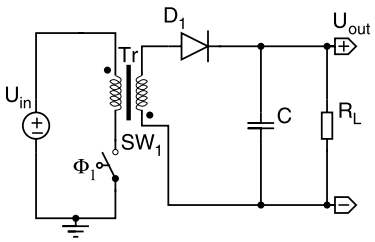

Fig. 3.33 The circuit of an ideal flyback DC-DC converter

Derived Step-Up/Down Converters

The galvanic separated variant of the buck-boost converter, discussed in Sect. 3.3.1, is the flyback DC-DC converter of which the ideal circuit is shown in Fig. 3.33. The relation between $k(\delta)$ and δ for CCM is equal to that of a buck-boost converter multiplied by n_{Tr}. The inverting property of the buck-boost converter can obviously be chosen by altering the direction of the windings relative to one another.

$$k(\delta) = n_{Tr}\frac{\delta}{1-\delta} \tag{3.25}$$

This converter has the simplest topology of the galvanic separated inductive DC-DC converters, only requiring one primary switch and one secondary rectifier (diode). The transformer is also very basic, as it does not require center-tapped windings. Also, the additional in/output inductor, acquired in the previously discussed galvanic separated converters, can be omitted in this converter. For these reasons the flyback converter proves to be suited for monolithic integration, which is confirmed by the practical realization of [Sav03]. However, this implementation suffers a relatively low power density of 50 mW/mm^2 and a low power conversion efficiency of 16.2%. The bottleneck of this type of converter is the parasitic series resistance of the air-core transformer's windings, which accounts for 40% of the total power losses of the converter.

3.4.2 Resonant DC-DC Converters

Figure 3.34 shows the circuit of an ideal series resonant DC-DC converter. This converter consists of a switch-network, formed by SW_1, SW_2, SW_3 and SW_4, to generate a square wave AC voltage. This AC voltage is fed into a series resonant LC-network, formed by L and C_1, whereafter it is fed into a full-bridge rectifier, formed by D_1, D_2, D_3 and D_4. The DC output voltage of the rectifier is filtered by output capacitor C_1 and is also the output voltage U_{out} of the converter. The voltage conversion ratio $k(f_{SW})$ of this converter is calculated by means of the transfer function $\|H(f_{SW})\|$ between the in- and output, which is given by (3.26) [Eri04].

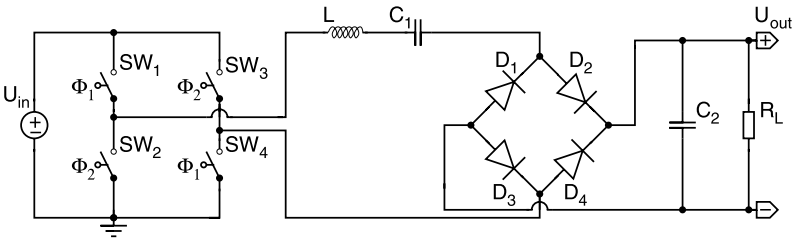

Fig. 3.34 The circuit of an ideal series resonant DC-DC converter

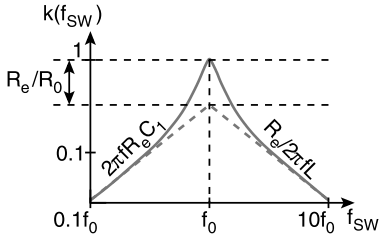

Fig. 3.35 The voltage conversion ratio $k(f_{SW})$ as a function of the switching frequency f_{SW}, for a series resonance DC-DC converter

$$k(f_{SW}) = \|H(f_{SW})\| = \frac{1}{1 + \frac{R_0}{R_e}\left(\frac{f_0}{f_{SW}} - \frac{f_{SW}}{f_0}\right)^2}$$

$$\text{with} \quad \begin{cases} f_0 = \dfrac{1}{2\pi\sqrt{LC_1}} \\ R_0 = \sqrt{\dfrac{L}{C_1}} \\ R_e = R_L \dfrac{8}{\pi^2} \end{cases} \tag{3.26}$$

In (3.26) f_0 is the resonance frequency, R_e is equivalent load resistance seen from the AC input side of the full-bridge rectifier and R_0 is the output resistance at f_0 of the LC-network. The graphical representation of (3.26) is shown in Fig. 3.35, where $k(f_{SW})$ is plotted as a function of f_{SW}. It is observed that $k(f_{SW})$ varies with f_{SW} and that it can have values between zero and one. The maximum $k(f_{SW}) = 1$ occurs at $f_{SW} = f_0$ and this value decreases with either increasing or decreasing values of f_{SW}. Thus, as opposed to the inductive DC-DC converters discussed earlier in this chapter, U_{out} of resonant DC-DC converters is controlled by means of f_{SW} rather than δ. Please note that (3.26) is only valid when the odd harmonics of f_{SW}, produced by the switch-network, are sufficiently attenuated by the LC-network.

The monolithic variants of resonant DC-DC converters are not yet proven to be feasible in the literature. Nevertheless, from a practical point of view this can be possible, regarding some remarks. First, the switching network contains four switches, probably introducing significant losses. Also, the full-bridge rectifier will introduce significant losses, especially at low output voltages, which could be overcome by replacing the diodes by active MOSFETs. In the end, it is questionable if the sig-

☮HIGH-FIELD ASYMMETRIC WAVEFORM ION MOBILITY SPECTROMETRY

The FAIMS technique is used for the separation of chemical components from a bulk sample. It is based on the unique non-linear mobility of ions at high electric fields [Gue10]. A mixture of ions, generated by means of Electro-Spray Ionization (ESI), is conducted between two parallel plates on which a high asymmetric AC voltage is applied, as illustrated in Fig. 3.36(b). A DC-offset voltage enables selectivity for a certain chemical compounds, thereby deflecting the other compounds towards the plates. The selected compound is then analyzed through Mass Spectrometry (MS).

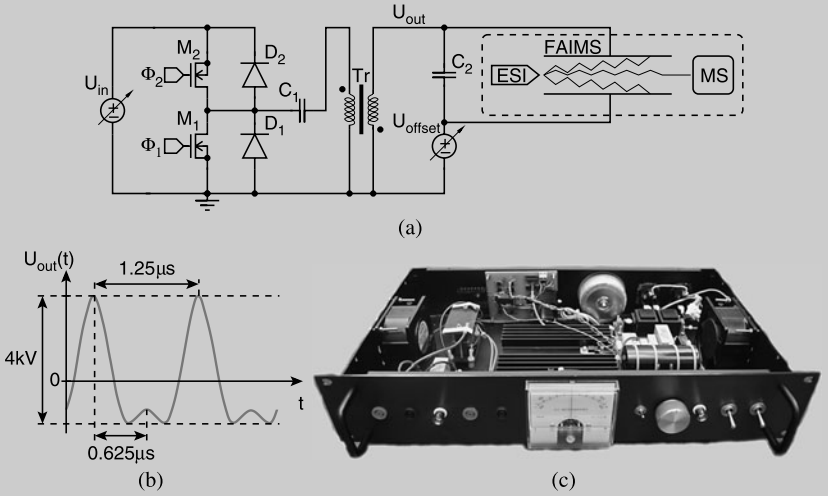

Fig. 3.36 **(a)** The circuit of a halve-bridge galvanic separated series resonance DC-AC high-voltage converter for the FAIMS setup. **(b)** U_{out} of the DC-AC converter as a function of t. **(c)** A photograph of the realization of the DC-AC converter

The circuit of the resonant DC-AC converter which generates the FAIMS's high-voltage is shown in Fig. 3.36(a) and a photo of the implementation is shown in Fig. 3.36(c). The converter achieves a peak-to-peak output voltage U_{out_ptp} of 4 kV at a fundamental frequency of 800 kHz.

nificant amount of additional required components can compete with a simple buck converter, having the same functionality. For this reason monolithic integration of this converter is not regarded practically useful in this work.

Finally, it is noted that step-up/down functionality can also be achieved by means of a parallel resonant LC-network, or the combination of parallel and series resonant networks. Also, galvanic separated variants exits, using the primary winding of a transformer in the LC or LCC-network. These converters are widely used for driving Compact Fluorescent Lamps (CFL). The are also used for multiple-output mains power supplies, in combination with transformers with multiple secondary windings.

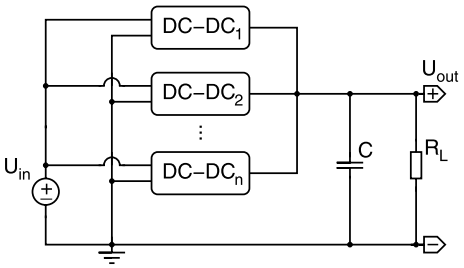

Fig. 3.37 The concept of multi-phase DC-DC converters

3.5 Topology Variations

The primary classes of inductive DC-DC converters, discussed in Sects. 3.1, 3.2 and 3.3, can be adopted, yielding two new subclasses. These subclasses are the multi-phase and the Single-Inductor Multiple-Output (SIMO) DC-DC converters, which are discussed in the respective Sects. 3.5.1 and 3.5.2. A new variant of a SIMO converter, intended for monolithic DC-DC converters, is discussed in Sect. 3.5.3.

3.5.1 Multi-phase DC-DC Converters

The concept of multi-phase DC-DC converters is illustrated in Fig. 3.37. Each of the DC-DC-stages contains a switching-stage and energy-storing elements, except for the output capacitor C which is shared by the DC-DC stages. The multi-phase setup has several possible advantages compared to a single-phase setup, which may be combined with one another:

1. *Output power* P_{out}: For single-phase converter the maximal P_{out} is limited, thus by adding n phases the total maximal P_{out} can be increased with this factor n. The power conversion efficiency will ideally not be affected.
2. *Power conversion efficiency* η_{SW}: η_{SW} is a function of P_{out} and will tend to drop above a certain P_{out} level, for a non-ideal converter. Adding DC-DC stages can enable the individual stages to be operated more closely to their optimal power conversion efficiency point η_{SW_max}, yielding an increased overall η_{SW}. This will of course result in an area A versus η_{SW} trade-off. This methodology is illustrated in Fig. 3.38 for a two-phase versus single-phase DC-DC converter, where the two-phase converter will achieve a higher η_{SW_max} than the single-phase converter, for the same P_{out}.
3. *Area* A: The DC-DC stages are generally operated out of phase of one another, distributing the in- an output current in the time-domain. For a certain specification of the in- and output voltage ripple this will result in relaxed specifications of the in- and output capacitor, compared to a single-phase converter with the same P_{out}. In other words the required A for these components will be reduced. However, the additional inductor(s) and switching-stage(s) will also require more A. Whether or not this will result in a decreased total A requirement will be investigated for the boost and the buck converter in the following sections.

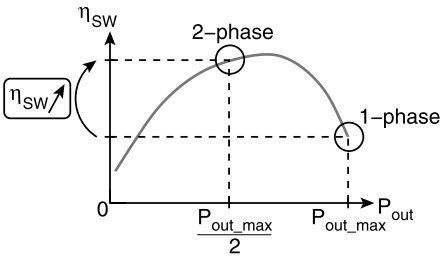

Fig. 3.38 The example of how a two-phase DC-DC converter can achieve a higher power conversion efficiency η_{SW} than a single-phase DC-DC converter, at the same output power P_{out}

4. *Output voltage ripple* ΔU_{out}: The previous trade-off can also be acquired to obtain a lower ΔU_{out} in a multi-phase converter, compared to its single-phase equivalent with the same output capacitor.

It is clear that these possible advantages are mutually non-exclusive, nevertheless they are all contradictory to each other. This will result in important design trade-offs, which will be deducted in Chap. 4.

Multi-phase DC-DC converters can also be implemented using coupled inductors, their feasibility for the purpose of monolithic integration has been demonstrated in [Wib08], which uses a capacitive coupled two-phase buck DC-DC converter topology. This topology has the advantage of eliminating ΔU_{out} for the entire voltage conversion ratio range, assuming ideal converter components. Therefore, it can achieve high power densities because the required capacitance for the output capacitor is minimized. Nevertheless, the achieved power density of this implementation is smaller than achieved with a standard four-phase buck converter [Wen09b]. Other possible advantages of coupled inductors in multi-phase topologies is the minimization of the reverse recovery losses in the rectifiers and the reduced phase current unbalance [Lee00]. However, the phase current unbalance in monolithic converters proves not to be a significant problem in monolithic DC-DC converters, because it is largely due to a physical unbalance between the different phases [Eir08]. This problem is more stringent for converters with external components and it can be largely avoided in monolithic converters by respecting the rules of symmetry in the chip lay-out. A more detailed discussion on inductive DC-DC converters with coupled inductors is omitted in this work, as it is virtually impossible to achieve significant magnetic coupling between more than two inductors on-chip, without compromising the quality-factor (Q) of the inductors.

Output Voltage Ripple in Multi-phase Converters

One of the possible benefits of multi-phase DC-DC converters is their ability to achieve a lower ΔU_{out} for the same P_{out}, providing that the individual DC-DC-stages are operated out of phase of each other. The following discussion will explain a mathematical method for the general approximation of ΔU_{out} of n-phase DC-DC converters in CCM. The method assumes that the phase-offset between the consecutive DC-DC-stages is equal to $2 \cdot \pi / n$ rad and that the mathematical relation between ΔU_{out} and δ is known for a single-phase converter.

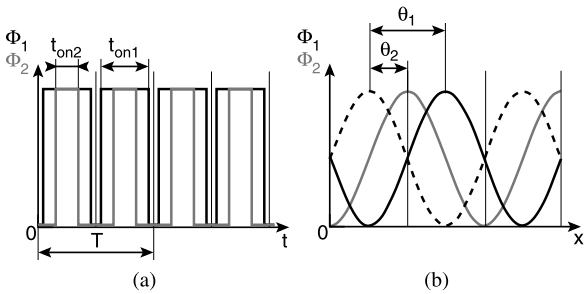

Fig. 3.39 **(a)** The timing signals of a two-phase converter and **(b)** the equivalent representation with sine waves, assuming that the converter is operating in CCM

Consider the timing signals of a two-phase DC-DC converter, as illustrated in Fig. 3.39(a), where both converters are operated with a phase-offset of π rad. The gray timing signal represents a value of δ much smaller than 50% and for the black timing signal the value of δ is close to 50%. When assuming that the output filter of the DC-DC converter only passes the fundamental frequency f_{SW} of the switch-network, $u_{out}(t)$ of a single-phase converter is a pure sine wave. It follows that the total $u_{out}(t)$ of the two-phase converter will be the sum of two sine-waves. Therefore, it can intuitively be understood that ΔU_{out} will be zero when the value of δ of the individual DC-DC-stages is equal to 50% and that ΔU_{out} will have a finite value for all other values of δ. Hence, the physical effect of the value of δ on ΔU_{out} can be modeled by the phase difference θ between the two sine waves, as illustrated in Fig. 3.39(b). This leads to the projection of δ onto θ, which is stated by (3.27).

$$\begin{gathered} \delta : 0\% \rightarrow 100\% \\ \Downarrow \\ \theta : 0 \text{ rad} \rightarrow 2 \cdot \pi \text{ rad} \end{gathered} \tag{3.27}$$

The approximation of $u_{out}(t)$ is calculated by the sum of two sine waves, having a phase difference as given by (3.27), resulting in $u_{out}(x)$ which is given by (3.28).

$$u_{out}(x) = \sin(x) + \sin(x + \theta) \tag{3.28}$$

The value of ΔU_{out} is approximated by the amplitude of (3.28): $\hat{u}_{out}$. This is calculated by equating the derivative of $u_{out}(x)$ to zero, yielding (3.29).

$$\begin{aligned} \hat{u}_{out}(x) = \frac{du_{out}(x)}{dx} &= \cos(x) + \cos(x + \theta) = 0 \\ \Longrightarrow \quad x &= \arccos\left(\frac{\sin(\theta)}{2\sqrt{\cos^2\left(\frac{\theta}{2}\right)}}\right) \end{aligned} \tag{3.29}$$

The locus of $\hat{u}_{out}$ as a function of θ is calculated by substituting x from (3.29) and replacing it in (3.28), after simplification this yields (3.30).

$$\hat{u}_{out}(\theta) = \sqrt{2}\sqrt{1 + \cos(\theta)} \tag{3.30}$$

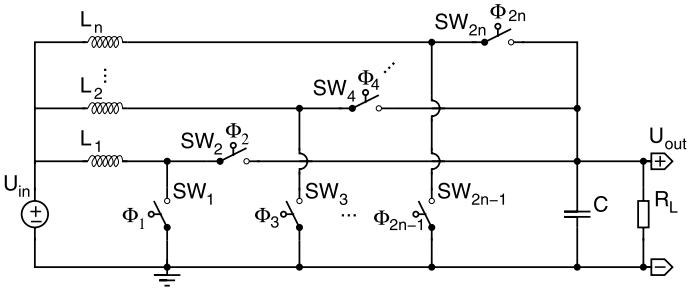

Fig. 3.40 The circuit of an ideal n-phase boost DC-DC converter

Finally, the combination of (3.30) and (3.27) yield the factor Υ, given by (3.31). Υ is to be multiplied with the function $\Delta U_{out}(\delta)$ of any given single-phase converter, resulting in the approximation of $\Delta U_{out}(\delta)$ for its n-phase equivalent, were n is a power of 2. The factor K is dependent on the form-factor of the current trough the output capacitor of the converter. It is equal to 4 for a square waveform (e.g. boost converter) and it is equal to 2 for a triangle waveform (e.g. buck converter).

$$\Upsilon = \prod_{i=1}^{n'} \frac{1}{K}\sqrt{2}\sqrt{1+\cos(\pi 2^i \delta)} \quad \text{with} \quad n = 2^{n'} \blacksquare \tag{3.31}$$

This approximation for ΔU_{out} will be validated for a boost and a buck converter in the following sections. Please note that this approximation is only valid for CCM. For DCM the method for calculating ΔU_{out} also depends on the converter topology and a general analytical method does not exist. Moreover, it will strongly depend on the type of control strategy, as will be discussed in Chap. 5.

Multi-phase Boost Converter

Figure 3.40 shows the circuit of an ideal n-phase boost DC-DC converter, requiring n inductors, $2 \cdot n$ switches and one output capacitor. The following discussion will show the calculation method for ΔU_{out} of a two-phase boost converter example, in CCM.

The calculation of ΔU_{out} for a boost converter requires the knowledge of $i_C(t)$, as explained in Sect. 2.3.3. For this purpose, $i_C(t)$ is graphically represented in Fig. 3.41(a) and (b) for the respective cases where $\delta < 50\%$ and $\delta > 50\%$. First, the case for $\delta < 50\%$ is discussed. It is observed in Fig. 3.41(a) that for this case the currents from L_1 and L_2 show an overlap during the discharge phase of the inductors. During t_{on} of each DC-DC-stage $i_C(t)$ is given by (3.32).

$$\delta < 50\%: \quad 0 \rightarrow t_{on} \quad \Longrightarrow \quad i_C(t) = \frac{I_{L\_max} + I_{L\_min}}{2} - \frac{\overline{U_{out}}}{R_L} \tag{3.32}$$

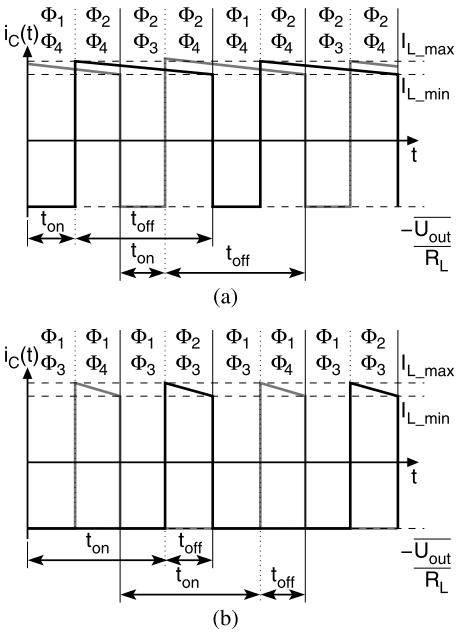

Fig. 3.41 **(a)** The current $i_C(t)$ through the output capacitor C of a 2-phase boost converter for $\delta < 50\%$ and **(b)** for $\delta > 50\%$, both valid for CCM. $i_C(t)$ is divided into the respective parts from the first (*black curve*) and second converter (*gray curve*)

In (3.32) only the parameters I_{L_max} and I_{L_min} are unknown. They can be solved from the system of equations formed by the expressions for $\overline{I_{out}}$ and ΔI_L, as stated by (3.33).

$$\begin{cases} \overline{I_{out}} = 2\dfrac{I_{L\_max} + I_{L\_min}}{2}(1-\delta) = \dfrac{\overline{U_{out}}}{R_L} \\ \Delta I_L = I_{L\_max} - I_{L\_min} = \dfrac{U_{in}}{L} t_{on} \end{cases} \tag{3.33}$$

By means of (3.32) and (3.33) ΔU_{out} can be found, using the same method as (2.65). Finally, substituting $\overline{U_{out}}$ by (2.62), yields (3.34).

$$\begin{aligned} \delta < 50\%: \quad \Delta U_{out} &= -\frac{1}{C}\int_0^{t_{on}} i_C(t)\,dt = \frac{t_{on}}{C}\left(\frac{\overline{U_{out}}}{R_L} - \frac{I_{L\_max} + I_{L\_min}}{2}\right) \\ &= \frac{T U_{in}(\delta - 2\delta^2)}{2C R_L (\delta - 1)^2} \blacksquare \end{aligned} \tag{3.34}$$

For the second case where $\delta > 50\%$, as illustrated in Fig. 3.41(b), the currents from L_1 and L_2 do not overlap during their respective discharge phase. Thus, $i_C(t)$ is calculated through (3.35).

$$\delta > 50\%: \quad 0 \to \frac{t_{on} - t_{off}}{2} \quad \Longrightarrow \quad i_C(t) = \frac{\overline{U_{out}}}{R_L} \tag{3.35}$$

Again by using (3.35) in (2.65) and replacing $\overline{U_{out}}$ by (2.62), yields (3.36).

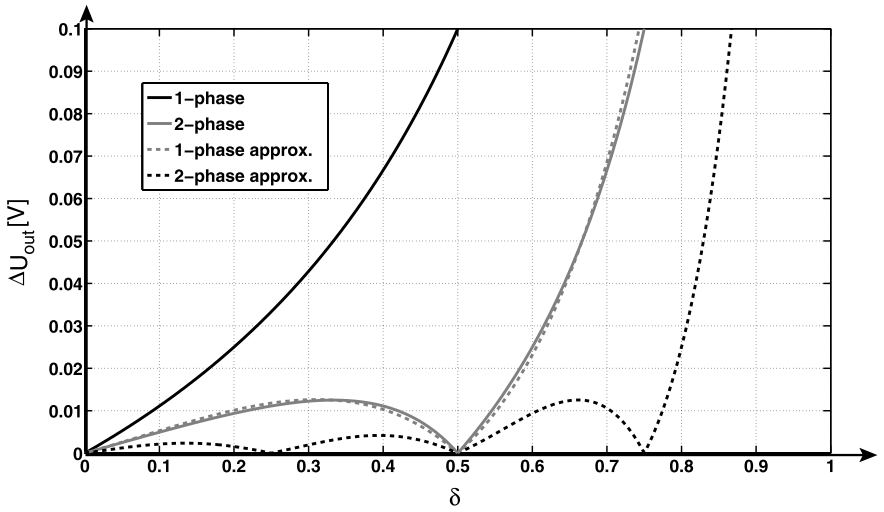

Fig. 3.42 The output voltage ripple ΔU_{out} as a function of the duty-cycle δ for an ideal 1-phase, 2-phase and 4-phase boost DC-DC converter. For the 1-phase and 2-phase boost converter both the exact and approximated functions are plotted. For the 2-phase and 4-phase boost converter the approximated functions are plotted

$$\delta > 50\%: \quad \Delta U_{out} = -\frac{1}{C}\int_0^{\frac{t_{on}-t_{off}}{2}} i_C(t)\,dt = \frac{\overline{U_{out}}}{CR_L}\left(\frac{t_{on}-t_{off}}{2}\right)$$
$$= \frac{TU_{in}(1+2\delta)}{2CR_L(1-\delta)} \blacksquare \tag{3.36}$$

To conclude the discussion on the multi-phase boost converter, ΔU_{out} is plotted as a function of δ in CCM, which is shown in Fig. 3.42, for the values of Table 3.8 and for $C = 25$ nF. In this figure (2.65) is plotted for a single-phase boost converter (black curve) and the positive parts of (3.34) and (3.36) yield the curve for a two-phase boost converter (gray curve). The curve for a two-phase boost converter can also be approximated by the product of (2.65) with (3.31) for $n = 2$, which is shown by the gray dotted curve. It can be seen that both the exact curve and the approximated curve form a good match. By using this approximation a four-phase converter can also easily be plotted, which is shown by the black dotted curve.

It is clear that the use of multiple phases dramatically reduces ΔU_{out} and that ΔU_{out} will even become zero at certain values for δ, increasing with the number of phases. The fact that ΔU_{out} is not dependent on the inductances of the inductors implies that multi-phase boost converters can achieve a significant area reduction, because the value of C can be smaller for the same ΔU_{out}, at constant P_{out}. This is of course only the case for CCM and will therefore prove to be of limited use for the purpose of monolithic integration, since these converters will tend to perform more efficient at DCM (see Chap. 4). In DCM the positive effect of multi-phase converters on ΔU_{out} will strongly depend on the control strategy, which is discussed

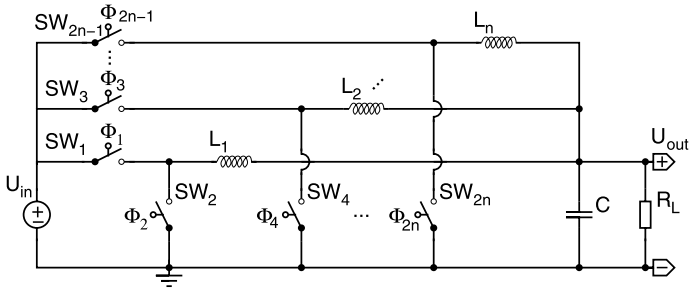

Fig. 3.43 The circuit of an ideal n-phase buck DC-DC converter

in Chap. 5. Notice that multi-phase monolithic DC-DC step-up converters have not yet been proven in the literature.

Multi-phase Buck Converter

Figure 3.43 shows the circuit of an ideal n-phase DC-DC buck converter, using n inductors, $2 \cdot n$ switches and one output capacitor. The following discussion will show the calculation method for ΔU_{out} of a two-phase buck converter example, in CCM.

The calculation of ΔU_{out} for a buck converter requires the knowledge of the total current ripple ΔI_{L_tot} through the inductors L_1 and L_2, as explained in Sect. 3.1.1. Therefore, $i_{L\_1}(t)$ and $i_{L\_2}(t)$ are plotted in Fig. 3.44(a) and (b) for the respective cases where $\delta < 50\%$ and $\delta > 50\%$. First, the case for $\delta < 50\%$ is considered. It can be seen in Fig. 3.44(a) that ΔI_{L_tot} is given by (3.37).

$$\delta > 50\%: \quad \Delta I_{L\_tot} = \Delta I_{L\_1} + \Delta I_{L\_2} = \frac{t_{off} - t_{on}}{2} 2 \frac{U_{out}}{L} \tag{3.37}$$

By using (3.37) with the same method used to calculate (3.7) ΔU_{out} for a two-phase buck converter is obtained, as given by (3.38).

$$\delta < 50\%: \quad \Delta U_{out} = \frac{\Delta Q}{C} = \frac{\Delta I_{L\_tot} T}{8C} = \frac{(\delta - 2\delta^2) T^2 U_{in}}{8CL} \blacksquare \tag{3.38}$$

For the second case where $\delta > 50\%$, as shown in Fig. 3.44(b), ΔI_{L_tot} is calculated through (3.39).

$$\delta > 50\%: \quad \Delta I_{L\_tot} = \Delta I_{L\_1} + \Delta I_{L\_2} = \frac{t_{on} - t_{off}}{2} 2 \frac{U_{in} - U_{out}}{L} \tag{3.39}$$

Similar to (3.38), (3.39) yields ΔU_{out} for $\delta > 50\%$, which is given by (3.40).

$$\delta > 50\%: \quad \Delta U_{out} = \frac{\Delta Q}{C} = \frac{\Delta I_{L\_tot} T}{8C} = \frac{(\delta - \delta^2) T^2 U_{in}}{8CL} \blacksquare \tag{3.40}$$

The discussion on the two-phase buck converter is concluded with the graphical representation of ΔU_{out} as a function of δ for CCM, which is illustrated in Fig. 3.45.

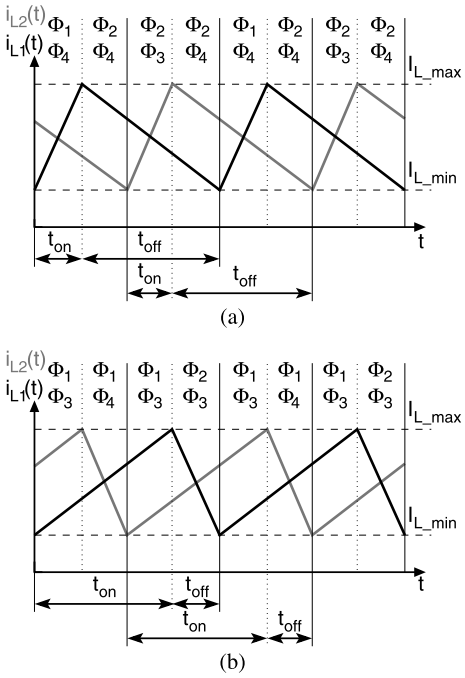

Fig. 3.44 **(a)** The respective currents $i_{L1}(t)$ and $i_{L2}(t)$ through inductors L_1 and L_2 of a 2-phase buck converter for $\delta < 50\%$ and **(b)** for $\delta > 50\%$, both valid for CCM

The parameters used for this plot are the same as in Table 3.1 and for $C = 12.5$ nF. The black curve is valid for a single-phase buck converter, as given by (3.7). The gray curve is the plot for a two-phase buck converter, of which the two sections are given by the positive values of (3.38) and (3.40). The approximation of ΔU_{out} for the two-phase buck converter, calculated by multiplying (3.7) with (3.31) for $n = 2$, is shown by the gray dotted curve. It can be seen that this approximation shows a good correspondence with the exact curve. The approximation for a four-phase buck converter is calculated similar to the two-phase converter, but for $n = 4$, and it is shown by the black dotted curve.

Clearly, the use of multi-phase buck converters can also dramatically reduce ΔU_{out}, especially for certain values of δ. However, opposed to the multi-phase boost converter, ΔU_{out} for the multi-phase buck converter is inverse proportional to the inductances of the inductors. Thus, for maintaining the same area requirement as for a single-phase converter the inductance per phase should be approximately be the n-times smaller than for the single-phase equivalent. This is not represented in Fig. 3.45, where the value of the individual inductances is always 10 nH. When applying the fixed total inductance of 10 nH, the curves of Fig. 3.45 will all reach the same maximal amplitude compared to the single-phase converter. This implies that there will still be an advantage for ΔU_{out} for certain values of δ, but for other certain values of δ the advantage might become very small and even non-existing. It is clear that these situations should be avoided. Note that, analogue to the boost converter, monolithic (multi-phase) buck converters will tend to be operated in DCM, due to the associated increased efficiency. In DCM the ΔU_{out} reduction will strongly

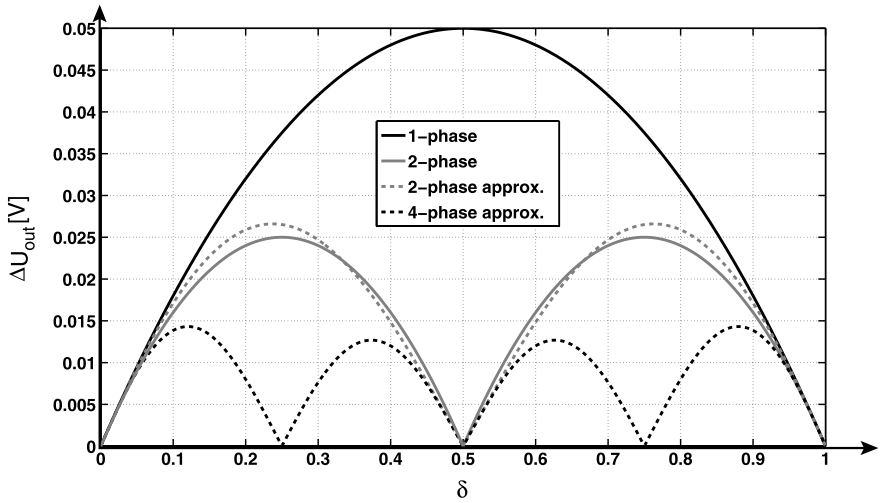

Fig. 3.45 The output voltage ripple ΔU_{out} as a function of the duty-cycle δ for an ideal 1-phase, 2-phase and 4-phase buck DC-DC converter. For the 1-phase and 2-phase buck converter both the exact functions are plotted. For the 2-phase and 4-phase buck converter the approximated functions are plotted

depend on the used control strategy. A more in depth discussion on this topic is therefore provided in Chap. 5.

Monolithic multi-phase DC-DC buck converters are proven feasible in literature, where [Abe07] discusses a two-phase implementation and [Wen09b] discusses a four-phase implementation. It shows these multi-phase converters are capable of achieving a high value P_{out} of 800 mW and that they are able to achieve a high power density of 213 mW/mm^2 [Wen09b]. At the time of writing these are the highest values reported in the literature for monolithic DC-DC converters in a standard CMOS technology. This converter, along with another multi-phase buck converter implementations, is discussed in Chap. 6.

3.5.2 Single-Inductor Multiple-Output DC-DC Converters

The concept of Single-Inductor Multiple-Output (SIMO) DC-DC converters is shown in Fig. 3.46. It comprises a single DC-DC-stage and multiple outputs, each separated from both the DC-DC-stage and from one another by means of switches. Each of the individual outputs also has a dedicated output capacitor.

The two main methods for distributing the delivered energy of the DC-DC-stage over the multiple outputs are [Kwo09]:

1. *Dedicated charge/discharge cycle*: The inductor of the DC-DC stage is consecutively charged by U_{in} and discharged through one of the outputs.

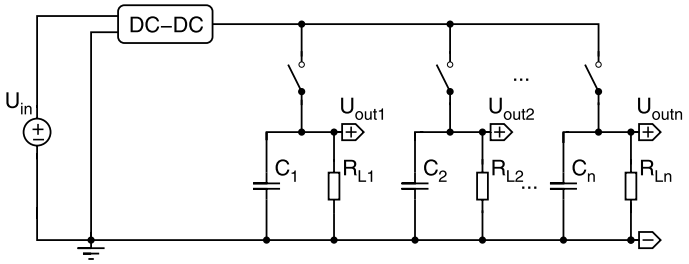

Fig. 3.46 The concept of Single-Inductor Multiple-Output (SIMO) DC-DC converters

2. *Shared charge/discharge cycles*: The inductor of the DC-DC-stage is first charged and then consecutively discharged through the different outputs.

Many variants of these two methods are possible, such as: the CM, the order in which to charge the outputs, Pulse Width Modulation (PWM) or Pulse Frequency Modulation (PFM) switching-schemes... Control methods suited for monolithic integration are discussed in Chap. 5. It is also possible to combine the multi-phase concept, explained in Sect. 3.5.1, with the SIMO concept to increase P_{out}, decrease ΔU_{out}, or combinations of both. An implementation example of such a combination is given in Chap. 6. Finally, it is noted that galvanic separated DC-DC converters, which are discussed in Sect. 3.4.1, are intrinsically suited for the SIMO concept, just by adding additional secondary windings [Ma03]. Clearly this method allows for only one output to be controlled in terms of P_{out}, since the separate secondary windings still share the same (magnetic) core.

In the following sections a SIMO boost and SIMO buck converter are briefly discussed.

SIMO Boost Converter

Figure 3.47 shows the circuit of an ideal SIMO boost DC-DC converter with n outputs. The converter requires one inductor, $n + 1$ switches and n output capacitors. Similar to a standard boost converter, the SIMO boost converter draws a continuous input current in CCM and the currents delivered to the outputs are always discontinuous. Also, all the switches and outputs are non-floating.

It can be concluded that this converter is suited for the purpose of monolithic integration. It has the advantage of being able to deliver multiple output voltages with only one inductor. This can certainly be beneficial for the area requirement, compared to separate single-output converters. The main drawback will obviously be the fact that the limited amount of energy, which can be stored in the inductor is to be divided over the outputs. This type of converter has not yet been reported in the literature as being practically realized in its monolithic form. Nevertheless, a practical realization performed in this work is discussed in Chap. 6.

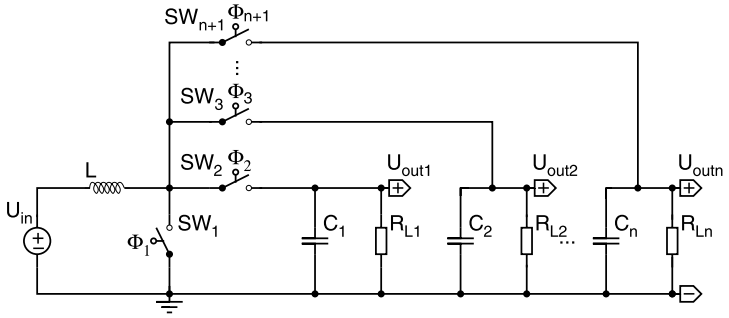

Fig. 3.47 The circuit of an ideal SIMO boost DC-DC converter with n outputs

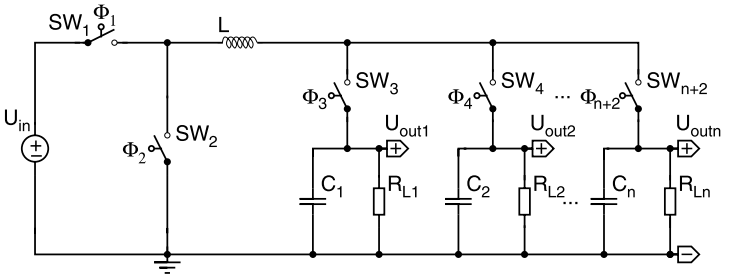

Fig. 3.48 The circuit of an ideal SIMO buck DC-DC converter with n outputs

SIMO Buck Converter

Figure 3.48 shows the circuit of an ideal SIMO buck DC-DC converter with n outputs. This converter incorporates one inductor, $n + 2$ switches and n output capacitors. Similar to a standard buck converter the SIMO buck converter draws a discontinuous input current in CCM, but opposed to a standard buck converter the currents delivered to the outputs are also always discontinuous. This implies that the individual output capacitors will require an increase capacitance, compared to a single-output buck converter with the same P_{out} and ΔU_{out}. Also, during the respective discharge cycles of the inductor through the outputs, two switches are in the current path: SW_1 and one of the output-select switches SW_3–SW_n. This will cause increased conduction losses due to these switches.

Apart from the drawbacks of this converter, compared to its single output equivalent, it is still considered suited for the purpose of monolithic integration. The area advantage over n single output converters will be lower, compared to the SIMO boost converter, because of the discontinuous output current. Also, the power conversion efficiency will tend to be somewhat lower compared to its single-output equivalent, due to the increased conduction losses. To the author's knowledge this type of converter has not yet been reported in its monolithic form in the literature.

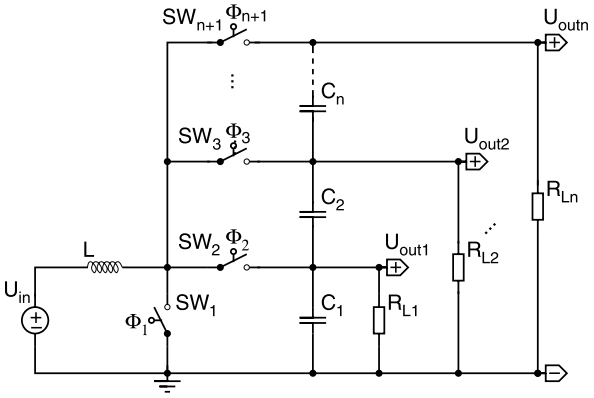

Fig. 3.49 The circuit of an ideal DC-DC boost Series Multiple Output Converter (SMOC) with n outputs

3.5.3 On-Chip Topologies

The SIMO converters, discussed in Sect. 3.5.2, all have an intrinsic disadvantage for the purpose of monolithic integration. Namely, when one or more of their output voltages is higher than the nominal supply voltage of the used IC-technology, the output capacitors will have to be implemented as the series connection of two or more capacitors. The reason for this is that the output capacitors are commonly implemented as Metal-Insulator-Metal (MIM) capacitors or as Metal-Oxide-Semiconductor (MOS) capacitors, which have a maximum operating voltage which in most is cases limited to the nominal technology supply voltage.

The following two sections provide the solution for this area-consuming problem: the Series Multiple Output Converter (SMOC). This topology variation will be discussed for a boost and a buck converter in the following sections. Please note that a similar topology variation has been proposed in [Nam09]. However, [Nam09] uses asynchronous freewheeling diodes rather than synchronous switches and it is intended for a different area of applications, incorporating external components and high voltages (few hundred volts).

SMOC Boost Converter

Figure 3.49 shows the circuit of an ideal boost SMOC with n outputs. This converter requires the same number components as a regular SIMO boost converter. In a standard CMOS implementations the required number of output capacitors is reduced with the SMOC topology, compared to the SIMO topology. This reduction can be understood by means of a simple example, comparing a two-output SIMO and SMOC converter in CCM, which is provided in Table 3.18. For this example it is assumed that all the in- and output parameters for the two converters are equal. It is also assumed that $P_{out\_1} = P_{out\_2}$, implying that the output capacitor C_{out_2} of output number two can have half the capacitance of the output capacitor C_{out_1} of output number one, for the same value of ΔU_{out}. This can be understood through

Table 3.18 The comparison of the required total output capacitance for a two-output boost SIMO and SMOC converter in CCM

	SIMO	SMOC
U_{out_1}	U_{dd}	U_{dd}
U_{out_2}	$2 \cdot U_{dd}$	$2 \cdot U_{dd}$
C_{out_1}	C	C
C_{out_2}	$C/2$	$C/2$
$\#C_{out\_1}$	C	C
$\#C_{out\_2}$	$2 \cdot C$	C
$\#C_{out\_tot}$	$3 \cdot C$	$2 \cdot C$

(2.65) for CCM, as $\overline{I_{out\_1}} = 2 \cdot \overline{I_{out\_2}}$. Furthermore, it is assumed that the maximum operating voltage of a capacitor is equal to U_{dd}. The difference between the two converters is found in the total required capacitance $\#C_{out\_2}$ to implement C_{out_2}. For the SIMO converter, having a dedicated output capacitor for each output, two capacitors each having a capacitance of twice the required capacitance for C_{out_2} need to be connected in series. The SMOC converter on the other hand, requires only one capacitor having twice the required capacitance. Thus, it can be concluded that the SMOC converter in this example achieves an area reduction of $1/3$ for the output capacitors.

The conclusion for the novel boost SMOC topology is that it is better suited for monolithic integration compared to a SIMO boost converter topology, because it can achieve the same specifications with less area. Obviously, this statement is only true for the condition that one or more of the output voltages is higher than the nominal maximum operating voltage of the capacitors. Moreover, this area reduction will become more significant when the output voltages become higher, requiring more capacitors to be placed in series. The example from Table 3.18 is only valid for CCM, but the proof that this statement is also valid for DCM is trivial. However, for that case the area reduction is more dependent on in- and output parameters and it is therefore omitted. Note that a monolithic variant of this converter has not yet been achieved.

SMOC Buck Converter

Figure 3.50 shows the circuit of an ideal buck SMOC with n outputs. This converter requires the same number components as a regular SIMO buck converter. Similar to the boost SMOC the buck SMOC is able to achieve a reduction of the required total output capacitance in a standard CMOS implementations, compared to the SIMO topology. This reduction is again discussed by means of a simple example, comparing a two-output SIMO and SMOC converter in CCM, which is provided in Table 3.19. For this example it as assumed that all the in- and output parameters for the two converters are equal. It is also assumed that $U_{in} = 3 \cdot U_{dd}$, $U_{out\_1} = U_{dd}$ and $U_{out\_2} = 2 \cdot U_{dd}$, implying that the two output capacitors C_{out_1} and C_{out_2} have the same capacitance for the same value of ΔU_{out}. This can be understood through (3.7)

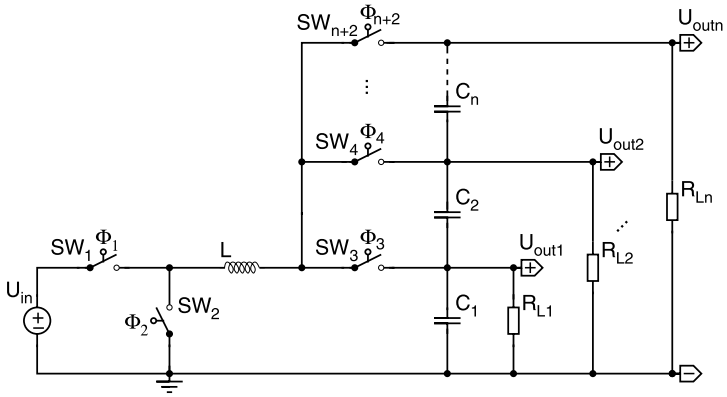

Fig. 3.50 The circuit of an ideal DC-DC buck Series Multiple Output Converter (SMOC) with n outputs

Table 3.19 The comparison of the required total output capacitance for a two-output buck SIMO and SMOC converter in CCM

	SIMO	SMOC
U_{out_1}	U_{dd}	U_{dd}
U_{out_2}	$2 \cdot U_{dd}$	$2 \cdot U_{dd}$
C_{out_1}	C	$2 \cdot C$
C_{out_2}	C	C
$\#C_{out\_1}$	C	$2 \cdot C$
$\#C_{out\_2}$	$4 \cdot C$	$2 \cdot C$
$\#C_{out\_tot}$	$5 \cdot C$	$4 \cdot C$

for CCM, which yields the same value for both $\delta = 1/3$ and $\delta = 2/3$. Furthermore, it is assumed that the maximum operating voltage of a capacitor is equal to U_{dd}. The difference between the two converters is found in the total required capacitance $\#C_{out\_2}$ to implement C_{out_2}. For the SIMO converter, having a dedicated output capacitor for each output, two capacitors each having a capacitance of twice the required capacitance for C_{out_2} need to be connected in series. The SMOC converter on the other hand, requires only one capacitor having twice the required capacitance. Thus, it can be concluded that the SMOC converter in this example achieves an effective area reduction of $1/5$ for the output capacitors.

It is concluded that the new buck SMOC topology is better suited for monolithic integration compared to a SIMO buck topology, because it can achieve the same specifications with less area. Obviously, this statement is only true for the condition that one or more of the output voltages is higher than the nominal maximum operating voltage of the capacitors. Although the actual area reduction of the buck SMOC in CCM is less compared to the boost SMOC, there is also an inherent advantage of the buck SMOC. It turns out that C_{out_1} is twice the required value when using the SMOC topology, therefore ΔU_{out_1} will be only half of the value achieved

with the SIMO topology. Analogue to the boost SMOC, the area reduction of the buck SMOC will become more significant when the output voltages become higher, requiring more capacitors to be placed in series. The example from Table 3.19 is only valid for CCM, but the proof that this statement is also valid for DCM is trivial. However, for that case the area reduction is more dependent on in- and output parameters and is therefore omitted. A monolithic realization of this converter, combined with multi-phase, is discussed in Chap. 6.

3.6 Conclusions

In this chapter the most used inductive DC-DC converter topologies are discussed, with respect to monolithic integration.

First, the primary classes of step-down, step-up and step-up/down converters are discussed in the respective Sects. 3.1, 3.2 and 3.3. Within each primary class a comparison is performed on various topologies, with respect to the output voltage ripple. This leads to the conclusion that for a maximal output power and a minimal reacquired area the following topologies are best suited:

- *Step-down*: Buck converter.
- *Step-up*: Boost converter.
- *Step-up/down*: Zeta converter.

Secondly, two other types of inductive DC-DC converters are discussed in Sect. 3.4:

- *Galvanic separated converters*: These converters require an on-chip transformer, which has two intrinsic drawbacks. The first drawback is that the energy conversion efficiency is proportional to the mutual coupling factor between the windings, which is never maximal. This causes the theoretical power conversion efficiency to be lower than 100%. The second drawback is the fact that the series resistance of the windings will be higher, compared to an inductor occupying the same area. This will cause increased losses. The flyback converter is considered best fitted for monolithic integration, as it requires merely one switch and one rectifier. Thus, suffering minimal losses in these components.
- *Resonant converters*: These converters are not considered practical for monolithic integration as their switch-network and rectifiers will cause high losses.

Thirdly, topology variations on the primary class of DC-DC converters are discussed in Sect. 3.5.

- *Multi-phase topologies*: These converters can be used to: increase the output power, to increase the power conversion efficiency, to decrease the output voltage ripple and/or increase the power density. All of these potential benefits are all contradictory to one another, but not mutually exclusive. Therefore, multi-phase converters are considered promising for monolithic integration.

- *SIMO converters*: These converters have multiple outputs, using only one inductor. For a certain limited output power they will require less area than a combination of single-output converters.
- *SMOC topologies*: These converters have the same functionality as SIMO converters. They require less area by placing the output capacitors in series, limiting the voltage across each capacitor to its nominal maximum supply voltage.