Design of an Integrated 60 GHz Transceiver Front-End in SiGe:C BiCMOS Technology

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Abstract

This thesis describes the complete design of a low-cost 60 GHz front-end in SiGe BiCMOS technology. It covers the topics of a system plan, designs of building blocks, designs of application-boards and real environment tests. Different LNA and mixer topologies have been investigated and fabricated. Good agreements between measurements and simulations have been achieved due to the used component models. A transceiver front-end system is built based on these blocks. A heterodyne architecture with a 5 GHz IF is adopted because it is compatible with IEEE 802.11a, which allows the reuse of some building blocks to realize a 5 GHz transceiver. The transceiver chips are assembled onto application boards and connected by bond-wires. Bond-wire inductances have been minimized by using a cavity and an on-board compensation structure. The front-end has been tested by both QPSK and OFDM signals in an indoor-environment. Clear constellations have been measured. This is the first silicon-based 60 GHz demonstrator in Europe and the second in the world.

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Chapter I Introduction

In the last few decades, communication technologies have been increasing exponentially from the very beginning of voice communication to today's data communication. Nowadays, almost all information is in digital form. Internet and intranet have been used extensively to transfer information globally and locally. The invention of Wireless Local Area Network (WLAN) gets rid of cable connections within a room or a building providing more freedoms in mobility. However, the highest data-rate that can be achieved is 54 Mbit/s among all of the current WLAN standards, which is half of the current 100 Mbit/s Ethernet. Next generation Ethernet will have a data-rate of 1 Gbit/s. Apparently, a very-high-speed wireless standard needs to be developed for giga-bit-per-second Ethernet. There are many other applications demanding wireless communication techniques with high data rates if one wants to remove the clumsy high-frequency-cables, e.g. HDTV.

To transmit such a high data-rate, a wide frequency band is needed. For instance, a bandwidth of 500 MHz is needed for 1 Gbit/s if a QPSK modulation without any error coding overhead is used. If a one-half coding scheme is used, the minimum bandwidth is 1 GHz. On the other hand, the frequency resources at low frequencies have already been allocated to other applications. This pushes the carrier frequency to microwave and millimeter wave. The best frequency candidate for short range communications is around 60 GHz, at a band that it is not suited for long-range communications due to the atmospheric attenuation. In a short range, this attenuation is of no significance. Many counties and districts have marked this band as unlicensed band, those are: Japan, 59.0-66.0 GHz; USA and Canada, 57.05-64.0 GHz; Korea, 57.0-64.0 GHz; Europe, 57.0-66.0 GHz; China, 59.0-66.0 GHz and Australia, 59.4-62.0 GHz.

This work is to investigate the feasibility of designing a low-cost 60 GHz transceiver system, which is sponsored by German Federal Ministry of Education and Research (BMBF), and is a part of the previous project 'WIGWAM'. This work mainly focuses on the front-end design of an integrated 60 GHz transceiver.

1.1 Technologies for 60 GHz applications

The cost of a chipset comprises the cost of the chips and the cost of its packaging. The packaging cost would be very high if the building blocks of a millimeter wave RF system are integrated at board level. Furthermore, the packaging loss is high if a cheap substrate is to be used. In order to reduce the total cost, a high integration level is preferable. III/V technologies, e.g. GaAs, have the fastest transistors and offer excellent RF performance, such as low noise figure and high output power. However, they are not suited for low-cost mass production because of their wafer cost and low integration level. CMOS is the cheapest technology among other semiconductor technologies. Unfortunately, in the beginning of this work, the speed of CMOS transistors was not fast enough for 60 GHz RF front-end designs. Even with today's 60 nm CMOS technologies, there are still many difficulties to be solved. Scaling down the feature size does increase the transistor speed, but the breakdown voltage is decreased as well. The design of a reliable power amplifier in CMOS becomes more difficult requiring very sophisticated power combining techniques, which of course will increase the time-to-market cost.

SiGe BiCMOS technology combines both high speed HBTs with relatively high breakdown voltages and standard CMOS transistors allowing a very high integration level. In this work, a 0.25 um SiGe:C BiCMOS technology from IHP is adopted for the whole transceiver design. The high performance (H1) process from the technology is used, which is optimized for high frequency applications. Both high speed HBTs and CMOS transistors are available in this process. The HBTs have an ft/fmax combination of 200/200 GHz, and have different sizes ranging from one finger to eight fingers. The open base breakdown voltage, V_{CBO}, is about 2 V. Three types of resistors are available, those are n-type poli-resistor (rpnd), p-type poli-resistor (rppd) and siliside resistor (rsil). Metal-insulator-metal (MIM) capacitors have a capacitance of 1 fF per square micrometer. Some common inductors are also included in the design kit. There are five aluminum metal layers for interconnections. The top two layers have thicknesses of two and three micrometers. They are used in designing low-loss transmission lines and inductors.

1.2 Current status of 60 GHz silicon RFIC

Radio Frequency Integrated Circuits (RFIC) have been investigated for some years in low frequency range (below 10 GHz), where the lumped circuit theory still holds for IC designs. Less work and investigation have been done in millimeter wave ICs due to the technology limitation. Only in recent years, fast transistors for millimeter-wave applications in silicon technologies have been developed. Nowadays, the transit frequency (ft) and maximum oscillation frequency (fmax) of silicon HBTs are approaching 0.5 THz. Before the year 2004, there were no good 60 GHz LNA in silicon technologies. So there was no information upon the integrated 60 GHz transmitter and receiver in literature. The traditional IC design tool, Cadence, is very powerful at time domain simulation, but lacks an electromagnetic (EM) simulation ability. A good design methodology for millimeter wave circuits is required. Fortunately, the design of Microwave Monolithic Integrated Circuit (MMIC) has been studied for some years in III/V technologies. Its methodology can be a good starting point in millimeter-wave silicon designs.

1.3 Characteristics of high frequency design

The challenges in 60 GHz integrated transceiver designs drop down into two fields: circuit designs and low-cost packaging. The circuit building blocks to be designed are an LNA, a down-conversion mixer, an up-conversion mixer and a 60 GHz output buffer. Among the different packaging techniques, bond-wire is the cheapest, and is adopted in this design. However, the minimum bond-wire inductance is in the order of 200 pH to 300 pH, which is a killer to 60 GHz signals. It introduces a high loss due to mismatch, and moreover it may cause an oscillation or even completely mal-function. This effect must be considered in the very beginning of the design phase.

At 60 GHz, the chip size is of the same order of the wavelength requiring microwave design techniques. Distributed components have to be incorporated into the simulation. At high frequency, the circuits are more vulnerable to mismatch. For instance, an overlook of a 10 fF parasitic capacitance may deviate a design or even

make it out of spec. A successful design needs a thorough simulation taking all effects into account. Otherwise, one-time-correct designs are not possible and many design iterations are needed in order to have one working building-block.

In the given silicon technology, the substrate loss is high due to its high conductivity compared to III/V technologies. And this is true for most of the silicon technologies. This loss reduces the Q-factors of inductive components, i.e. transmission lines and inductors. The first idea of reducing the loss is to shield the conductor from the lossy silicon substrate. However in such a case, a much longer and narrower conductor is needed to achieve the same inductance, which increases the resistive loss of the conductor. The properties of inductive structures have to be investigated before the actual circuit design. Three kinds of inductors can be easily realized in silicon technologies: metal line inductors, Coplanar Waveguide inductors and microstrip inductors. In real designs, the choice of inductors depends not only on their Q-factors, but also on their physical dimensions and the ease of integration. A good compromise can only be found by extensive EM simulations and verified by measurements.

1.4 Circuit building blocks to be designed

There are four circuit building blocks for the planned 60 GHz transmitter and receiver, an LNA, a down-conversion mixer, an up-conversion mixer and a 60 GHz output buffer.

1.4.1 LNA

An LNA is used in a receiver to reduce the overall noise figure. High gain and low noise figure are the main requirements of the LNA. High gain implies a high oscillation potential with the bond-wire inductance. A differential topology can reduce the oscillation risk. LNA noise depends on the minimum-noise-figure (NFmin) of active devices and the Q-factor of passive devices. Optimization of passive devices becomes important for a low noise design since we are going to use the available active devices. With the available transistors, the working frequency of 60 GHz is at one third of their ft/fmax, where the power gain decreases. A high gain LNA requires

a multi-stage design. Clearly, the gain and noise distribution of the LNA have to be optimized to achieve a low overall noise-figure and a satisfying gain.

1.4.2 Down-conversion mixer

In a receiver system, a down-conversion mixer down-converts the RF signal to low frequency, where it is easier to be processed. This frequency shift is realized by multiplying two frequencies. A local oscillator (LO) generates a sinusoidal signal, and is used as one frequency (also called pumping frequency). The other frequency is the received RF signal. After multiplying the two signals, the whole RF signal is converted to two bands. A low-pass-filter (LPF) is used to select the lower band. The main specifications of the down-conversion mixer are: noise figure, conversion gain and linearity. A mixer is a three-port block: RF, LO and intermediate frequency port (IF). To achieve a high performance, these three ports are matched to the corresponding load and source impedances. In passive diode mixer designs, this is mainly realized by using R-L-C components. While in active mixer designs, this is realized by both R-L-C components and the optimization of the operating conditions of the active devices.

1.4.3 Up-conversion mixer and output buffer

The transmitter comprises two building blocks: an up-conversion mixer and an output buffer. In reality, they are combined in one building block because the whole transmitter chip is integrated in the first design. The up-conversion mixer does the reverse function of the down-conversion mixer. It up-converts the IF signal to RF frequency. The requirements are similar to the down-conversion mixer except that its linearity is stressed more than noise figure because the IF signal is supposed to be high and white noise has no significant effect. The output power is low after up-conversion. An output buffer is required in order to drive the output PA. High gain and high linearity are the main concerns in the transmitter design.

1.5 Standardization of the 60 GHz band

Currently, the 60 GHz standardization is being developed by IEEE 802.15 Task Group 3c (TG3c). Their main task is to develop the MAC and physical layer of the Wireless Personal Area Network (WPAN) at 60 GHz, which provides a

short-range (less than 10 meter), very-high-speed (more than 2 Gbit/s) data service. The newest agreement in TG3c is that the whole band, 57-66 GHz, is divided into 4 sub-channels, and each channel has 2 GHz plus some guard bands. The center frequencies of those sub-bands are integer multiples of 19.2 MHz in order to use the available quartz crystals. Modulation schemes are still to be decided. This work provides a reference for the standardization committee in specifying the physical layer parameters. IHP is actively contributing to the IEEE standardization committee by presenting our work in their meetings.

1.6 Outline of the thesis

The thesis is organized as follows:
In chapter II, the transceiver system considerations will be discussed.
Chapter III summarizes the design theories of LNA and mixer.
Chapter IV and V describe LNA and mixer designs.
Chapter VI deals with the integration of the transceiver front-end.
Chapter VII covers board design issues and system level measurement results.
In the end a short conclusion concludes this thesis.

Chapter II Transceiver System

This chapter covers the issues of the design of a high frequency transceiver system including channel properties, modulation schemes and link budget. The 60 GHz band is of special interest for short-range communications because of the specific attenuation due to the atmospheric oxygen of 10 to 15 dB/km [1]. The atmospheric loss makes this band not suitable for long-range communications so that it can be dedicated to short-range communications. For the short distances within an indoor environment, the atmospheric loss has no significant impact. Detailed channel parameters have been derived from different channel sounding systems. According to the given channel property, many modulation schemes have been proposed in literature for different application scenarios, e.g. WLAN and HDTV. The arguments are mainly on: frequency efficiency, system complexity, immunity to hardware non-ideality and possibility of low-cost products. The modulation candidates drop into two categories: OFDM and single-carrier, i.e. OOK, QPSK and MSK. Transceiver architectures are in accordance with the intended application scenarios and modulation schemes. Options of transceiver architectures are ZIF, heterodyne with fixed IF and heterodyne with sliding IF. A heterodyne architecture with a 5 GHz fixed IF is adopted in this work, which allows a dual-mode operation at 5 GHz and 60 GHz with little change in hardware. The 60 GHz demonstrator developed in IHP supports both OFDM and single-carrier QPSK with corresponding BB signals. The building block diagram of the developed demonstrator and its link budget will be given at the end of the chapter.

2.1 Indoor channel property

2.1.1 Line-of-sight (LOS) free-space loss

Free-space loss increases with the increase of frequency due to the short wave length. Different channel properties can be expected at 60 GHz compared to that at 5 GHz. We can calculate the LOS loss by using the free-space loss equation:

$$L = 10\log\left(\left(\frac{4\pi df}{c}\right)^2\right) = 20\log(d) + 20\log(f) + 32.44, \qquad (2.1)$$

where *d* is distance (in meter) and *f* frequency (in GHz).

For a distance of one meter, the free-space losses at 60 GHz and 5 GHz are 68 dB and 46 dB, respectively. The link budget at the 60 GHz band will be tighter than that at the 5 GHz band. To overcome the high space loss, a thorough optimization of a transceiver system is necessary. On the other hand, the antenna dimensions at 60 GHz are smaller, where quarter wavelength is only 1.25 millimeter. High gain antennas can be used to improve the link budget, which will reduce the mobility due to the high directivity. Antenna array and beam-forming techniques can overcome this problem. Furthermore, beam-forming technique reduces the in-band interference from other 60 GHz transmitters, and can be used for space diversity. Therefore, the frequency reuse and system capacity are improved. However, the price is that the system is much more complicated.

2.1.2 Delay spread

Apart from the free-space loss, the 60 GHz band exhibits similar normalized-received-power as in low frequency bands, e.g. 2.25 GHz [2]. Moreover, the time dispersion at 60 GHz band is smaller, which is characterized as delay spread. The measured RMS delay spreads (RMSDS) at 60 GHz are 8.8 ns and 13.2 ns for LOS and NLOS cases in a typical indoor environment, while at 2.25 GHz they are 20.9 ns and 27.4 ns [2]. The low RMSDS can be explained as high penetration loss of walls. The 60 GHz signal is well confined within a single room and the reflections or multi-path components from neighboring rooms have no significant effect. Similar RMSDS results have been obtained in [3], where the authors performed a MIMO channel measurement. The short RMSDS implies a wider coherence bandwidth at 60 GHz band, thus a higher data-rate in the absence of equalizers. The channel sounding results from Heinrich-Hertz-Institute (HHI), Berlin, was taken to model the channel [4], where similar Vivaldi antennas as in IHP's demonstrator are used. The measured RMSDSs are 13 ns and 9.5 ns for TX-RX antenna configurations of Omni-Omni and Omni-Vivaldi. RMSDS can be further improved by using a Vivaldi-Vivaldi combination to below 1.5 ns as reported in [5] for a Fan-Fan TX-RX antenna configuration. Taking the reverse of RMSDS in [5] leads to coherence bandwidths are ranging from 660 MHz to 1250 MHz. The delay-spread profile of the Omni-Vivaldi configuration is plotted in figure 2.1 [4].

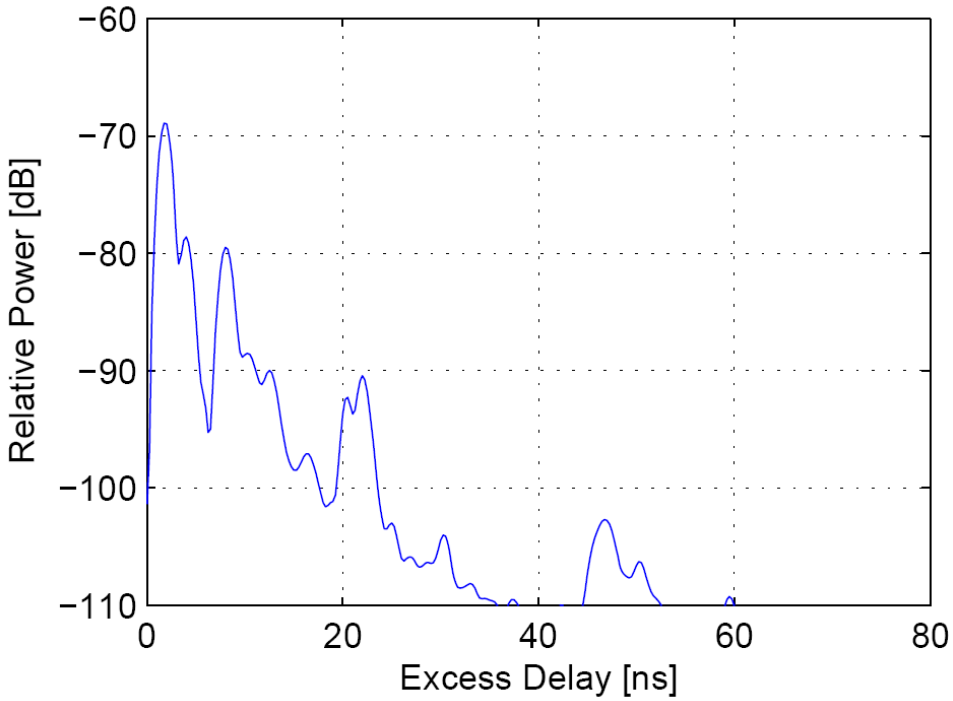


Figure 2.1. Delay-spread of Omni-Vivaldi channel [4].

2.1.3 Doppler shift

A sinusoidal signal may have a frequency spread through a wireless channel due to transceiver movements and the reflections of moving objects, which is characterized as Doppler frequency shift. If we assume the transmitter is fixed, it can be calculated according to the relative speed between the transmitter and receiver by using the equation [6]:

$$f_d = \frac{v}{c} f_c \cos(\alpha) . \qquad (2.2)$$

where c is the speed of light, v the speed of the receiver, f_c the carrier frequency and α the angle between the moving direction and the incident direction. Doppler shift effects will be accumulated in phase domain. In an indoor environment, the moving speeds of transceivers are limited to the walking speed of 2 m/s, thus a maximum Doppler shift of 400 Hz at 60 GHz.

Transceivers are stationary in most of the indoor applications. Doppler frequency spread comes mainly from the reflections of moving objects. The phase of the n-th path reflected at a moving object becomes [5]:

$$\phi_n = \overline{\phi_n} + 4\pi \frac{f_c v}{c} t \cos(\theta_n)\cos(\varphi_n). \quad (2.3)$$

where $\bar{\phi}_n$ is the phase when the channel is static, θ_n the reflection angle of the path at the moving object and φ_n the angle between the direction of the movement and the direction orthogonal to the reflecting surface. At 60 GHz, the Doppler spread can be as high as 1.6 kHz for a moving object with a speed of 2 m/s. Phase noise of the local oscillator contributes to further spreading the instantaneous frequency. Frequency spread is troublesome, and the data structures have to be elaborated to compromise them, especially in OFDM systems [7]. With the use of a directional antenna, the frequency spread and delay spread can be suppressed. However, for multi Gbit/s transmission, the coherent channel bandwidth is not sufficient in single-carrier modulation schemes due to the RMSDS, where complicated equalization techniques are required.

2.2 Modulation schemes

Many modulation schemes have been proposed for 60 GHz applications, including OFDM and single-carrier modulations. OFDM proponents intend to use the 60 GHz band in a high data-rate WLAN or WPAN system in multi-path environments, i.e. NLOS, where RMSDS is high. Proponents of single-carrier modulation schemes intend to use the 60 GHz band in a typical LOS environment. Single carrier proposals include OOK, QPSK and MSK.

2.2.1 Single-carrier modulations

2.2.1.1 Amplitude modulation OOK

On-OFF keying (OOK) or Amplitude Shift Keying (ASK) is the simplest modulation scheme allowing the use of the simplest analog front-end architectures. Its mathematical representation is:

$$f_{OOK}(t) = Am(t)\cos(\omega_c t), \quad (2.4)$$

where *m(t)* is the modulating signal taking the values of 0 and 1, and ω_c the carrier frequency.

An OOK transmitter can be realized by a signal generator followed by a switch. Receivers can use either of the envelope or the coherent detection techniques. In the early stage of 60 GHz applications, OOK was thoroughly investigated due to its simplicity and easy realization. A data rate of 3.5 Gbit/s has been demonstrated with an OOK modem [8], where the system was tested outdoors in a LOS and relatively obstacle-free environment. Furthermore, high gain antennas (23.5 dBi) were used to further reduce the delay spreads. Transceivers in [9] have demonstrated a data-rate of up to 1.5 Gbit/s in an indoor environment with high gain antennas (25 dBi). Advantages of OOK modulation schemes include easy implementation of hardware, usage of non-linear amplifiers and immunity to VCO phase noise. However, OOK has a low frequency-efficiency and the average power is 3 dB lower than the peak power. All the early experiments on OOK were carried out in LOS environments with high gain antennas to suppress the delay spread, avoiding the use of complicated equalizers.

2.2.1.2 Frequency modulations.

Frequency-Shift-Keying (FSK) is a digital modulation scheme, which alters the carrier frequency according to its input signals or the combinations of the input signals. Binary FSK (BFSK) is the simplest form, which has two output frequencies separated by Δf Hz. The frequency spacing is commonly defined as the modulation index, d,

$$d = \Delta f * T \tag{2.5}$$

where T is the symbol duration.

With two band-pass-filters (BPF) followed by two envelope detectors, an FSK signal can be detected non-coherently provided the frequency overlap is trivial. Coherent detection is also applicable for FSK signals, which improves the E_0/N (the ratio of average-energy per bit to noise power-spectral-density) by more than 3 dB compared to OOK modulation for the same data-rate and bandwidth [10]. Under certain conditions, FSK is even superior to phase modulation schemes [11]. FSK is a constant amplitude modulation scheme allowing the use of non-linear PAs, therefore the power efficiency of the transmitter is improved. Of particular interest is the Minimum-shift-keying (MSK) as proposed in IEEE P802.15 work group [12]. MSK is a special case of FSK with a continuous phase change and a modulation index of 0.5. It has a fast roll-off in frequency exhibiting an excellent frequency-efficiency.

With proper filtering techniques (e.g. GMSK), the bandwidth can be further reduced with little degradation in performance.

2.2.1.3 Phase modulations

In phase modulations, the modulating signal shifts the phase of the carrier frequency. It is expressed by the following equation:

$$f_{PSK} = A\cos(\omega t + \phi(t)) \tag{2.6}$$

where $\phi(t)$ is the signal phase modulated by base-band signals.

The most straightforward phase modulation is BPSK, where 0s and 1s are represented by 0 and 180 degrees of the phase of the carrier frequency. By mapping two input bits into one phase shift, QPSK signal can be obtained, where the phase takes values of {0, 90, 180, 270} or {45, 135, 225, 325}. QPSK modulators require quadrature LO signals and serial/parallel converters for the base-band signals [13]. The quadrature baseband signal is generated either by a digital-to-analogue converter (DAC) or by a poly-phase filter [14] [15]. QPSK offers a 5.1 dB improvement in E_0/N compared to coherent OOK modulation scheme [10]. A higher throughput can be reached by combining phase and amplitude modulation techniques, e.g. 16QAM, 64QAM, where linear PAs are required to maintain the amplitude information. However in phase modulations, it is obligatory to use coherent detection techniques. QPSK shows similar performance as MSK and FSK in a multi-path environment and in utilizing non-linear PAs. It has been tested in an indoor LOS environment within this work. Clear constellations have been obtained without equalization techniques, where Vivaldi antennas are used in the transmitter and receiver boards to suppress the delay spread and to improve the link budget.

2.2.2 OFDM modulation

OFDM (Orthogonal Frequency Division Multiplexing) is a multi-carrier modulation scheme. It modulates the base-band signal onto *N* closely-spaced sub-carriers, where the sub-carriers are orthogonal to each other. Traditional single-carrier modulations are used for each sub-channel. The signals on each sub-channel are demodulated independently. The bandwidth of each sub-channel is designed much smaller than the coherent bandwidth of the wireless channel

eliminating the use of complicated channel equalizers. Frequency overlaps are allowed between the N sub-carriers due to the orthogonal property resulting a very high frequency-efficiency, which can approach the Nyquist rate [17] [18]. OFDM offers a higher SNR than single carrier systems with respect to white noise because the noise bandwidth is much smaller for each sub-carrier. It is robust to narrow-band time varying interference by dropping the affected sub-carriers. OFDM modulation and demodulation are normally realized by the use of IFFT (Inverse Fast Fourier Transformation) and FFT (Fast Fourier transformation).

However, the peak-to-average ratio is high because the signals in each sub-carrier may add in-phase. Normally, the PA needs to work at 6 to 10 dB back-off from its 1-dB compression point in order to keep the amplitude information, which reduces the power efficiency. In the receiver, it is required to have a precise phasing of the demodulating carrier and accurate sampling times in order to keep the cross-talk between sub-channels small [18]. This is very critical in a single chip solution. A summary of different modulation schemes is listed in table 2.1 [10]. In OFDM systems, the data-rate depends on the modulation scheme in each sub-carrier, and its relative SNR improvement is normally limited by the phase noise of the local oscillators.

Modulation schemes	Modulation Circuit Complexity	Demodulation Circuit Complexity	Clock Recovery	IF Circuity Complexity	Relative SNR Improvement
ASK/OOK Envelope	Low	Lowest	No	Lowest	Reference (0)
FSK Coherent	Medium	High	Yes	Lowest	-4.7 dB
BPSK	Low	Medium	Yes	Lowest	-6.1 dB
QPSK	Medium	High	Yes	Low	-6.1 dB
MSK	High	High	Yes	Low	-6.1 dB
OFDM	Highest	Highest	Yes	Low	TBD

Table 2.1. Comparisons of modulation schemes.

2.3 Transceiver architectures

Complexity and robustness are the main concerns in choosing a transceiver architecture. It is favorable to use one LO frequency in both transmitter and receiver in order to reduce the component count, thus a reduction in chip area and cost. The major candidates are homodyne, heterodyne and dual IF architectures. Clearly, the dual IF solution is the most complicated architecture, and it is not an option in a millimeter-wave single-chip solution.

2.3.1 ZIF transceiver

A homodyne transceiver, also called Zero-IF (ZIF) or direct-conversion, has the lowest complexity, which directly modulates the carrier frequency with the base-band signals. A typical ZIF transceiver front-end architecture is shown in figure 2.2. In a ZIF receiver, the RF signal is split into two mixers driven by LO signals with a phase difference of 90-degree. LO frequencies are tuned to the RF frequency. Its outputs are IQ base-band signals. In a ZIF transmitter, IQ signals are directly up-converted to the carrier frequency by using the same LO frequencies, and then they are added together to form the RF signal. The cost and power consumption of a ZIF transceiver are reduced due to the smaller number of building blocks. Filter requirements are relaxed in a ZIF receiver because the channel selection filters are replaced by LPFs, which are compatible with IC designs. However, the performance is compromised due to some issues specially related to a ZIF transceiver, e.g. DC offset, LO leakage and even-order distortions. Many techniques can be used to mitigate these problems [13]. In a ZIF transmitter, it is of great importance to have a good isolation between the output port and the LO port of the mixer. The output of the PA has the same carrier frequency as the LO and its amplitude is high. Its leakage to the local oscillator may cause the problem of injection locking.

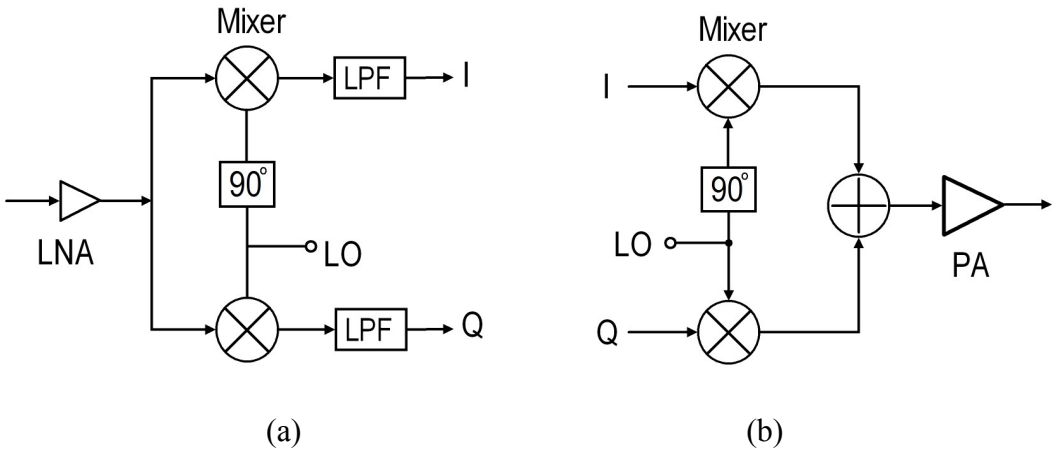


Figure 2.2. ZIF transceiver architecture, (a): receiver, (b): transmitter.

2.3.2 Heterodyne transceiver

A heterodyne receiver down-converts the RF signal to an intermediate frequency before converting it to base-band signals, where AC coupling can be used to eliminate the DC-offset problem. RF filters are used to suppress the out-of-band signals, and IF filters are used for channel selection within the band, because it is easier to realize a high selectivity BPF at a low frequency than at an RF frequency. The transmitter is realized by an IF modulator followed by an up-converter. The heterodyne system is the most robust transceiver architecture and has been widely used in wireless transceivers. Therefore, we adopt it in our first design of the 60 GHz transceiver. An important variation of the heterodyne transceiver is the sliding IF architecture, where one LO frequency is required and all other frequencies are derived by multiplying or dividing it [16]. In this work, the IF is chosen at 5 GHz, because it is compatible with the 802.11a WLAN standard.

2.4 Link budget analysis

The complete transmitter and receiver architectures used in this work are shown in figure 2.3 and 2.4. There are four chips in the transceiver system as shown in the figures. The main function of the receiver front-end is to convert the received 60 GHz RF signal to a 5 GHz IF. An LNA with sufficient gain is required in order to suppress the mixer noise. The LO signal is generated by a 56 GHz PLL which has a

fixed division ratio of 512. The IF chip of the receiver demodulates the 5 GHz IF signal. In the transmitter, the IF chip modulates the base-band signal to a 5 GHz carrier frequency and the FE chip up-converts the 5 GHz IF to the 60 GHz band. The same PLL as in the receiver FE is used to generate the LO signal. The up-converted signal is amplified by a buffer amplifier. Equation (2.1) is used to calculate the free-space loss. The white thermal noise power is calculated by:

$$ThermalNoise = kTB_n \ , \tag{2.7}$$

where k is Boltzmann's constant, T the absolute temperature and B_n the noise bandwidth. At a room temperature of 290 °K, it can be calculated in dBm as:

$$ThermalNoise = -174 + 10\log(B_n). \tag{2.8}$$

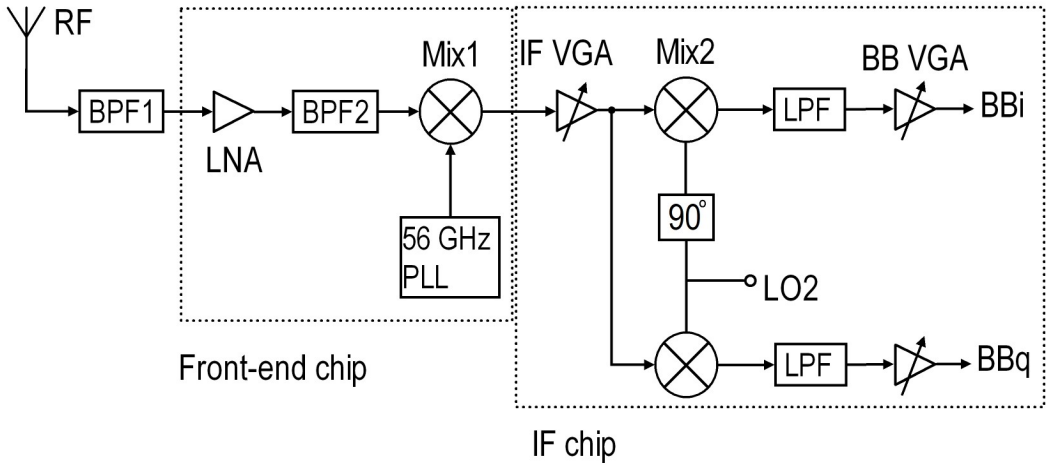


Figure 2.3. Receiver architecture based on the hererodyne principle.

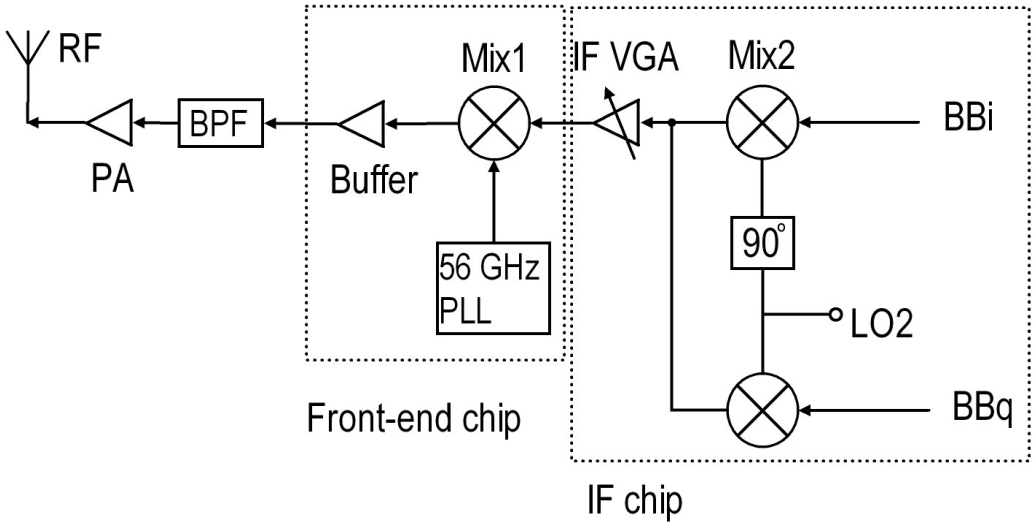


Figure 2.4. Transmitter architecture using the same LO frequency as the receiver.

In the receiver front-end, BPF2 is the frequency response of the LNA, and BPF1 is the frequency response of the antenna and packaging. In the transmitter, the BPF is realized on-board and is used to suppress the image frequency at around 50 GHz. In the link budget calculation, BPFs are not included. Their effects are incorporated into the amplifier frequency response and the packaging loss.

Non-linearity properties can be characterized either by P_1dB or by IP3. The empirical relationship between them is [19]:

$$P_{1-dB} \approx P_{IP3} - 9.6 \tag{2.9}$$

Total IP3 of a two-stage cascaded system is calculated by:

$$\frac{1}{P_{TotalIP3}} = \frac{1}{P_{IP3First}} + \frac{1}{P_{IP3Second}} \tag{2.10}$$

However, the 9.6 dB difference is not always true [20]. So we adopt P1_dB because it can be measured directly. The link budget for the receiver chips is listed in table 2.2, where IF chip is modeled by one block. The output linearity is limited by the IF demodulator because it starts distortion at an input power of –26 dBm. Noise figures are calculated according to the cascaded noise factor equation (3.16).

Blocks	Gain (dB)	Noise figure (dB)	Pout_1dB (dBm)
LNA	18	6.8	3
Mix1	4	14	-5
IF demodulator	26 to 50	20	1
Total	48 to 72	7.6	1

Table 2.2. Link budget summary of receiver chips.

In transmitter design, linearity is the main concern. An external commercial PA was planned after the transmitter FE chip. However, it is not used in the first demonstrator because it oscillates with the bond-wire inductances. The link budget of the two transmitter chips is listed in table 2.3, where the IF modulator is modeled as one block.

Blocks	Gain (dB)	Pout_1dB (dBm)
IF modulator	0	-12
Mix1	-2	-15
Buffer	20	3
Total	18	3

Table 2.3. Link budget summary of transmitter chips.

In order to analyze the dynamic range, several assumptions have to be made, i.e. antenna gain, packaging loss and modulation scheme. A 10 dB gain of the on-board Vivaldi antenna is assumed in this analysis. Packaging losses for both receiver and transmitter are assumed to be 3 dB. To simplify the analysis, single-carrier QPSK is used and its bandwidth is 500 MHz. The whole system with air interface is depicted in figure 2.5, where the LOS distance is assumed to be one meter and the packaging loss includes both the bond-wires and the on-board transmission lines. This analysis does not include the external PA and the on-board filter. The base-band output signal of the receiver at the lowest gain configuration is:

$3_{TX} - 3_{Packaging} + 10_{Ant} - 68_{Channel} + 10_{Ant} - 3_{Packaging} + 48_{Rx} = -3dBm$.

The VGA in the receiver chain needs a 3 dB higher gain to deliver a 0 dBm output power required by the AD converter. It has a gain margin of 21 dB, which is equivalent to more than 10 times distance. That is, the same output level can be achieved at a distance of 10 meters.

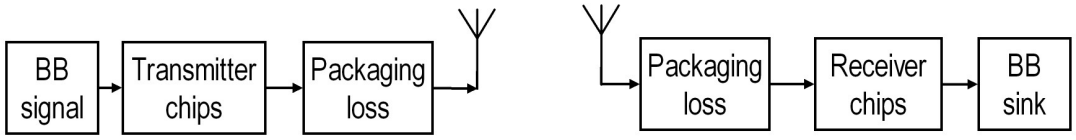


Figure 2.5. Transmitter and receiver with one meter air link.

However, if we look at the input of the LNA, the noise floor is:

$-174 + 10\log\left(500 \times 10^6\right) + 3_{Packaging} + 7.6_{Rxnoise} = -76.4dBm$.

With a LOS distance of 1-meter, the received power in front of the LNA is –51 dBm, which implies a maximum SNR of 25.4 dB. To demodulate a QPSK signal, a

minimum SNR of about 10 dB is required. So the maximum transmission distance is less than 6 meters. The system is limited by the white noise. To overcome this problem, the received signal level before the LNA has to be increased by either using a high power PA or high-gain antennas. With respect to noise-floor aspects, OFDM has better performance provided the phase-noise is sufficiently low.

If we look into table 2.2, the 60 GHz FE has an input P_1dB of –47 dBm corresponding to a LOS distance of 0.6 meter with the same output power at the transmitter. In order to work within 0.6 meter, the IF VGA needs more tuning range or the transmitter needs to transmit less power. At the current chip specifications, the expected transmission range is from 0.6 meter to 6 meters for the assumed QPSK system.

Summary

This chapter covers the system level issues. The wireless channel response at the 60 GHz band is reviewed in the beginning of the chapter. All the published channel responses from different sounding systems indicate that the delay spread is much smaller than those of the 2.5 GHz band and the 5 GHz band. The high free-space loss limits the communication range at 60 GHz. However, it has a special advantage of reducing in-band interference due to the fast fading. The 60 GHz wireless signal is well restricted within a room because of its high penetration loss. The popular modulation schemes proposed for the 60 GHz band have been briefly reviewed. OFDM has an advantage in the presence of multi-path signals, which is well suited for WLAN applications. Transceivers for single-carrier modulation schemes have simple hardware and relaxed phase-noise requirements of the LO signals. They are suited for point-to-point transmission systems. A very-low-cost transceiver can be built with a ZIF architecture because it has the least component count. But it suffers from many problems, so that its performance is compromised. The heterodyne architecture is robust and is chosen in this work. The transceiver system is characterized in the link budget analysis. This transceiver system is limited by the noise floor in a single-carrier giga-bit-per-second system. OFDM has better performance if the phase noise can be made sufficiently low.

Chapter III Basic Theories of Building Blocks

The basic LNA and mixer design theories will be reviewed in this chapter. An LNA can be considered as a small-signal linear two-port-network (TPN) due to the small signal imposed at its input. All LNA design issues are explained in frequency domain by the use of S-parameters, which include stability, power gain and noise figure. Both K-B and μ factors can be used to evaluate LNA stability, but μ factor is more preferable because of its simplicity and physical meaning. Constant gain circles and constant noise circles are very useful graphical tools in the tradeoff between gain and noise figure. When they are plotted within one Smith chart [21], the tradeoff becomes very intuitive. A mixer is a non-linear circuit because of the frequency transformation. Its design is based on time domain arguments. The simulation engines of mixers are either transient or harmonic balance (HB). HB is more convenient in that it treats signals in polar format facilitating the impedance matching issues. Mixer topologies will be reviewed including passive diode mixers and active mixers. Each of them has its own advantage and is used in some specific applications. The first part of the chapter summarizes the basic LNA theory and the second part the mixer theory.

3.1 LNA design theory

3.1.1 Amplifier stability

It is desirable for an amplifier to work with different source and load impedances without any oscillation. Under such conditions, an amplifier is called unconditionally stable. Otherwise it is conditionally stable. For an unconditionally stable system, the reflected power must be less than the incident power, which indicates there is no extra energy flowing back to the source from the amplifier. Figure 3.1 shows a TPN with the reference directions of signals and of reflection coefficients. First of all, the reflection coefficients at port1 and port2 must be obtained.

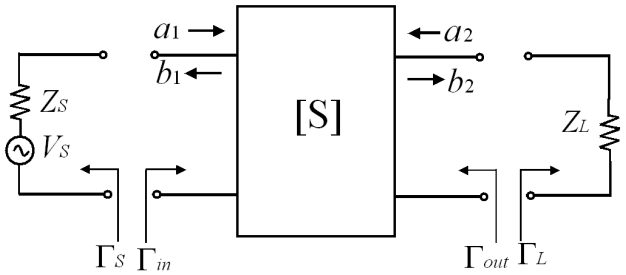


Figure 3.1. TPN with reference directions of signals and reflection coefficients.

From the S-parameter and the reflection coefficient definitions, $\Gamma_L = a_2/b_2$ and $\Gamma_S = a_1/b_1$, the input reflection coefficients Γ_{in} and Γ_{out} are:

$$\Gamma_{in} = \frac{b_1}{a_1} = s_{11} + \frac{s_{12}s_{21}\Gamma_L}{1 - s_{22}\Gamma_L} = \frac{s_{11} - \Delta\Gamma_L}{1 - s_{22}\Gamma_L} \quad (3.1a).$$

$$\Gamma_{out} = \frac{b_2}{a_2} = s_{22} + \frac{s_{12}s_{21}\Gamma_S}{1 - s_{11}\Gamma_S} = \frac{s_{22} - \Delta\Gamma_S}{1 - s_{11}\Gamma_S} \quad (3.1b),$$

where $\Delta = s_{11}s_{22} - s_{12}s_{21}$.

And after inversion of (3.1a) and (3.1b), we find:

$$\Gamma_L = \frac{s_{11} - \Gamma_{in}}{\Delta - s_{22}\Gamma_{in}} \quad (3.2a).$$

$$\Gamma_S = \frac{s_{22} - \Gamma_{out}}{\Delta - s_{11}\Gamma_{out}} \quad (3.2b).$$

For an unconditionally stable amplifier, the reflection coefficients Γ_{in} and Γ_{out} must be within the unity circle. By setting $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$, and manipulating them, the unconditional stability condition is given [22]:

$$K = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta|^2}{2|s_{12}||s_{21}|} > 1 \quad (3.3a)$$

$$|s_{12}s_{21}| < 1 - |s_{11}|^2 \quad (3.3b)$$

$$|s_{12}s_{21}| < 1 - |s_{22}|^2 \quad (3.3c),$$

and K is known as the stability factor. Under the condition of (3.3a), (3.3b) implies (3.3c) and vice versa. $K > 1$ together with any of (3.3b) and (3.3c) are the sufficient and necessary conditions of unconditional stability. In most of the cases, the K-factor

alone can be used to guarantee an unconditional stability since the other two conditions normally can be satisfied.

An alternative is the *K* and *B* combinations. *K* is the same as defined in (3.3a). Another two parameters, B_1 and B_2, are [23]:

$$B_1 = 1 + |s_{11}|^2 - |s_{22}|^2 - |\Delta|^2 \tag{3.4a}$$

$$B_2 = 1 + |s_{22}|^2 - |s_{11}|^2 - |\Delta|^2 . \tag{3.4b}$$

The unconditional stable conditions become

$$K > 1 \text{ and } B_1 > 0 \tag{3.5a}$$

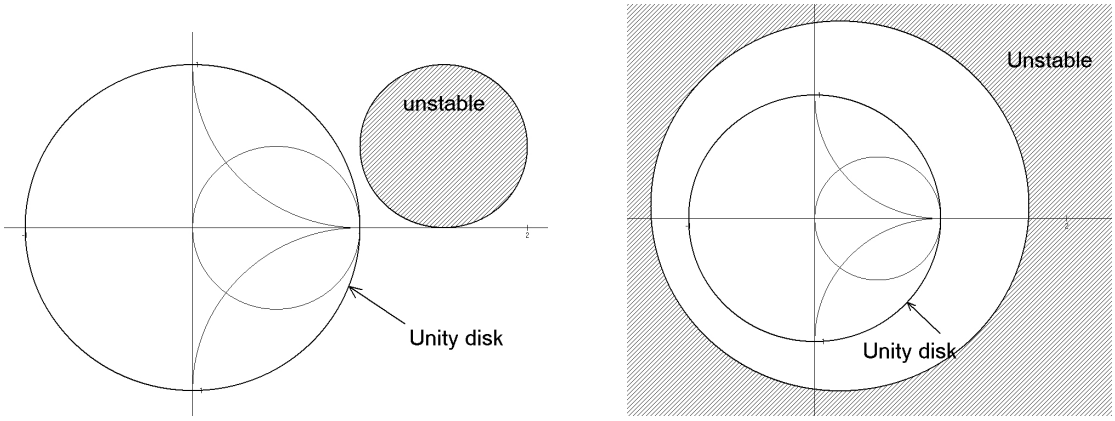
$$\text{or } K > 1 \text{ and } B_2 > 0 . \tag{3.5b}$$

The *K-factor* method has been widely deployed in many simulation tools to ensure an unconditional stable amplification, and is proved to be very useful. However, *K-factor* alone is not able to judge the stability of a TPN. It requires an auxiliary condition either from (3.3) or (3.4), and it does not give any physical insight into the TPN.

Another way of judging the stability of a TPN is the μ-parameter method [24]. The μ-parameter is defined as:

$$\mu = \frac{1 - |s_{11}|^2}{|s_{22} - s_{11}^* \Delta| + |s_{21} s_{12}|} . \tag{3.6}$$

μ > 1 is a sufficient and necessary condition of unconditional stability. The μ-parameter is derived geometrically from the mapping of the equations in (3.1) and (3.2). In (3.1), the load and source reflection coefficients, Γ_L and Γ_S are mapped into input and output reflection planes. And their inverses, (3.2), make an opposite mapping process. Note that all the reflection coefficients of passive loads are within a unity circle. A unity smith chart (USC), representing all load impedances, can be mapped back to Γ_{in} plane resulting in another disk area and vice versa because the transformation is bilinear. While mapping Γ_{in} to Γ_L plane, there are eight possibilities [25]. Two mapping possibilities of unconditional stability are shown in figure 3.2 [24].



(a) (b)

Figure 3.2. Two unconditional stability mappings from Γ_{out} to Γ_S plane. (a) with the unstable region a disk outside the USC and (b) with the unstable resion a disk complement encircling the USC.

The radius and center of the mapped circles in figure 3.2 are:

$$r_S = \frac{\left|s_{21}s_{12}\right|}{\left|\left|s_{11}\right|^2 - \left|\Delta\right|^2\right|} \tag{3.7a}$$

$$C_S = \frac{s_{11}^* - s_{22}\Delta^*}{\left|s_{11}\right|^2 - \left|\Delta\right|^2} \tag{3.7b}$$

$$c_S = \left|C_S\right| \tag{3.7c}.$$

This circle is known as load stability circle. In the same way, we can derive source stability circles. These circles are useful tools when designing the source and load matching circuits because they give a graphical insight of the potential unstable source and load impedance regions. The μ factor is defined as the minimum distance in Γ_S-plane between the center of the USC and the unstable region:

$\mu = c_S - r_S$ in figure 3.2(a) and

$\mu = r_S - c_S$ in figure 3.2(b).

If μ is greater than unity, not only does it tell us that the two-port network is unconditionally stable, but it also tells us how large the design margin is according to the quantity of the μ-factor. Because of its simplicity and physical meaning, the μ-factor method is the most preferable way in judging the stability of a TPN.

In case of conditional stable devices, conjugate matchings at both input and output are not possible. However, it is possible to conjugate match it at one side. The method described in [25] can be used. In an LNA design, the input needs to be matched. Its maximum gain is bounded by

$$G_{OL} = g_{ol}|S_{21}|^2 = \frac{2k}{|S_{12}S_{21}|}\cdot|S_{21}{}^2|. \quad (3.8).$$

3.1.2 Power gains and constant gain circles

There are three commonly used power gains, transducer power gain G_T, power gain G_p (also called operating power gain) and available power gain G_A. They are defined as:

$$G_T = \frac{P_L}{P_{AVS}} = \frac{\text{power delivered to the load}}{\text{power available from the source}},$$

$$G_p = \frac{P_L}{P_{IN}} = \frac{\text{power delivered to the load}}{\text{power input to the network}},$$

$$G_A = \frac{P_{AVN}}{P_{AVS}} = \frac{\text{power available from the network}}{\text{power available from the source}}.$$

The expressions of these power gains are [23]:

$$G_T = \frac{1-|\Gamma_S|^2}{|1-\Gamma_{in}\Gamma_S|^2}|s_{21}|^2\frac{1-|\Gamma_L|^2}{|1-s_{22}\Gamma_L|^2}, \text{ or} \quad (3.9a)$$

$$G_T = \frac{1-|\Gamma_S|^2}{|1-s_{11}\Gamma_S|^2}|s_{21}|^2\frac{1-|\Gamma_L|^2}{|1-\Gamma_{out}\Gamma_L|}, \quad (3.9b)$$

$$G_p = \frac{1}{1-|\Gamma_{in}|^2}|s_{21}|^2\frac{1-|\Gamma_L|^2}{|1-s_{22}\Gamma_L|^2}, \quad (3.10)$$

$$G_A = \frac{1-|\Gamma_S|^2}{|1-s_{11}\Gamma_S|^2}|s_{21}|^2\frac{1}{1-|\Gamma_{out}|^2}. \quad (3.11)$$

From their definitions, it is clear that G_T is a gain including both the input and output mismatches, whereas G_p assumes a conjugate match at the input, and G_A at the output. Rearranging (3.11) with the use of (3.1b),

$$G_A = \frac{|s_{21}|^2\left(1-|\Gamma_S|^2\right)}{\left(1-\left|\frac{s_{22}-\Delta\Gamma_S}{1-s_{11}\Gamma_S}\right|^2\right)|1-s_{11}\Gamma_S|^2} = |s_{21}|^2 g_a \tag{3.12}$$

where $g_a = \frac{G_A}{|s_{21}|^2} = \frac{1-|\Gamma_S|^2}{1-|s_{22}|^2+|\Gamma_S|^2(|s_{11}|^2-|\Delta|^2)-2\,\mathrm{Re}(\Gamma_S C_1)}$

and $C_1 = s_{11} - \Delta s_{22}^*$.

For a given G_A, the locus of Γ_S is a circle centered at C_a with a radius of r_a, which are given by:

$$C_a = \frac{g_a C_1^*}{1+g_a(|s_{11}|^2-|\Delta|^2)} \quad , \tag{3.13a}$$

$$r_a = \frac{\sqrt{1-2k|s_{12}s_{21}|g_a+|s_{12}s_{21}|^2 g_a^2}}{\left|1+g_a(|s_{11}|^2-|\Delta|^2)\right|} . \tag{3.13b}$$

This circle is known as the constant available-power-gain circle. A cluster of circles can be obtained by varying the value of G_A. They are normally plotted together with the constant-noise-figure circles because they all are functions of Γ_S. For a given source impedance, it is trivial to read out the noise figure and available gain of a TPN. The tradeoff between them becomes intuitive in a Smith Chart. This will be demonstrated in the chapter of LNA design. An example of available-power-gain circles together with noise circles is shown in figure 4.6.

In the same way, the constant power-gain circle can be obtained as a function of Γ_L for a given G_p. The constant power-gain circles are used together with a load-pull simulation for the co-optimization of gain and output power.

3.1.3 Noise of a TPN

3.1.3.1 Thermal noise

The noise presented to the input of a TPN has a lower limit, i.e. thermal noise or Johnson noise due to the thermal agitation. The power of the thermal noise is given as *KTB*, where *K* is Boltzmann's constant, *T* the absolute temperature and *B* the

bandwidth in Hz. For a bandwidth of B Hz, the noise power at a room temperature of 290 K is:

$$10\log(KTB) = 10\log(1.38\times10^{-23}\times290) + 10\log(B)$$
$$= -174dBm + 10\log(B)\,. \qquad (3.14)$$

Noise factor (F) and noise figure (NF) are used to evaluate the noise added by a TPN to a signal. They are defined as follows:

$$F = \frac{\left(S/N\right)_{input}}{\left(S/N\right)_{output}} \quad \text{and} \quad NF = 10\log(F)\,, \qquad (3.15)$$

where S/N is the signal to noise ratio (SNR).

3.1.3.2 Noise factor of a cascaded system

The noise factor of a cascade system is calculated by using the cascaded noise-factor equation [26]. A general form of Friis' equation is:

$$F = F_1 + \left(F_2-1\right)/G_1 + \left(F_3-1\right)/G_1G_2 + \left(F_4-1\right)/G_1G_2G_3 + \ldots \qquad (3.16)$$

where F_1 and G_1 are the first-stage noise factor and gain, F_2 and G_2 the second stage and so forth. Equation (3.16) tells us that the main noise contribution comes from the first stage, provided the gain of the first stage is high. The noise contribution of a building block is suppressed by the gain of the previous stages. However, if the first stage has a loss instead of a gain, the second stage noise contribution to the whole system is amplified because G_1 is less than unity.

When two amplifiers are cascaded as shown in figure 3.3, the noise-measure, M, is introduced to determine which amplifier should be placed first in order to achieve the lowest overall noise factor [22]. M of the i^{th} amplifier is defined as:

$$M_i = \frac{F_i - 1}{1 - 1/G_i} \qquad (3.17)$$

where F_i is the noise factor of the i^{th} stage and G_i the gain of the i^{th} stage.

The lowest noise figure can be achieved when the amplifier with a smaller M is connected as the first stage.

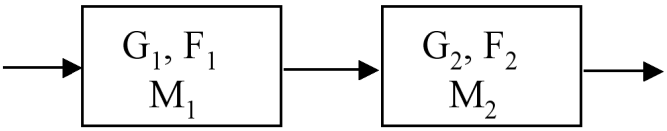


Figure 3.3. Cascaded two-stage amplifier.

3.1.3.3 Constant noise figure circles

A noisy two-port network can be modelled as a noise-free two-port network with a voltage noise source and a current noise source at the input, which is depicted in figure 3.4 [27]. The separation of the noise sources from the TPN makes them independent of the network response facilitating noise analysis.

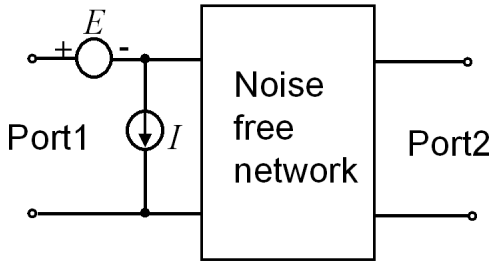


Figure 3.4. Noisy two-port network representations.

Noise factor or noise figure is sensitive to source admittance. There is an optimum source admittance, which gives the lowest noise factor, Fmin. This source admittance is called Y_{opt}. Any mismatch of source admittance increases the noise factor. Noise factor can be expressed as follows [27]:

$$F = F_{\min} + \frac{R_n}{G_S}\left|Y_S - Y_{opt}\right|^2 = F_{\min} + \frac{R_n}{G_S}\left[\left(G_S - G_{opt}\right)^2 + \left(B_S - B_{opt}\right)^2\right], \qquad (3.18)$$

F_{min} is the minimum noise factor of the two-port network. $Y_S = G_S + jB_S$ is the source admittance of the measurement system. $Y_{opt} = G_{opt} + jB_{opt}$ is the optimum source admittance. R_n is the noise resistance, which denotes how fast the noise factor increases from F_{min} as the source admittance departs from Y_{opt}. From (3.18), the locus of a constant-noise-factor or a constant-noise-figure is a circle in a rectangular source admittance plane. It is convenient to convert this circle to a Smith Chart plot for the co-optimization with gain and stability. A bilinear transformation is applied to (3.18) to transform the circle from a rectangular plane to a Smith chart [28]. Y_S and Y_{opt} have the following relations with the corresponding source reflection coefficients,

$$Y_S = \frac{1-\Gamma_S}{1+\Gamma_S} \text{ and } Y_{opt} = \frac{1-\Gamma_{opt}}{1+\Gamma_{opt}}. \tag{3.19}$$

Equation (3.18) is re-expressed by the use of (3.19) as,

$$F = F_{\min} + \frac{4R_n\left|\Gamma_S - \Gamma_{opt}\right|}{\left(1-\left|\Gamma_S\right|^2\right)\cdot\left|1+\Gamma_{opt}\right|^2}. \tag{3.20}$$

For a fixed noise factor F (F>Fmin), rearrange equation (3.20) as:

$$\left|\Gamma_S - \frac{\Gamma_{opt}}{1+N_i}\right|^2 = \frac{N_i^2+N_i\left(1-\left|\Gamma_{opt}\right|^2\right)}{\left(1+N_i\right)^2}, \tag{3.21}$$

where $N_i = \frac{F_i - F_{\min}}{4R_n}\left|1+\Gamma_{opt}\right|^2$.

Equation (3.21) is a circle in Γ_S plane centered at

$$C_F = \frac{\Gamma_{opt}}{1+N_i},$$

and its radius is

$$r_F = \frac{1}{1+N_i}\sqrt{N_i^2 + N_i\left(1-\left|\Gamma_{opt}\right|^2\right)}.$$

A set of circles is obtained by varying the value of the noise factor. They are normally plotted together with the available-power-gain circles on one Smith Chart to determine the tradeoff between NF and gain. An example of constant-noise-figure circles is shown in figure 4.6, which is at 60 GHz for the npn200_8 transistor in IHP's 0.25 um SiGe BiCMOS technology.

3.1.4 LNA design procedure

The basic LNA design issues have been discussed in the previous sections. A general LNA design procedure is given in this section. It is not a straitforward procedure in that all the LNA specifications are related to each other either directly or indirectly. In general, several design iterations are needed.

Step 1: Select the appropriate transistors as the main amplifying devices according to the required LNA specifications. Main parameters are NFmin and maximum power gain.

Step 2: Investigate the stability of the transistor and stabilize it if necessary. This step can be omitted if the transistor is unconditional stable.
Step 3: Make a trade-off between noise figure and gain. Plot the constant-noise-figure circles and constant-available-gain circles at the operation frequency. The compromised source impedance is determined from this step.

Step 4: Design input and output matching networks. Match the input to the source impedance obtained in step 3 and conjugate match the output. Stability should be always checked during the matching procedure.

Step 5: Check if all the specifications are met. If not, re-optimize them and keep an eye on those parameters which have met the specifications.

Step 6: Design the bias networks. Test the stability and RF performance after the insertion of the bias networks. Bias networks should not affect RF performance nor stability.

Step 7: Layout the LNA using the results from the previous steps.

3.2 Mixer design theory

3.2.1 Basic mixer operation

A mixer is one of the key building blocks in a transceiver. In a heterodyne architecture, it transforms the input frequency to another frequency. In a ZIF architecture, mixers are used to modulate the base-band signals to the RF carrier frequency and demodulate the received RF signals. Fundamentally, mixers are multipliers. This is illustrated in figure 3.5. When two sinusoidal signals are applied to an ideal multiplier, two new frequencies come out of the multiplier according to trigonometry:

$$\cos(\omega_1 t) \bullet \cos(\omega_2 t) = \tfrac{1}{2} \{\cos[(\omega_1 + \omega_2)t] + \cos[(\omega_1 - \omega_2)t]\}. \qquad (3.22)$$

If one of the two input signals is modulated, the whole modulation band will be shifted. Filters are used to select one of the two mixing products. In figure 3.5, the lower side band is selected.

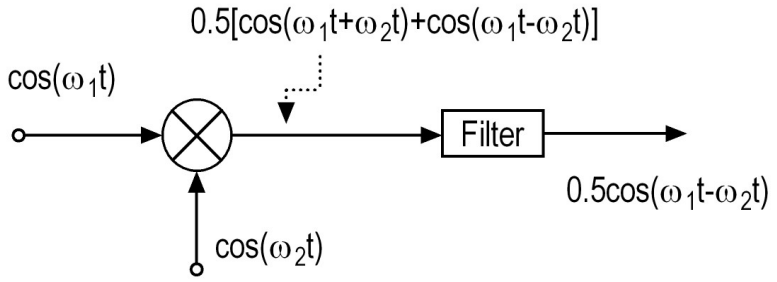


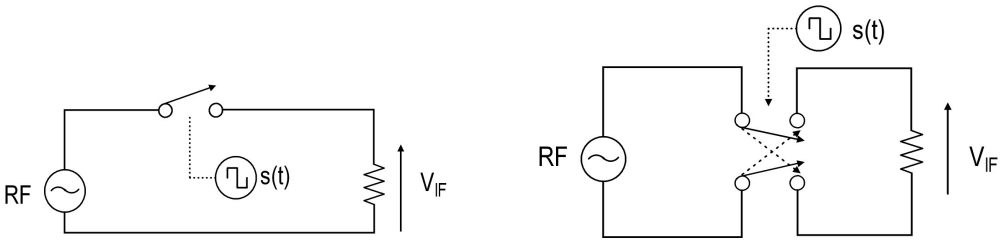
Figure 3.5. An ideal multiplier is used to shift frequency.

There are two ways to realize the signal multiplication. The first one is the use of non-linear devices, such as a diode. The I/V characteristic of a non-linear device can be described via a power series,

$$I = a_0 + a_1 V + a_2 V^2 + a_3 V^3 + ... \qquad (3.23)$$

If the input signal V comprises two different frequencies, the output current contains many combinations of the input frequencies, $m\omega_1 + n\omega_2$, where m and n are integer numbers. With a proper filter, the desired frequency can be filtered out from the rest.

Another way to realize a mixer is the use of a switch, as is shown in figure 3.6. In figure 3.6a, the switch interrupts the RF waveform periodically at LO frequency resulting the product of the two signals. Figure 3.6b is a balanced switch, where the signal polarity is changed instead of simply interrupting the RF signal. In this case, the output is a differential signal and it is robust to common mode noise.



(a) (b)

Figure 3.6. Mixers realized via switches.

3.2.2 Mixer architectures

3.2.2.1 Passive mixers

Diodes and FETs can be used to build mixers without DC supplies. They are called passive mixers. Schottky diodes have a very high cutoff frequency, and they are widely used in traditional microwave mixers. There are three common architectures in diode mixers: single device, singly balanced and doubly balanced. They are shown in figure 3.7.

The mixing effect in figure 3.7(a) fully depends on the non-linear I/V characteristics of the Schottky diode. Port-to-port isolations can only be realized through filters. In the singly balanced topology of figure 3.7(b), the LO signal is applied to the ground of RF and IF ports providing an inherit isolation. Figure 3.8 illustrates the operation of the singly balanced mixer with an 180-degree hybrid. The LO signal is applied to the delta port and it is out-of-phase across the two diodes, while the RF voltage is in-phase. Ideally, there is no LO signal at RF and IF port. The two diodes are switched on and off simultaneously by the LO pumping signal. This procedure is similar to figure 3.6(a) with the advantage of the improved LO isolation. The current definitions are shown in figure 3.8(b). With the use of (3.23), they are written as:

$$I_1 = a_0 + a_1(V_{LO} - V_{RF}) + a_2(V_{LO} - V_{RF})^2 + a_3(V_{LO} - V_{RF})^3 \ldots \quad (3.24)$$

$$I_2 = a_0 + a_1(V_{LO} + V_{RF}) + a_2(V_{LO} + V_{RF})^2 + a_3(V_{LO} + V_{RF})^3 \ldots \quad (3.25)$$

$$I_{IF} = I_2 - I_1 = 2a_1V_{RF} + 4a_2V_{LO}V_{RF} + 6V_{LO}^2V_{RF} + 3V_{RF}^3 + \ldots \quad (3.26)$$

In equation (3.26), there is no LO output term and many terms in (3.25) and (3.24) have been canceled out. The product of $V_{LO}V_{RF}$ is the desired operation, from which the frequency shifting is realized. However, the RF frequency appears at the output. In normal operation, the RF signal is weak and is well separated from the IF frequency. It can be easily filtered out by the output filter. In case of a doubly balanced mixer, both RF and LO ports are isolated from the IF port suppressing their leakage [29]. However, this better isolation requires more LO power because the diode of diodes is doubled.

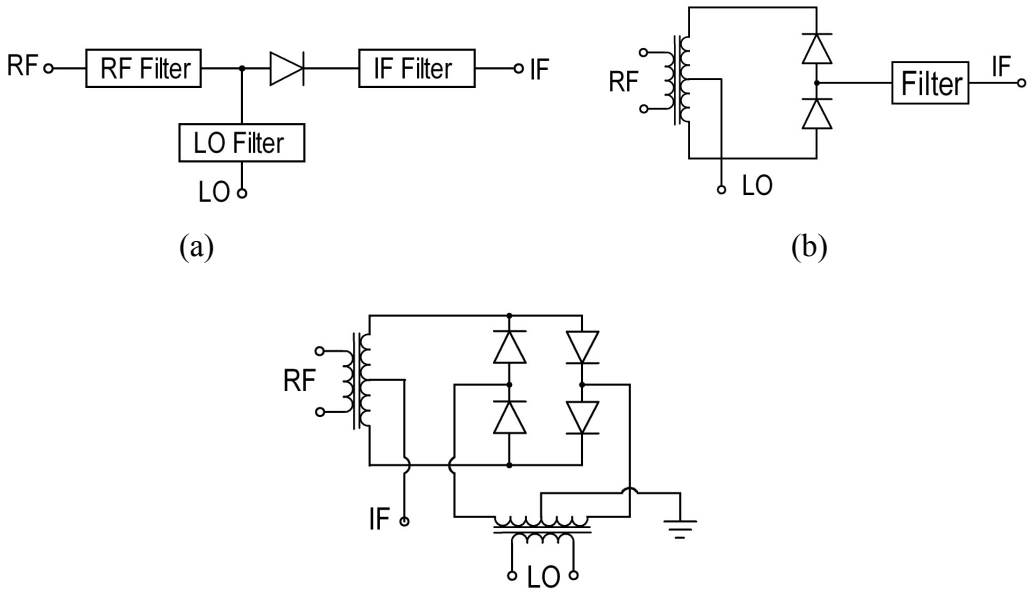


Figure 3.7. Three basic diode-mixer architectures [29]. (a) single device; (b) singly balanced; (c) doubly balanced.

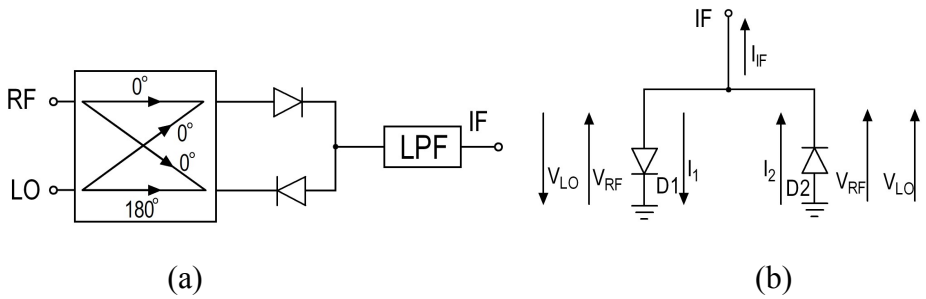


Figure 3.8. Single balanced mixer, (a) hybrid connection, (b) voltage and current definitions at the diodes and IF port.

Another interesting diode mixer is the subharmonically pumped mixer (SPM) [30] [31]. An anti-parallel diode pair (APDP) is used in this kind of mixers, e.g. figure 3.9. SPMs can use the second or fourth order harmonic of the LO frequency as the pumping signal, which significantly reduces the LO frequency facilitating the design of VCOs and PLLs. It has a comparable conversion gain as the fundamental tone pumped mixers. But the drawback is that three filters are needed to separate the three ports. Design details of subharmonically pumped mixers can be found in [32].

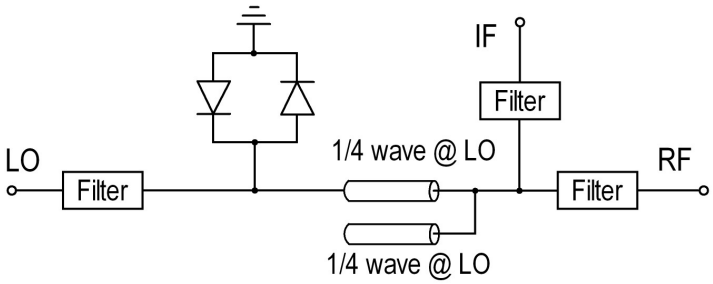


Figure 3.9. Subharmonically pumped mixer.

3.2.2.2 Active mixers

Besides the advantage of not requiring DC current, passive mixers have lower noise figures and higher input linearity compared to active mixers. However, they have a conversion loss, which has to be compensated by introducing more gains in LNA or IF circuitry. The noises from later stages are amplified by the inverse of the mixer loss. Active mixers have conversion gains and require less LO power, so that they are the preferred mixer topology in integrated circuits.

Analogue multipliers can be used as active mixers by applying LO and RF to its two input ports. A two-quadrant multiplier is shown in Figure 3.10 [33]. The RF signal is directly applied to the base of the lower transistor due to its small amplitude in a wireless receiver. The currents flowing through the two load resistors are related to the LO differential input, V_{id}, by

$$Ic_1 = \frac{I_C}{1+\exp\left(-\frac{V_{id}}{V_T}\right)} \tag{3.27}$$

$$Ic_2 = \frac{I_C}{1+\exp\left(\frac{V_{id}}{V_T}\right)}. \tag{3.28}$$

The difference between the two output currents, which is proportional to the IF output signal, is then:

$$\Delta I = Ic_1 - Ic_2 = I_C \tanh\left(\frac{V_{id}}{2V_T}\right). \tag{3.29}$$

For a large V_{id}, the output current will be clipped to I_C and $-I_C$. I_C is proportional to the RF voltage as long as its amplitude is small. Thus a polarity switched version of the RF signal is obtained and the mixing operation is accomplished. When a differential LO signal is not available, this circuit can work in a single-ended configuration by applying the single-ended LO signal to one of the LO inputs and leaving the other LO input to a correct DC voltage. Due to the fact that the RF port requires a positive voltage, this topology is a two-quadrant multiplier.

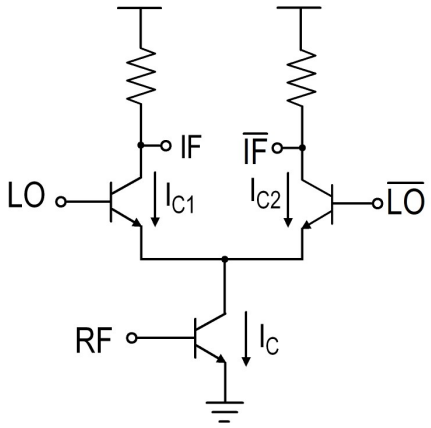


Figure 3.10. Two-quadrant analogue multiplier.

The Gilbert cell is a complete four-quadrant multiplier because both LO and RF signals are differential and centered at zero volt. When a Gilbert cell is used as a mixer, the lower differential pair is used as the small RF input and the higher switching transistors are used as the LO input. A Gilbert cell core is shown in figure 3.11, where the upper level transistors are mainly used to steer the currents delivered to the two load resistors. Mixers realized in the form of a Gilbert cell have the same property as a doubly balanced mixer in that RF and LO signals are canceled out at the IF port. Furthermore, the common mode noise coupled from adjacent blocks is suppressed due to the fully differential topology.

The current definition of the Gilbert cell mixer is also shown in figure 3.11. In order to analyze its operation, the currents are derived with respect to the input voltages [33]. Using (3.27) and (3.28), the collector currents of Q_3 to Q_6 are:

$$I_{C3} = \frac{I_{C1}}{1 + \exp\left(-\frac{V_{LO}}{V_T}\right)} \tag{3.30}$$

$$I_{C4} = \frac{I_{C1}}{1 + \exp\left(\frac{V_{LO}}{V_T}\right)} \tag{3.31}$$

$$I_{C5} = \frac{I_{C2}}{1 + \exp\left(\frac{V_{LO}}{V_T}\right)} \tag{3.32}$$

$$I_{C6} = \frac{I_{C2}}{1 + \exp\left(-\frac{V_{LO}}{V_T}\right)} \tag{3.33}$$

I_{C1} and I_{C2} are related to V_{RF} by:

$$I_{C1} = \frac{I_{EE}}{1 + \exp\left(-\frac{V_{RF}}{V_T}\right)} \tag{3.34}$$

$$I_{C2} = \frac{I_{EE}}{1 + \exp\left(\frac{V_{RF}}{V_T}\right)} \tag{3.35}$$

Combining (3.30) through (3.35), the expressions for collector currents I_{C3}, I_{C4}, I_{C5}, and I_{C6} in terms of input voltages are:

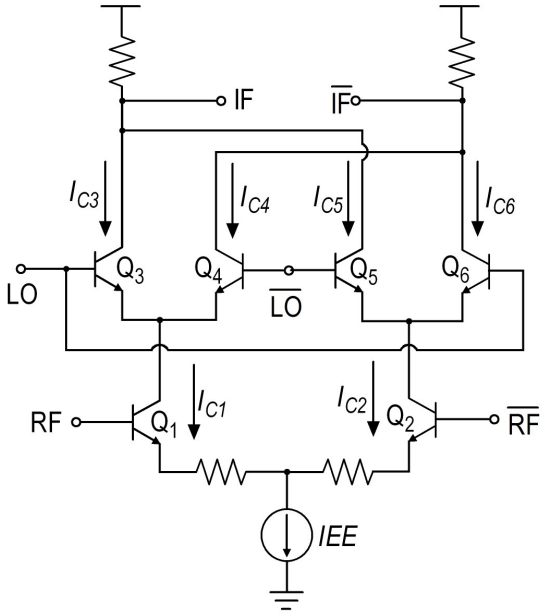


Figure 3.11. Gilbert cell mixer with current definitions.

$$I_{C3} = \frac{I_{EE}}{\left[1+\exp\left(-\frac{V_{LO}}{V_T}\right)\right]\left[1+\exp\left(-\frac{V_{RF}}{V_T}\right)\right]} \tag{3.36}$$

$$I_{C4} = \frac{I_{EE}}{\left[1+\exp\left(\frac{V_{LO}}{V_T}\right)\right]\left[1+\exp\left(-\frac{V_{RF}}{V_T}\right)\right]} \tag{3.37}$$

$$I_{C5} = \frac{I_{EE}}{\left[1+\exp\left(\frac{V_{LO}}{V_T}\right)\right]\left[1+\exp\left(\frac{V_{RF}}{V_T}\right)\right]} \tag{3.38}$$

$$I_{C6} = \frac{I_{EE}}{\left[1+\exp\left(-\frac{V_{LO}}{V_T}\right)\right]\left[1+\exp\left(\frac{V_{RF}}{V_T}\right)\right]}. \tag{3.39}$$

The differential current is given by

$$\begin{aligned}\Delta I &= I_{C3} + I_{C5} - (I_{C4} + I_{C6}) \\ &= I_{EE}\left[\tanh\left(\frac{V_{LO}}{V_T}\right)\right]\left[\tanh\left(\frac{V_{RF}}{V_T}\right)\right]\end{aligned} \tag{3.40}$$

If the LO power is high enough to switch the transistors completely on and off, and if the RF signal is small, the term $\tanh\left(\frac{V_{LO}}{V_T}\right)$ becomes a square wave and the term $\tanh\left(\frac{V_{RF}}{V_T}\right)$ can be approximated by V_{RF}/V_T. The small RF signal is multiplied with I_{EE} and $-I_{EE}$ alternatively at the rhythm of the LO frequency. Assume the RF signal is $V_{RF}\cos(\omega_{RF}t)$, the equation (3.40) can be further developed by using a Fourier series expansion for the difference current

$$\begin{aligned}\Delta I &= I_{EE}\sum_{n=1}^{\infty} A_n V_{RF}\cos(n\omega_{LO}t)\cos(\omega_{RF}t) \\ &= I_{EE}\sum_{n=1}^{\infty}\frac{A_n V_{RF}}{2}\left[\cos(n\omega_{LO}+\omega_{RF})t + \cos(n\omega_{LO}-\omega_{RF})t\right]\end{aligned} \tag{3.41}$$

where $A_n = \dfrac{\sin\left(\frac{n\pi}{2}\right)}{\frac{n\pi}{4}}$.

Thus the RF signal is transformed to the two sides of the LO frequency and its harmonics. There are no outputs at the LO and RF frequencies nor at their harmonics.

3.2.2.3 Image rejection mixers

The mixer architectures discussed above shift the input frequency into two sidebands centered at the LO frequency. Each of them contains complete information. One way of removing one sideband is the use of filters (band-pass, band-stop or notch filters). However, it is not possible to filter out the image to a satisfied degree in a low-IF or ZIF transceiver architecture. Another way is the use of an image-rejection-mixer (IRM), e.g. figure 3.2. The working mechanism of an IRM is based on the Hilbert transformation. It can be intuitively explained in the time domain. Assuming the RF signal is $\cos(\omega_{RF}t)$ and the LO signal is $\cos(\omega_{LO}t)$, we can derive the IF output as:

$$S_{IF} = \cos(\omega_{LO}) \cdot \cos(\omega_{RF}) + \sin(\omega_{LO}) \cdot \sin(\omega_{RF}) = \cos((\omega_{LO} - \omega_{RF})t). \quad (3.42)$$

In (3.42), the lower sideband is taken. Upper sideband can be taken by changing the sign of the upper mixer:

$$S_{IF} = \cos(\omega_{LO}) \cdot \cos(\omega_{RF}) - \sin(\omega_{LO}) \cdot \sin(\omega_{RF}) = \cos((\omega_{LO} + \omega_{RF})t). \quad (3.43)$$

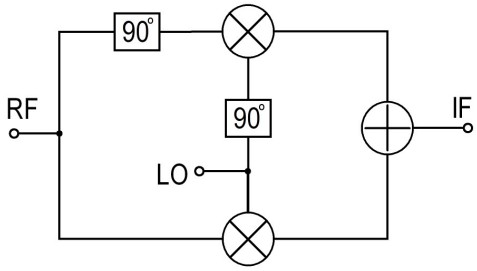


Figure 3.12. Image rejection mixer.

3.2.3 Mixer noise

The most common noise sources in a mixer are shot noise and thermal noise. Shot noise is generated in a PN or Schottky junction because its current consists of a series of pulses that occur as each electron crosses the junction. If the transit time is short compared to the inverse of the operation frequency at which the noise is

evaluated, the current waveform can be treated as a series of random impulses. This is a random noise process [29] with an average of DC current. The mean-square shot-noise current in a forward-biased diode is

$$\overline{i^2} = 2qI_j B, \tag{3.44}$$

where q is the electron charge, I_j the real part of the current across the junction, and B the bandwidth.

Both thermal noise and shot noise are white Gaussian processes when the diodes or transistors carry DC currents only. Therefore, noise processes are uncorrelated at different frequencies. Under LO excitation, thermal noise remains constant because the series resistance is time invariant. However, shot noise is changed to a pulsed waveform because of the change in the junction current. The pulses are located at the LO frequency and its harmonics. As shown in figure 3.13, the shot noise is mixed up and down to every other mixing frequency. As a result, the shot noise at different frequencies is correlated with each other complicating the noise analysis.

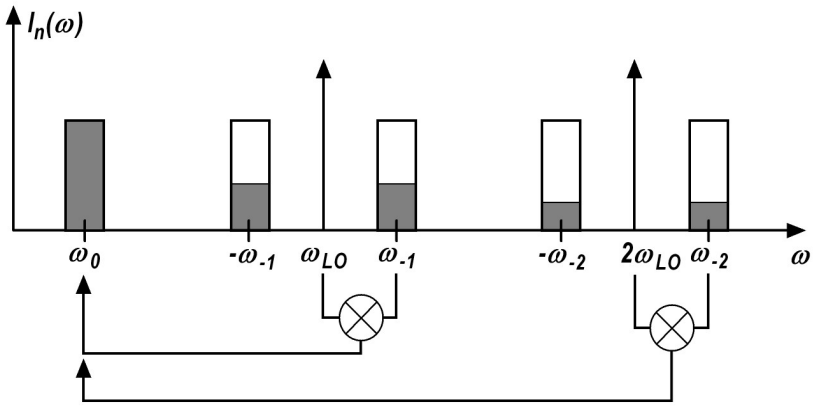


Figure 3.13. Shot noise at different frequencies is correlated due to the presence of an LO pumping signal [29].

The noise figure of a mixer is defined as the ratio of the noise temperature generated within the mixer to the ambient temperature. The single-side-band (SSB) noise-figure is defined by IEEE as:

$$F_{SSB} = \frac{T_{SSB}}{T_0} + 1. \tag{3.45}$$

3.2.4 Mixer simulation and optimization

3.2.4.1 Mixer simulation

Small signal linear solvers can not be used in a mixer simulation due to the large pumping LO signal. The most often used solvers are transient and harmonic balance [34] simulation. If the IF frequency is much lower than the RF and LO frequencies, simulation time is rather long in a transient simulation because many RF and LO cycles have to be simulated for one complete IF cycle. This makes HB more efficient than transient simulation. Another favourable feature of HB is that it treats signals in the form of amplitude and phase in the frequency domain. The input impedances of the three ports at different frequencies can be easily calculated by the ratio of port voltages and currents, which facilitates the impedance matching of the three ports.

It is assumed that a steady state can always be reached if a circuit is stimulated by a steady sinusoidal signal. An HB simulation is developed as an iteration of successive guess-and-tries. An initial guess sets the currents flowing out of each node. The current flowing into those linear components, i.e. passive components and distributed components, are calculated in the frequency domain. The currents flowing into those non-linear components are calculated in the time domain and transformed back to the frequency domain after the calculation. At each node, they are summed at all base-tones and their harmonics. If Kirchoff's current law (KCL) is satisfied, the convergence is reached. If not, an error is calculated, and a modified guess is given. A new iteration is to be carried out. HB solvers converge only at steady state, which do not give any transient information.

3.2.4.2 Mixer optimization

The optimization techniques in different mixer topologies are different. In diode mixers, the mixing operation happens when the conductance and capacitance of the diode is modulated by the large LO pumping signal. At different frequencies, the diodes have different impedances. This will influence the voltages and currents along the diodes. To improve the conversion gain and noise figure, the correct terminations at LO and its harmonics are of special importance.

In an active mixer design, the mixing operation happens when RF current is switched between the two loads. For each individual switching transistor, the impedance is also modulated by the LO signal. But in an active mixer design, taking a Gilbert cell as an example, there are more degrees of freedom in optimizing its performance such as DC voltages and currents. Furthermore, different ports are isolated from each other due to the topology, so the optimization of harmonic terminations is not common in an active mixer design. A detailed Gilbert mixer design will be carried out in the chapter on mixer design.

Summary

The basic theories of the design of transceiver building blocks have been reviewed in this chapter, including LNA design and mixer design. The LNA design issues are derived based on the linear two-port-network theory, which include stability, gain and noise figure. Both K and μ factors can measure the stability of a TPN. The K-factor is used in conjunction with an auxiliary condition and the μ-factor alone can judge the stability of a TPN. Constant-noise-figure circles and constant-available-gain circles are of great help in an LNA design, they give a detailed insight in the tradeoff between the noise figure and gain. There is no straightforward way in designing an LNA. Its design procedure usually requires several iterations.

The fundamental operation of a mixer is modeled as a switch. Passive mixers are usually realized by the use of diodes or FETs, and they are categorized in three classes: single-diode mixers, singly-balanced mixers and doubly-balanced mixers. An active mixer has a conversion gain and requires less LO power, so that it is the preferred mixer topology in an IC design. Most of the active mixers are based on multipliers. The operation mechanisms of a two-quadrant and a four-quadrant multiplier have been discussed. In mixer simulation, HB is the preferred simulation engine due to the advantage of less simulation time and easy impedance maching. The method of the mixer optimization depends on the used mixer topology.

Chapter IV LNA Design

LNA design theory has been summarized in the previous chapter. This chapter will cover its implementation issues. The technology used in the LNA design has been introduced in the chapter of introduction, which is a 0.25 micrometer SiGe:C BiCMOS process. A low-cost 60 GHz transceiver can be built in this technology with an acceptable performance. It is of great importance to design high performance on-wafer inductive matching components, such as transmission lines and inductors. Inductors realized in different structures will be compared in the used SiGe technology. The design details and measurement results of two LNAs will be given, i.e. a three-stage common-emitter LNA and a two-stage cascode LNA. In the end, a short summary concludes this chapter.

4.1 Passives

Passives include R, C and L components. In the used technology, the resistors and capacitors are standard components and well modeled. Some inductors working at low frequency range are also available. To work at 60 GHz, the inductors need to be designed and optimized. A tradeoff between Q-factor and chip area is to be determined from EM simulations.

4.1.1 Comparison of different types of inductors

One of the difficulties in designing integrated RF circuit is the low quality factor (Q-factor) inductors and transmission lines mainly due to the loss of the substrate, the very thin insulator layer and the DC resistance of the wire. Three types of inductors can be easily realized on-chip, which are metal-line (ML) inductors or coils, high-impedance transmission-line (MTL) inductors and coplanar waveguide (CPW) inductors. Their structures are shown in figure 4.1.

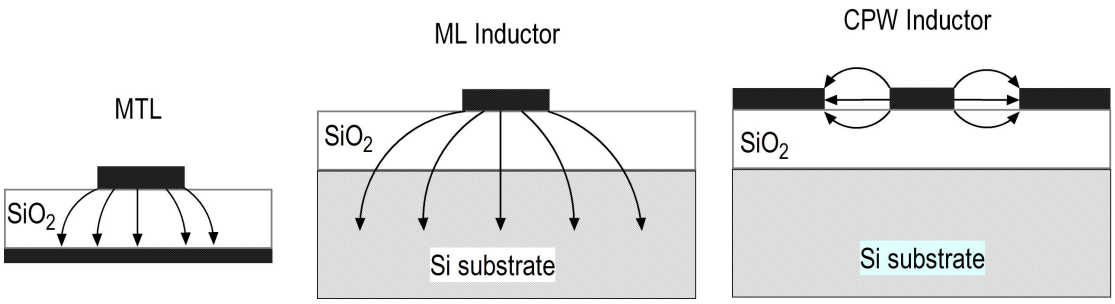


Figure 4.1. Three types of inductors and their electric field distribution.

ML inductors are realized with a wire or a coil without ground shield below the metal wire. MTL inductors are realized in the same way, but with a ground shield below the metal wire blocking the electric field from going into the lossy silicon substrate. CPW inductors shift the ground plane up to the same metal layer as the center conductor and let most of the electric field concentrate at the two slot regions reducing the loss due to silicon. In order to compare them, three 100 pH inductors are designed in the aforementioned three structures, all of them are optimized for high Q-factors at 60 GHz. These inductors are simulated in Momentum, a two and half dimension simulator in ADS. Figure 4.2 shows the Q-factors and inductances of the three inductors.

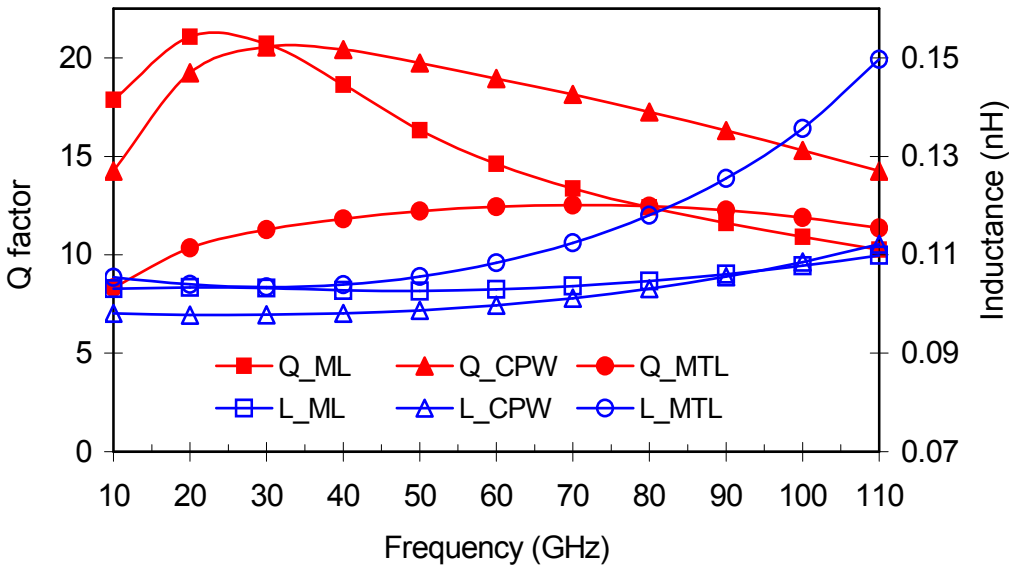


Figure 4.2. Q-factors and inductances for different inductors.

The Q-factor is calculated directly from its definition, i.e. the energy stored in the component and the energy lost in the component. To simplify the calculation, the

inductor is shorted to ground at one end. Its Q-factor and inductance are calculated by using the following equations:

$$Z_{11} = 50\frac{1+S_{11}}{1-S_{11}}$$

$$L = \frac{\mathrm{Im}(Z_{11})}{2\pi f}$$

$$Q = \frac{\mathrm{Im}(Z_{11})}{\mathrm{Re}(Z_{11})}.$$

The Q-factor and inductance are slightly different from those calculated by using Y parameter method. Since the inductors are used with one end grounded in the circuit, this calculation is more appropriate in this context.

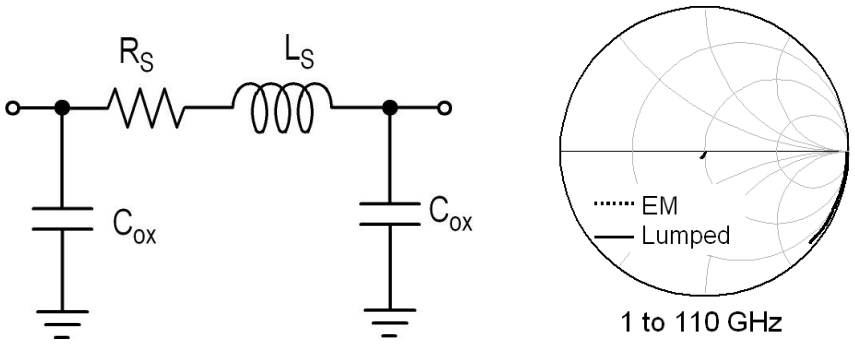
At low frequencies, the radiation is low and the DC resistance loss dominates the Q-factor. In Figure 4.2, the ML inductor has the highest Q-factor at frequencies below 30 GHz. This is because the ML inductor has the shortest length for a same inductance due to its low ground coupling. However, when frequency goes up, the loss increases because the EM field in the silicon substrate is increased resulting a quick drop in the Q-factor. At 60 GHz, it has a moderate Q-factor of 14. Although the ML inductor has the shortest length for a given inductance, it has to be used very carefully not to introduce any harmful coupling between each other. A separation of ten times distance of metal to silicon gives a less than -40 dB coupling factor. This will not create any area trouble in the used SiGe technology since the distance between the top metal layer and the silicon substrate is only 10 micrometers.

A high impedance MTL is used to create an MTL type inductor, which increases the DC resistance of the inductor. Even narrower line width is used, the capacitive coupling to ground is still high because the very thin substrate thickness. The substrate thicknesses are 4.26 um from Metal4 to Metal1 and 9.27 um from Metal5 to Metal1. A longer wire is demanded to achieve the same inductance as in the ML inductor. Its Q-factor is the lowest among the three types of inductors and its variation with frequency is small as shown in figure 4.2. However, the coupling between MTL inductors is low, which makes the integration easier. A rule of thumb: the separation between inductors is no less than three times of substrate thickness.

One more freedom, the ratio of line width to slot width, is introduced into CPW inductors, which allows a tradeoff between radiation loss and silicon loss. In order to limit the field within the two slots in a CPW inductor, narrower slots are used, which gives rise to capacitive coupling to ground. The length of the inductor is the longest. After optimization, the CPW inductor achieves the highest Q-factor of above 15 at 60 GHz at the expense of more chip area. However, CPW has to be used with care in integrated circuits because other transmission modes can be excited at discontinuities, e.g. slot-line mode [36]. CPW inductors have not been used in this work mainly due to the large chip area, which is a factor of 2 in length compared to ML inductors.

4.1.2 Lumped models of inductive components

Lumped models of inductors are constructed according to their physical structures. MTL inductors are modeled by using a Π network as shown in figure 4.3(a), where R_S models the resistive loss of the wire, L_S the inductance of the transmission line, and C_{OX} the capacitance to ground. All of the parameters are curve-fitted to 60 GHz. Skin effect is small, and is not considered in this model. As can be seen in figure 4.3(b), the lumped model matches the EM simulation very well from 1 to 110 GHz.

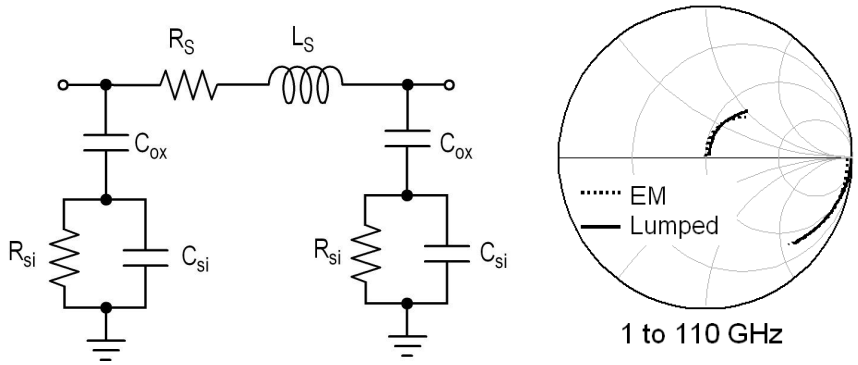


(a) (b)

Figure 4.3. MTL inductor lumped model, (a): lumped model and (b): S-parameters of the lumped model and EM simulation.

The lumped model for the ML inductor is shown in figure 4.4(a). The bridge capacitance in [35] is omitted because there is no under-path in the designed ML inductor. The parameters, R_S, L_S and C_{OX}, have the same physical meaning as those in

the MTL inductor but with different values. The silicon bulk is modeled by a parallel combination of a capacitor and a resistor. R_{Si} and C_{Si} are used to model the loss and the parasitic capacitance of the silicon bulk. Again in this model all the frequency variant effects, i.e. the skin effect of the conductor and the bulk frequency response, are not taken into account. The parameters are curve-fitted to 60 GHz. In figure 4.4(b), the lumped model matches EM simulation well from 1 to 110 GHz, and the highest accuracy is at 60 GHz.



(a) (b)

Figure 4.4. ML inductor lumped model, (a): lumped model and (b): S-parameters of the lumped model and EM simulation.

4.1.3 Bond-pad effect

As discussed in the previous section, silicon bulk contributes to the loss at high frequencies. The conventional unshielded bond-pad suffers from this loss. For a standard 100 um by 100 um bond-pad, the loss is as high as 0.8 dB at 60 GHz, which will be fully converted to the increase in noise figure. A ground metal shield below the bond-pad is used to remove this loss, which introduces a MIM capacitance between the bond-pad and the ground shield. However, if the input and output matching circuits can make use of this capacitance, it will not cause any mismatch problem.

4.2 Actives

LNA design starts from selecting the transistor with a high fmax, low NFmin and easy input matching impedance. In the used technology, the npn200 series

transistors are the best candidate. The eight-finger transistor, npn200_8, is selected for the LNA design. When it is biased at 5 mA, its NFmin is 4.5 dB and maximum gain is 7 dB at 60 GHz in a CE configuration, as shown in figure 4.5. The bias current of 5 mA is a tradeoff between NFmin and maximum gain. Reducing the current gives a smaller NFmin, but the transducer gain decreases as well. A V_{CE} voltage close to V_{CEO} is used in the simulation, at where the transistor has a high gain.

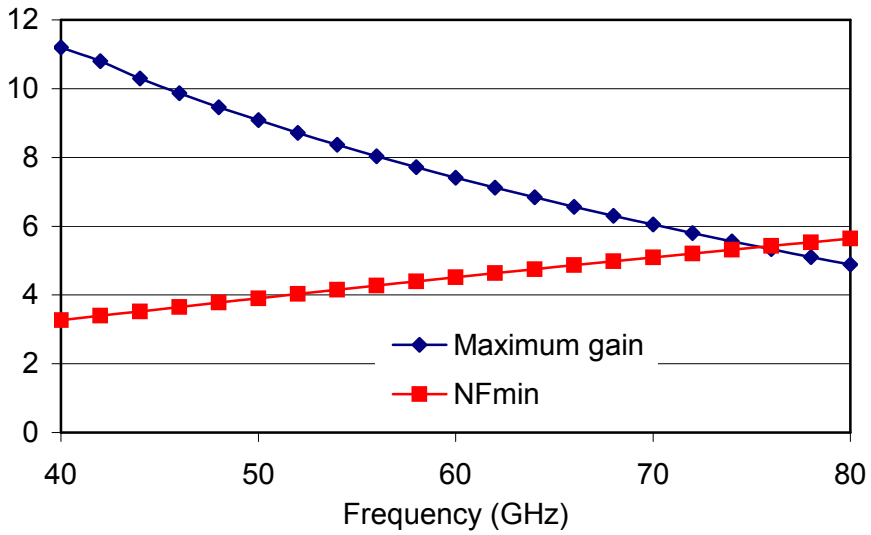


Figure 4.5. NFmin and G_T the npn200_8 transistor with a 5 mA I_{CE}.

In reality, optimum source impedances for noise figure and for conjugate matching are different. A compromise between noise figure and reflection loss is required. The constant-noise-figure circles and constant-gain-circles with respect to source impedances are plotted in figure 4.6. These circles are for the unmatched transistor npn200_8. The blue dotted circles are available-gain-circles with a gain step of 0.4 dB. The maximum available gain is 7.4 dB at the center of the available gain circles. The three circles are the source impedance loci for the available gains of 7.0, 6.6 and 6.2 dB, respectively. Constant-noise-circles are plotted in the Smith Chart with solid red lines with a step of 0.2 dB. At the center of the noise circles, a minimum NF of 4.5 dB is simulated, where it is the optimum noise matching point. The four noise circles stand for the source impedance loci of the noise figures of 4.7, 4.9, 5.1, and 5.3 dB. From figure 4.6, an optimum noise matching introduces a 1.2 dB loss in the available gain and a conjugate input match increases the noise figure by more than 0.8 dB. A compromise is made at the triangle marker, where the gain drops about 0.4 dB and the noise figure increases slightly higher than 0.2 dB. When real

components are used at the input and output, the performance will be worse than the above simulation, as will be shown in the following sections.

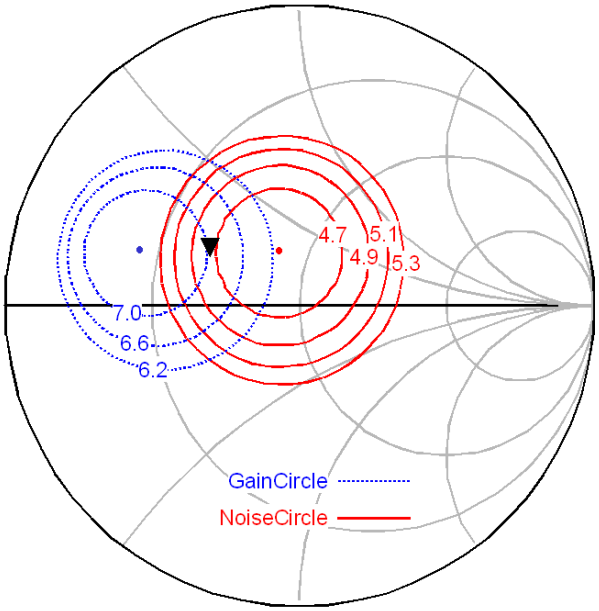


Figure 4.6. Noise circles and available gain circles of npn200_8 at 60 GHz.

Stability of the transistor is checked by both μ and K-B factors. They are plotted in figure 4.7. From both μ and K-B factors, the transistor is unconditionally stable at frequencies above 24 GHz. Stability is not a big concern in this design since the operation frequency is at around 60 GHz. Furthermore, the stability at low frequencies will be improved by the insertion of the input and output matching circuits as will be shown in the next section.

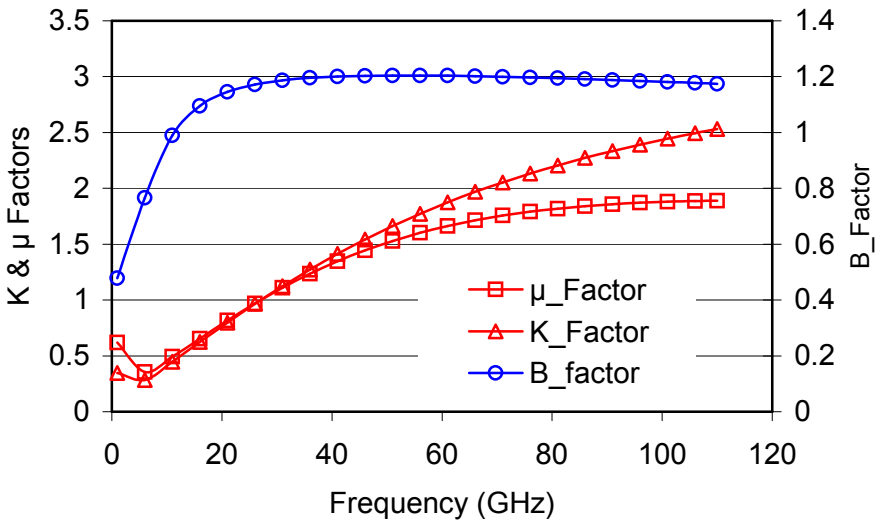


Figure 4.7. μ and K-B factors of npn200_8.

4.3 Design of a CE LNA

In order to deliver a gain of more than 15 dB, three stages are required in the LNA. The simplified LNA schematic is shown in figure 4.8, which is a three-stage differential CE LNA. A differential topology has a couple of advantages over a single ended one. Firstly, it has the property of rejecting common mode noise. Secondly, it is robust to bond-wire inductances. The bond-wire inductances may cause an oscillation in a single-ended amplifier even if the amplifier is designed unconditionally stable, because the chip ground is separated by an inductor from the packaging or board ground. If we assume the packaging or board ground is the real ground, AC voltage fluctuations exist on chip ground causing the amplifier potentially unstable. In a differential design, both negative and positive paths generate AC current fluctuations through the bond-wires. However, they are 180 degrees out-of-phase and equal in amplitude removing the AC current through the ground bond-wire, thus eliminating the oscillation potential.

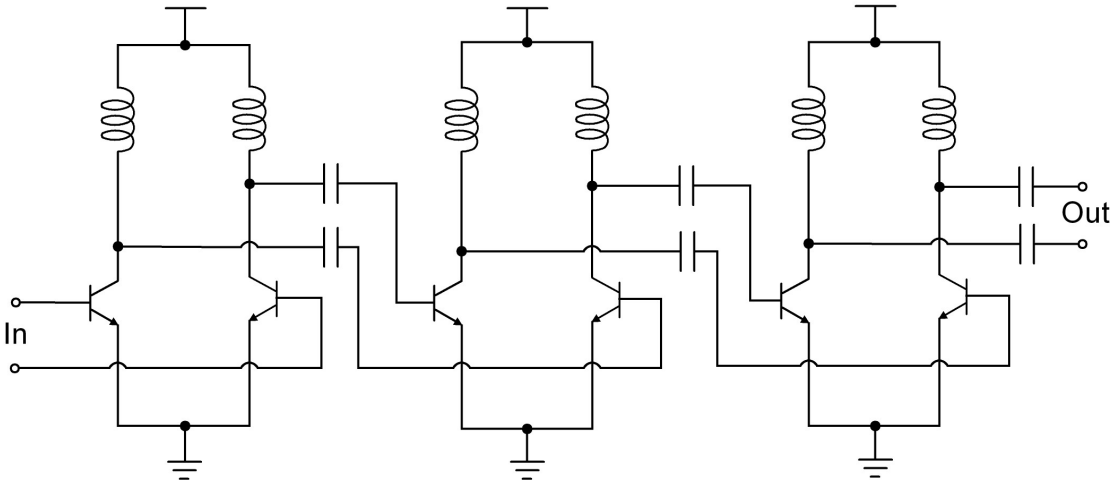


Figure 4.8. Simplified schematic of the three-stage CE LNA.

4.3.1 Input matching circuit

The half circuit of the input matching topology is shown in figure 4.9. The base bias inductor L_B, realized by an ML inductor, is integrated into the input matching circuit. C_1 is an AC decoupling capacitor providing an AC ground at the node V_B, where is the input point of the base bias voltage. The bias current flows through L_B and an MTL to the base of the transistor at V_b. Capacitor C_2 works as a

matching component and as a DC blocker. C_3 is the input bond-pad capacitance, which is used as a matching component instead of absorbing it into a CPW structure [37]. The MTLs are used for interconnections and separations of inductors.

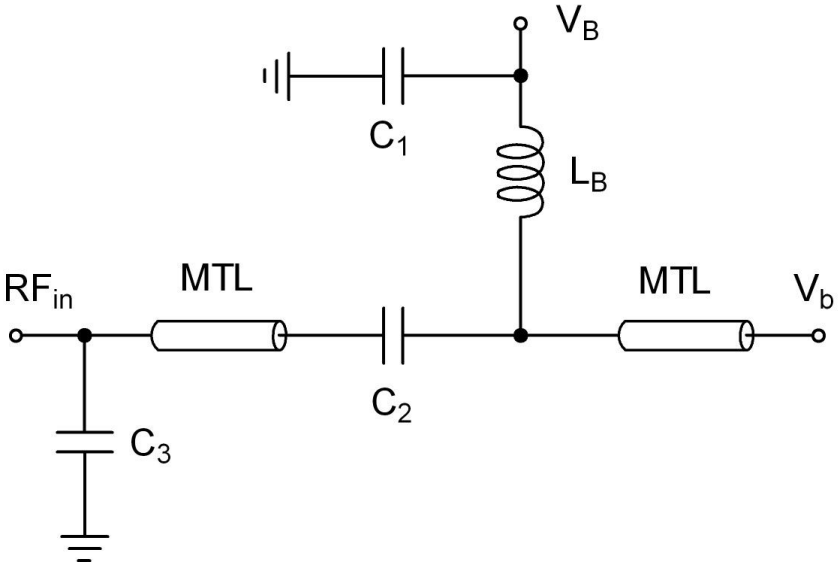


Figure 4.9. Half circuit of input matching topology.

After adding the real components to the input of the CE stage, let us check the constant-noise and available-gain circles again. They are plotted in figure 4.10, where the loci of the effects of the input matching components are also plotted. The MTL is the one between C_2 and C_3. The other MTL is omitted because of its very little effect. The empty marker is the compromised point in figure 4.6. Notice that the impedances shown in the smith chart are source impedances instead of transistor input impedances, i.e. the impedances are obtained by looking back to the source direction at the different points in the input matching circuit. For instance, the empty marker is the compromised source impedance at the base of the transistor. Because the bond-pad is ground shielded from the silicon bulk, the bond-pad capacitance will move the source impedance along the constant conductance circle of Smith Chart as shown by the line section of C_3. This determines that the LB and MTL combination has to bring the empty marker to the lower part of the 0.02 siemens constant conductance circle. After properly choosing the inductor value and transmission line length, they are shown as L_B and MTL sections.

The available gain and constant noise have the same steps as in figure 4.6, 0.4 dB and 0.2 dB. But their values are different because of the losses of the real

components. The maximum available gain drops to 6.9 dB from 7.2 dB, and NFmin increases to 5.3 dB from 4.5 dB. However, Γ_{opt} and S_{11}^* become closer from each other. At the tradeoff point of solid triangle marker, the available gain drops about 0.4 dB from its maximum value, and the noise figure increases less than 0.2 dB from NFmin.

K-B and μ factors are plotted in figure 4.11 after adding the input matching circuit. The CE stage becomes unconditionally stable from 1 to 110 GHz. Stability will be further improved after adding the real components at the output. The result of cascading two unconditionally stable networks is another unconditionally stable network. Stability issues will not be stressed in designing and optimizing the LNA.

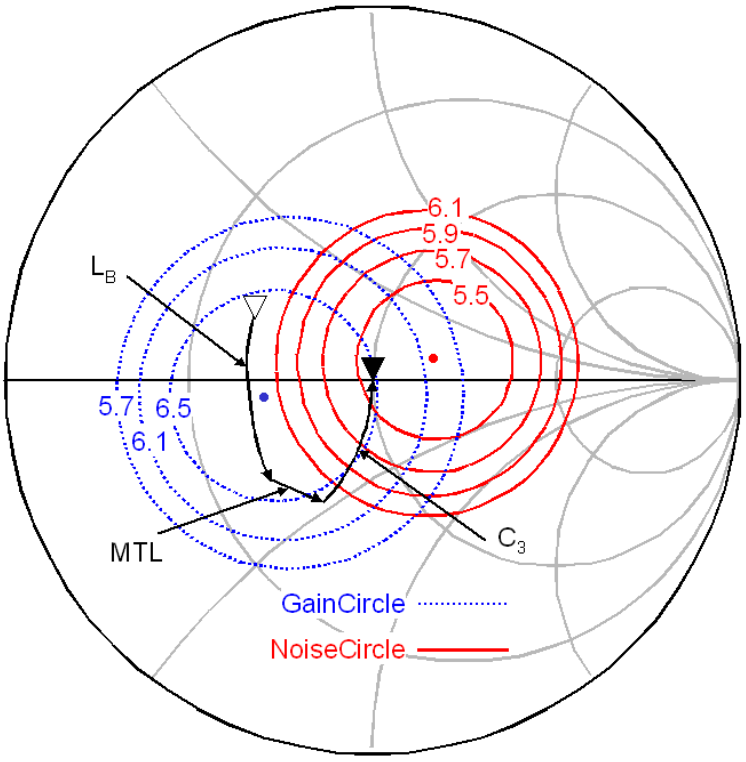


Figure 4.10. Constant noise circles (red solid curve) and constant gain circles (blue dotted curve) and the loci of the input matching components at 60 GHz.

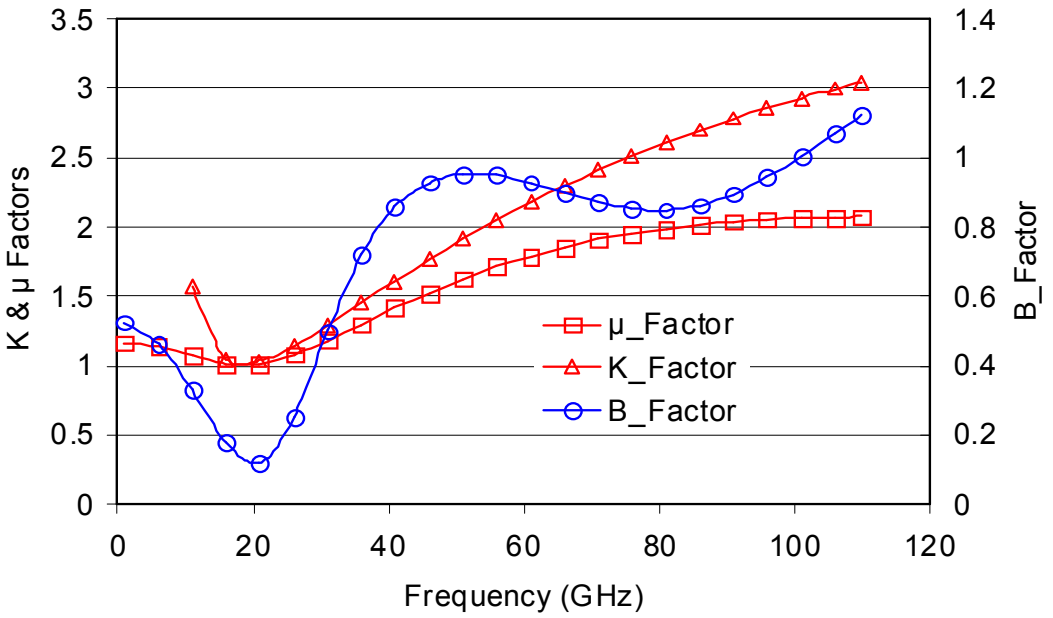


Figure 4.11. μ and K-B factors after adding the real input matching components.

4.3.2 Output matching circuit

The load matching networks for all stages share the same structure as shown in figure 4.12. A small resistor R_C is inserted between V_{CC} and the load inductance L_C to limit the collector current in case of malfunction and it also improves the stability at low frequencies. Capacitor C_1 provides an AC ground. L_C is the load inductor. C_2 is a matching capacitor and a DC blocker. MTL is used for the separation of inductors, which also gives a small phase shift. C_3 models the bond-pad capacitance at the output of the LNA, which does not exit in the first two stages. The output impedance is matched to 50 Ω for a single-ended signal, so that the differential impedance is 100 Ω. The output impedances of the first two stages are conjugate matched to the input impedance of the next stage to maximize the overall gain. After adding the load matching components, an extra loss on the same order of the input matching is introduced. We can get a plot of constant-available-gain circles by simply reducing 0.5 dB in figure 4.10. The constant-noise-figure circles barely change after adding the output matching components.

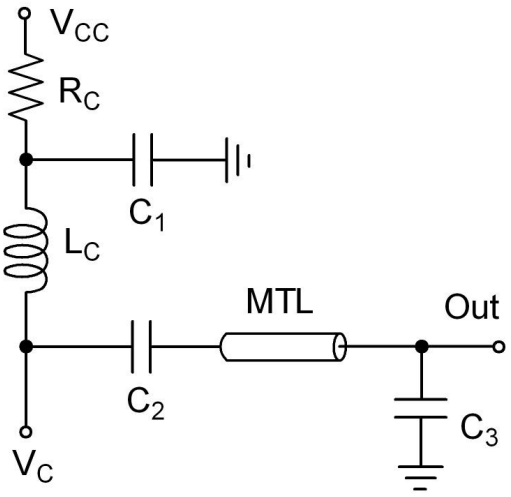


Figure 4.12. Half circuit of load matching network.

4.3.3 Bias circuit

Current mirrors are used for biasing the transistors. One of the biasing schematic is shown in figure 4.21. For a given voltage, the resistors set the current. The voltage at the collector of the diode-connected transistor is mirrored to bias the amplification transistor through a resistor. Three bias circuits are used to bias the three differential stages.

4.3.4 Experimental results of the CE LNA

Even though noise figure depends mostly on the first stage, the noise contribution from later stages can not be omitted because of the low gain in the first stage. In order to optimize the overall noise and gain performance, the collector currents are increased gradually from the first stage to the third stage, which are set to be 4, 5 and 6 mA, respectively. The overall noise figure is 6.8 dB after connecting all of the three stages together. Among this 6.8 dB, 4.5 dB is the NFmin, 0.8 dB is from the input matching, 0.2 dB is used to compromise with the gain and another 1.3 dB is from the second and third stages. The overall gain is 18 dB, contributed from the first to the third stages by 5.5 dB, 6 dB and 6.5 dB, respectively. The peak of the frequency response is designed at 60 GHz. This is achieved by conjugate matching the inter-stage to a frequency slightly higher than 60 GHz to compensate for the damping of the transistor trans-conductance, g_m.

The physical dimensions of the matching components and interconnections are laid out exactly the same as in simulation. Via is treated as a short in simulation because a via-array of at least 6 standard vias is used in each inter-layer connection. A single-ended LNA is laid out first, and then it is copied upside down to make another half of the differential LNA. The tail current source is omitted in the design and the emitters are directly connected to ground for the reason of measurement, so that a single-ended network analyzer can measure the LNA without the use of an external balun.

The chip photo is shown in figure 4.13. The LNA occupies a chip area of 0.42 mm^2 (0.6 mm by 0.7 mm) with bond-pads and 0.2 mm^2 without bond-pads. It draws 30 mA from a 2.2 V DC supply. With a supply voltage variation from 1.6 V to 2.8 V, the gain variation is below 1 dB. The simulated and measured S-parameters are shown in figure 4.14. A wideband input matching is achieved both in simulation and in measurement. The measured S11 is below –17 dB from 45 GHz to 75 GHz. Simulation predicts the same value at around 60 GHz, where the models are perfectly fitted. In S21 measurement, a gain of 18 dB is obtained at the center frequency of 60 GHz, and it has a 3-dB bandwidth of 22 GHz ranging from 49 to 71 GHz. The simulated gain agrees with measurement well in all frequencies. Within the 3-dB bandwidth, simulation predicts the exact value of measurement. Simulated reverse isolation, S12, also agrees with measurement within the 3-dB bandwidth. However, the measured and simulated S22 has a discrepancy, where the high output impedance of the collector is matched to an impedance of 100 Ω. The strong resonance in matching circuit amplifies the errors in the models of the active and passive components.

The measured and simulated K-B factors are shown in figure 4.15, where the frequency range is from 30 GHz to 110 GHz because the gain is below zero dB at other frequencies. The measured and simulated K factors agree with each other and all above unity. Both measured and simulated B factors are above zero. The combination of K-B factors guarantees the amplifier unconditional stable. The simulated and measured μ factors are shown in figure 4.16. Both are above unity in all frequencies implying an unconditional stable amplifier.

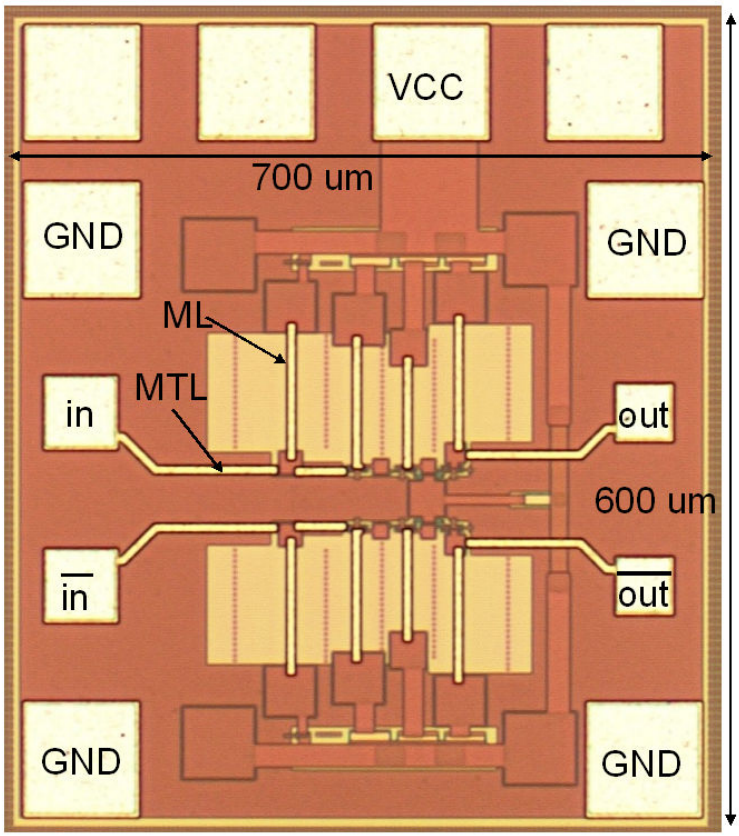


Figure 4.13. Chip photo of the CE LNA.

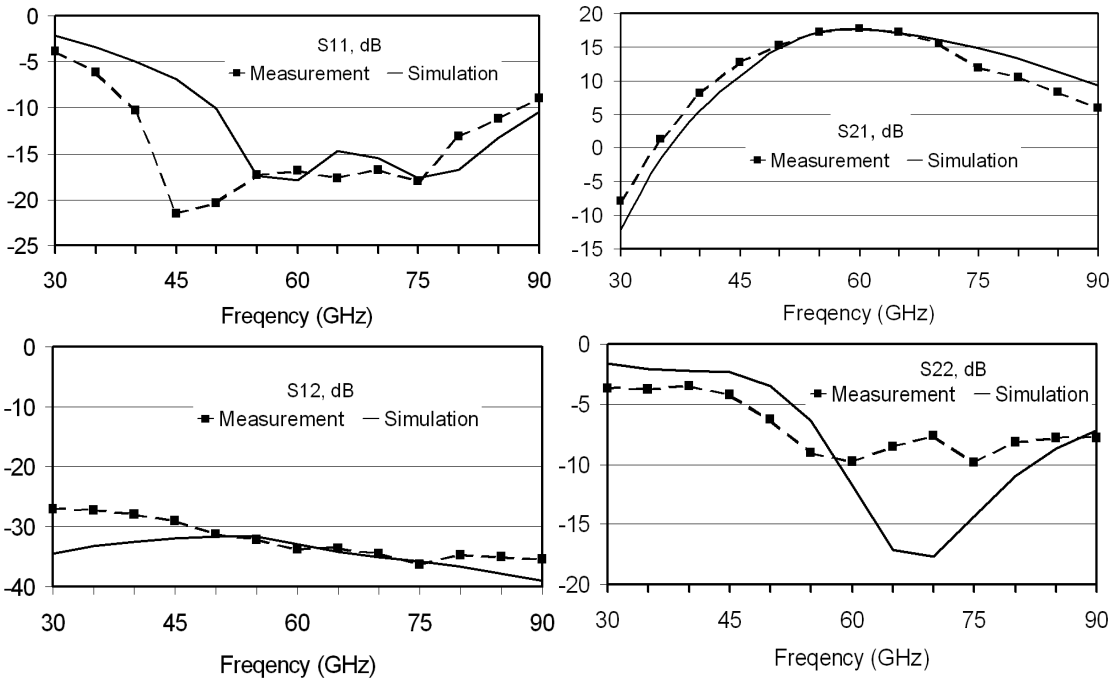


Figure 4.14. Simulated and measured S-parameters of the three-stage CE LNA.

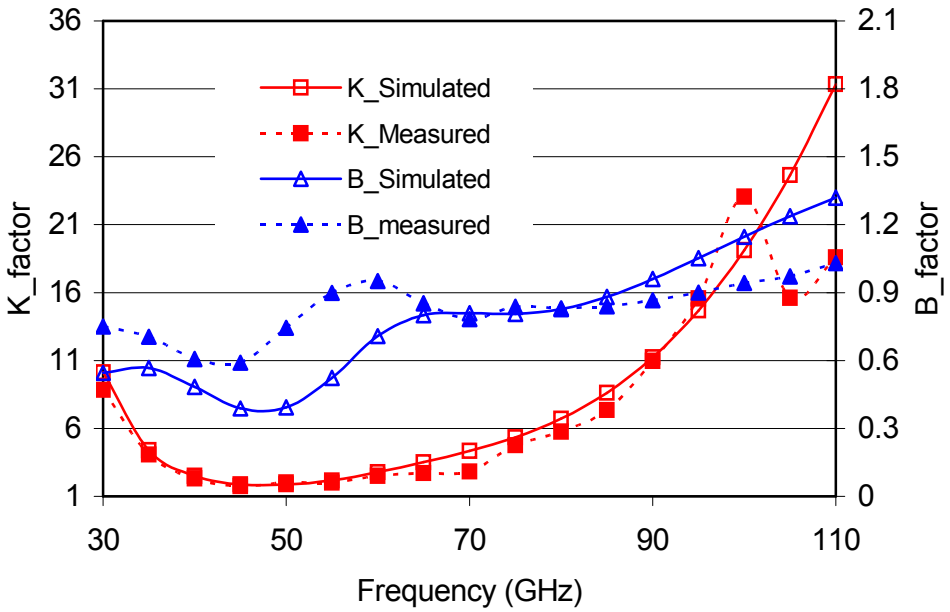


Figure 4.15. Simulated and measured K-B factor for the whole CE LNA.

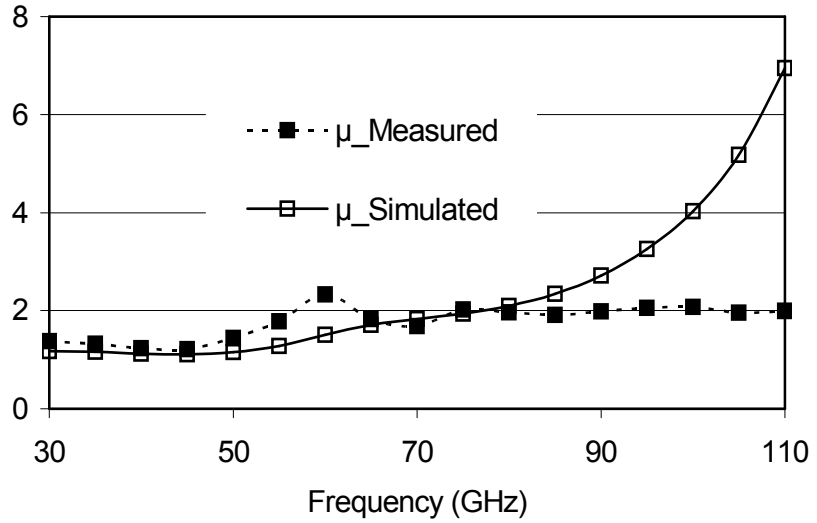


Figure 4.16. Simulated and measured μ factor of the whole CE LNA.

4.4 Design of a Cascode LNA

The previous CE LNA has achieved all the design targets. However, there are some parameters can be further improved, i.e. frequency response, gain and current consumption. A cascode LNA has been designed to improve these parameters. A cascode stage can deliver a higher gain than a CE stage because of the two amplification transistors. The lower transistor works as a CE stage transforming the

input voltage into its collector current. The upper transistor works as a CB stage amplifying the current from the CE stage. Both transistors share the same collector DC current.

4.4.1 Difficulties of on-chip filter implementation

In order to obtain a robust receiver, RF filters and image filters are the necessary components. There are two ways to realize a band-pass-filter (BPF): by the use of distributed coupling structures and by the use of lumped L-C components. At microwave frequencies, most filters are realized in coupling structures [21]. However, the performance of the metal structures in silicon technologies is not as good as that in printed circuit boards (PCB). The very thin silicon dioxide substrate between metal one and top metal layer gives rise to the line loss. Furthermore, it is difficult to obtain a strong coupling for the given design constraint. The minimum line spacing of top metal layer is 2 um in the used technology. In simulation, a third-order BPF coupling structure has an insertion loss of around 10 dB, which can not be placed before the LNA or even after the LNA due to its high attenuation.

By the use of lumped L-C components, a typical third-order BPF schematic is shown in figure 4.17, where two resonators are in parallel and one in series. The inductor and capacitor values are synthesized in ADS by specifying the damping factor and the number of orders. In this third-order filer, and damping factor is 18 dB per octave (6 dB for each resonator). However, the real problem comes after the synthesis. Some of the components are not realizable, i.e. inductors of a few nHs and capacitors of a few fFs. The self-resonant frequency of an on-chip inductor with an inductance of a few nH is much lower than 60 GHz. Although it is possible to realize a capacitor of a few fF, the tolerance would be very high because the parasitic capacitance of a line or a junction is on the same order. Clearly, the on-chip lumped filter is not feasible. However there is a way to circumvent, which is to integrate the filter response into an LNA.

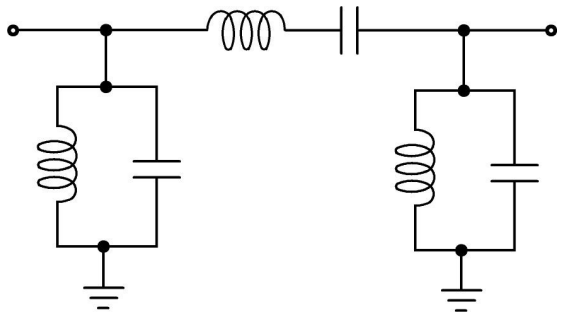


Figure 4.17. A lumped third-order BPF.

4.4.2 Optimization of LNA frequency response

To illustrate how a filter response can be integrated into an LNA, a CE stage with an inductive load is shown in figure 4.18, where we can replace VCC by a ground symbol for AC analysis. The load inductor L and the collector parasitic capacitance are in parallel, similar to the parallel resonator in figure 4.17. By tuning the inductor L and adding an extra capacitor parallel to the parasitic capacitance Cp, a parallel resonator is introduced. The two parallel resonators in figure 4.17 requires two stages. The series resonator can be obtained by optimizing the inter-stage matching components.

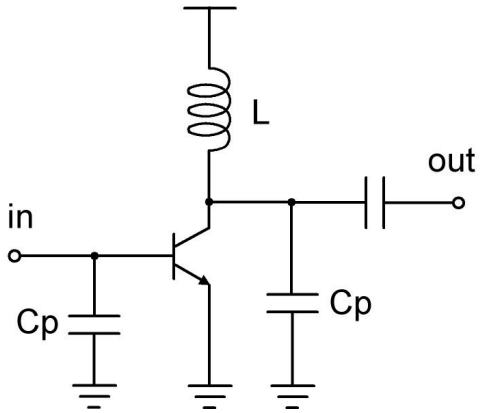


Figure 4.18. An inductive load CE stage with parasitic capacitance.

Another way of introducing a BPF response into an LNA is from impedance matching point of view. The collector output impedance is capacitive at RF frequencies. A parallel load inductor can compensate for the parasitic capacitance. If we introduce a smaller load inductor than needed, the output impedance becomes inductive along the constant conductance circle in an admittance Smith Chart. An extra parallel capacitor is then used to bring it back to resistive again. After this

procedure, a parallel resonator is introduced into the circuit and the output impedance is still under control. At inter-stage matching, a capacitor with a smaller capacitance is inserted to bring the output impedance of the first stage to be capacitive along the constant resistance circle in an impedance Smith Chart. Then a series inductor is used to bring it back to resistive along the same trajectory. By varying the different combinations of the matching components, different frequency responses can be realized. However, the gain drops after adding the on-chip matching components due to the low quality factors. Gain and frequency response have to be compromised.

The simplified schematic of the two-stage cascode LNA is shown in figure 4.19, where the resonators are marked out by those dashed boxes. Cp is the sum of the collector parasitic capacitance and the external matching capacitor. All inductors are realized in microstrip lines. Notice that the resonators are in the collector nodes of the two cascode stages and between the two stages, which have no significant influence on noise figure.

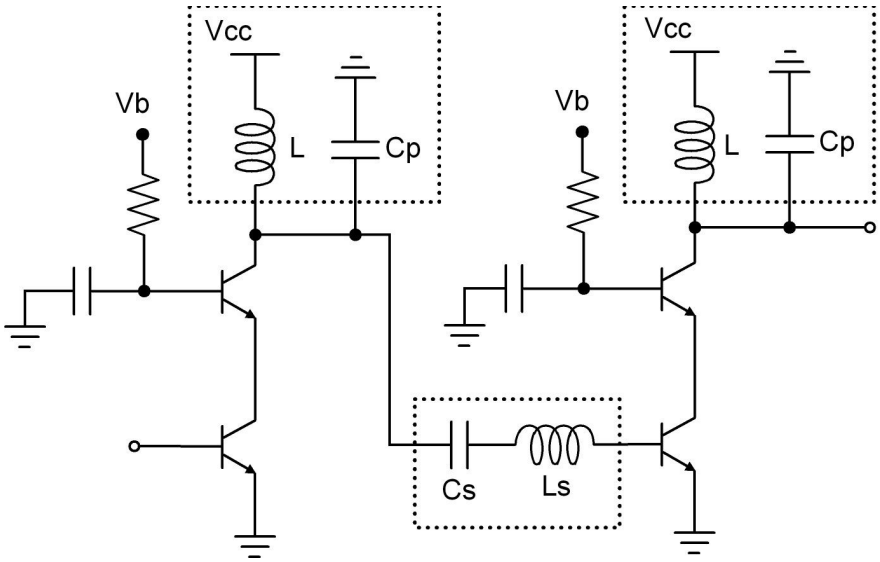


Figure 4.19. Schematic of the two-stage cascode LNA.

A detailed matching trajectory for the first parallel resonator and the series resonator is depicted in figure 4.20. The output impedance of the first stage without matching is shown as the empty triangle marker in the Smith Chart. After introducing the load inductor, L_1, in the first stage, the output impedance becomes inductive along the constant conductance circle, as shown in the figure. The external parallel

capacitance, C_{P1}, brings the output impedance to the point where it has the same real part as the input impedance of the second stage. After adding the serial capacitor, C_S, the output impedance becomes capacitive along the constant resistance circle. Then the serial inductor, L_S, brings the output impedance to the solid triangle marker, where is the conjugate of the input impedance of the second stage. The third resonator, at the collector of the second cascode stage, is realized in the same procedure. But it is optimized together with the output bond-pad to have an output impedance of 50 Ω. The frequency response is optimized to be maximal flat for a minimum in-band ripple and phase variation.

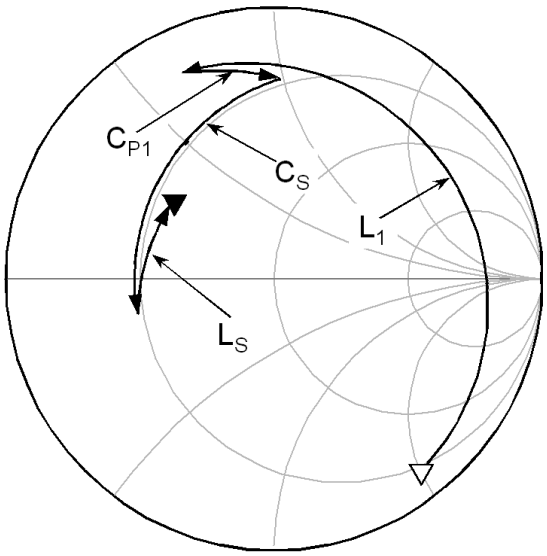


Figure 4.20. First-stage load and inter-stage matching trajectory of the two-stage cascode LNA at 60 GHz.

4.4.3 Other issues

The Input and output matching circuits have similar topologies as those in the previous CE LNA. MTL inductors are used in this design. Noise figure and gain are compromised in the same procedure as in the CE LNA, but with more emphasis on noise because a cascode topology can deliver a higher gain than a CE configuration.

Stability issue is not discussed in this design because every stage is unconditional stable after adding the matching circuits. Biasing circuits are integrated into the LNA, as shown in figure 4.21. DC current is optimized to be 5 mA for each stage. Only one DC voltage, Vcc, is required in this design.

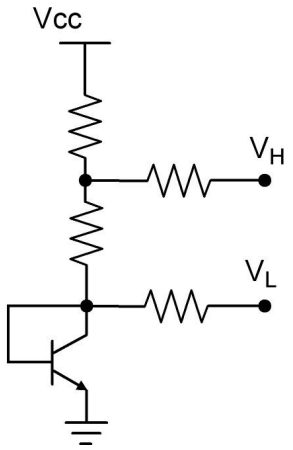


Figure 4.21. Biasing circuit of the cascode LNA.

4.4.4 Experimental results of the two-stage cascode LNA

The layout is shown in figure 4.22, where all the inductors are MTL type. This chip occupies a chip area of 0.3 mm^2 with bond-pads and 0.1 mm^2 without bond-pads. It draws 11 mA DC current from a 3.3 V DC supply including biasing current. Its noise figure has not been measured because of the lack of measurement equipment. The simulated noise figure is 6 dB, which is lower than the previous CE LNA because the noise from later stages are suppressed more efficiently thanks to the high gain of the first stage.

The measured and simulated S-parameters are shown in figure 4.23. Again the solid line is used for simulation and the dashed line with markers is for measurement results. A very good input matching is achieved because the same topology as in the CE LNA is adopted. From 49 GHz to 90 GHz, the measured S11 is below –13 dB. Simulation predicts a similar curve, which is shown in S11 plot. One of the main targets of this design is to obtain a filter-like frequency response eliminating the use of the lossy on-chip filter. The gain-frequency response is shown in S21 measurement. The measured gain at 60 GHz is 20 dB. Both measured and simulated 3-dB bandwidths are from 56 to 65 GHz, which covers the 7 GHz ISM bandwidth from 57 to 64 GHz and leaves 1 GHz margin at each side for process variations. The roll off factor is more than 35 dB per octave. This frequency response is similar to that of a third-order maximum-flat filter. It is achieved with the sacrifice of about 4 dB gain. In reverse isolation measurement, there is a big difference between

measurement and simulation, which is mainly due to the noise floor of the S-parameter measurement system. The measured and simulated output reflection is shown in S22 measurement. They have similar frequency response but with a 2 GHz frequency shift. The reason is the same as the frequency shift in the CE LNA. In this design, the output impedance of the cascode stage is even higher than that of the CE stage. The measured output return loss is 9 dB at 60 GHz.

The measured and simulated μ factors are shown in figure 4.24. They have similar curves but with a frequency deviation of 2 GHz due to the error in S22. Within the frequency range of 30 GHz to 90 GHz, all μ factors are above unity, which guarantees an unconditionally stable amplifier.

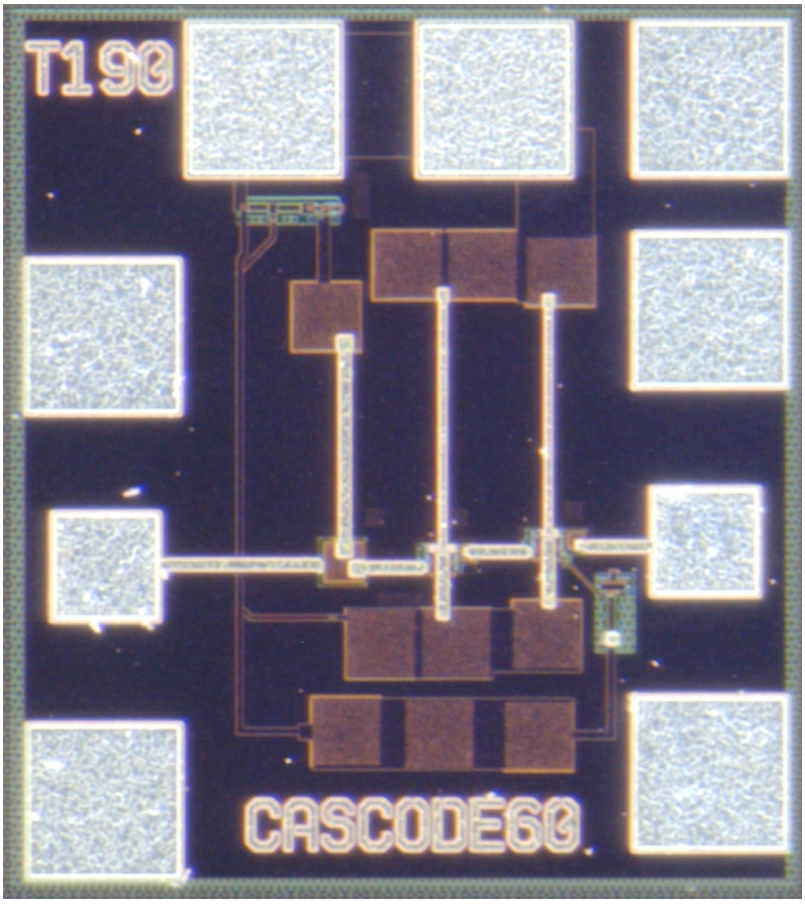
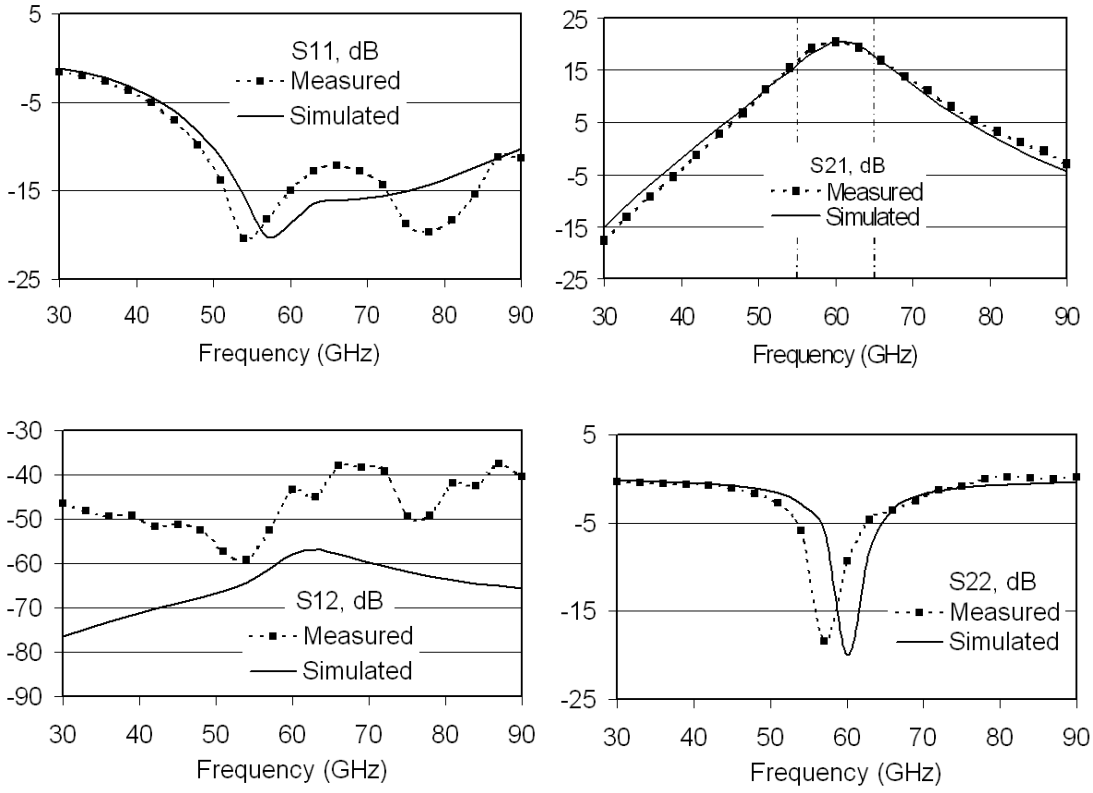


Figure 4.22. Chip photo of the two-stage cascode LNA.



Figur 5.23. Measured and simulated S-parameters of the two-stage cascode LNA.

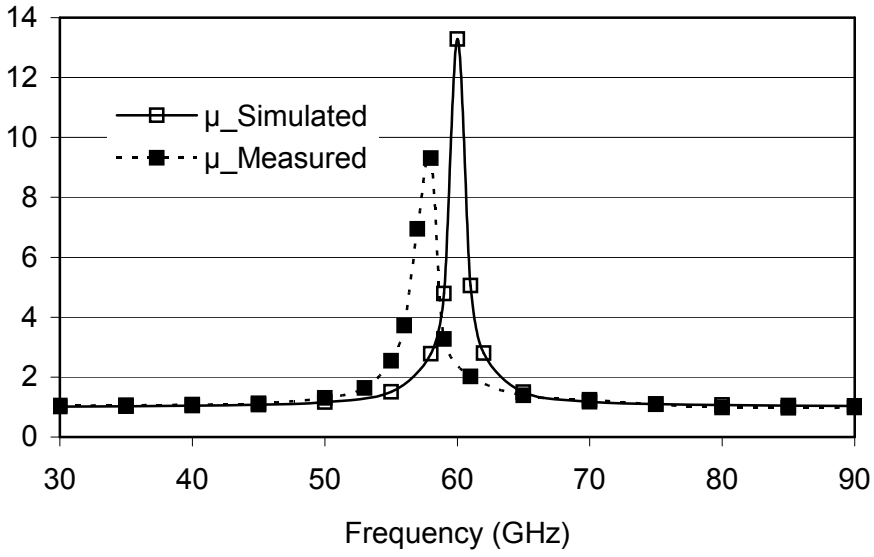


Figure 4.24. Measured and simulated μ factors of the two-stage cascode LNA.

Summary

In this chapter, the designs and experimental results of two LNA have been presented. One is a three-stage CE differential LNA, and the other one is a two-stage cascode LNA. Three types of inductors have been described and compared before the LNA designs. ML inductors are used in the CE LNA design, and MTL inductors are used in the cascode LNA because of the compromise between their Q-factors and chip areas. The CE LNA achieves a gain of 18 dB at the center frequency of 60 GHz. Its 3-dB bandwidth is 22 GHz ranging from 49 GHz to 71 GHz. A wideband input matching is achieved. The measured S11 is below –17 dB from 45 GHz to 75 GHz. A noise figure of 6.8 dB is simulated at 60 GHz. Simulation agrees well with measurements, especially the input matching and the gain. It draws 30 mA from a 2.2 V DC supply. The chip consumes an area of 0.42 mm^2 with bond-pads and 0.2 mm^2 without bond-pads.

The cascode LNA is optimized to have a filter-like frequency response eliminating the use of an on-chip RF filter. Three resonators are integrated into the load matching circuits and the inter-stage matching. A noise figure of 6 dB is simulated, which is lower than the CE LNA thanks to the high gain of the first cascode stage. The LNA has a measured gain of 20 dB at the center frequency of 60 GHz, and its 3-dB bandwidth is 9 GHz ranging from 56 GHz to 65 GHz, which covers the 7 GHz ISM band and leaves 1 GHz margin at each side for the compensation of process variation. The roll-off factor is more than 35 dB per octave. A maximum-flat frequency response is adopted in this design for the sake of minimum in-band ripple. A wide band input matching is achieved because of the same input matching topology as in the CE LNA. This LNA is a single-ended design. It occupies a chip area of 0.3 mm^2 with bond-pads and 0.1 mm^2 without bond-pads.

Chapter V Mixer Design

This chapter will discuss the design details of the 60 GHz mixers. Since there is no high performance Schottky diodes in the used technology, two active mixers are designed and fabricated. One is a Gilbert-cell mixer, which is optimized for a fully differential system. Another one is half of a Gilbert cell, which requires a single-ended RF signal and has a differential output. This mixer can be used directly with a single-ended LNA.

5.1 Gilbert cell mixer design

5.1.1 DC operation points

The core of this mixer is a Gilbert cell. Its operation mechanism has been explained in chapter III. The first step in designing a Gilbert cell mixer is to allocate and optimize the DC operation points. The maximum voltage swing at the collector is between the saturation and break-down voltages. In the used transistor, the break-down voltage, BV_{CEO}, is 2 V, which sets the highest output voltage. For a linear operation, the minimum voltage is limited by the saturation voltage. The collector-emitter voltage of the upper level transistors is set in the middle of these two voltages. The collector-emitter voltage of the lower differential pair can be set to a lower value. However in reality, it is set to be the same as that of the upper level transistors in order to achieve a high trans-conductance. The DC node voltages are shown in figure 5.1. Note that the transistors can not be completely switched off due to the limited voltage swing of the LO signal, which implies that the output voltage can not reach V_{CC}. So the voltage from V_{CC} to the emitters of the upper switching transistors is slightly higher than 2 V. In order to bias all the transistors at the currents of fmax, the transistor sizes of the differential pair are doubled. Tail Current Source (TCL) is omitted in this design to meet the voltage headroom, because a TCL consumes a DC voltage of about 0.5 V. Otherwise, supply voltage has to be increased accordingly to achieve the aforementioned DC operation conditions.

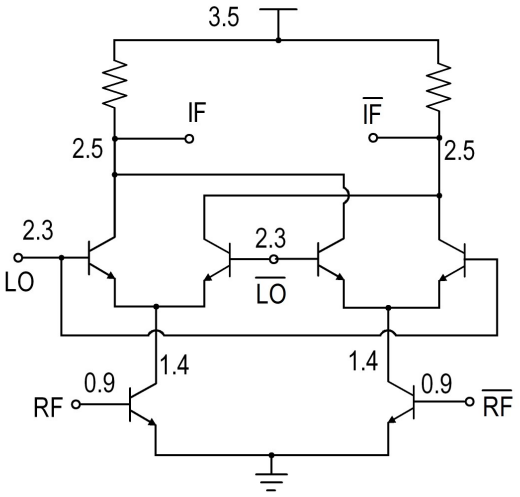


Figure 5.1. DC node voltages of the Gilbert cell core.

5.1.2 Optimization of the mixer core

The mixer optimization can be performed in two steps [40], optimizing the lower differential pair like an amplifier and optimizing the upper switching transistors like a switch. Noise of the mixer can be calculated according to the cascade noise equation:

$$F = F_{DP} + \frac{F_{SW} - 1}{G_{DP}} \qquad (5.1),$$

where F_{DP} and G_{DP} are the noise factor and gain of the differential pair and F_{SW} is the noise factor of the switching transistors. Since most of the mixer noise is from the switching transistors, it is desirable to have a high trans-conductance in the differential pair to suppress the switching noise. It is difficult to match the mixer ports by using inductive components because the three ports are very close. The best way is to choose transistors that have impedances close to 50 Ω in the operation frequency at each port eliminating inductive matching components. The fastest transistor npn200 is used is this design, and the transistors with different finger numbers are simulated in a differential pair configuration. Their input impedances are shown in figure 5.2, where the impedances refer to the input of the half circuit. The finger number is halved for the upper switching transistors. RF ports are marked by the red triangle markers and LO ports are marked with the blue X markers. From the simulation results, transistors with four to eight fingers allow us to match the RF and LO ports to 100 Ω with the

combination of a transmission line and a bond-pad capacitance. In this design, four-finger transistor is chosen for the differential pair.

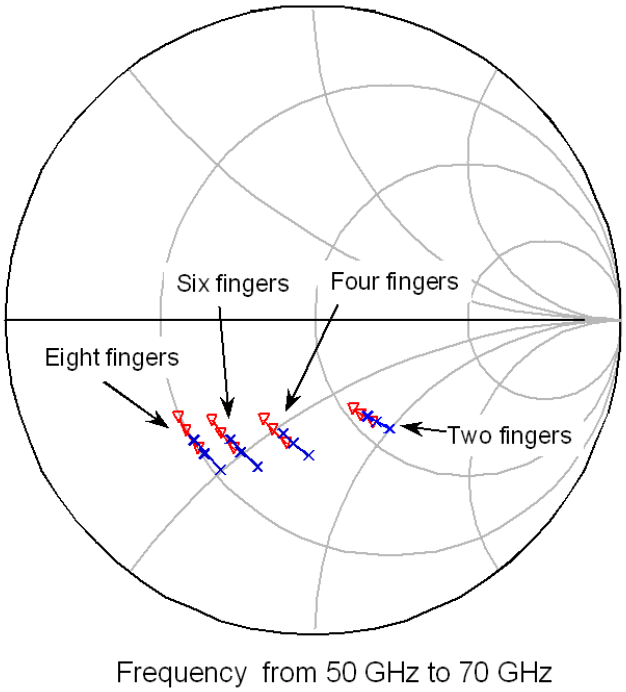


Figure 5.2. Input impedances of npn200 transistors with different fingers.

Load resistor value is a trade-off between gain, linearity and DC voltage drop, which is 250 Ω in the design. The AC current fluctuations through the load resistors are nearly fixed if RF power and LO power are fixed. A high load resistance gives a high voltage conversion gain since output voltage is the product of the AC current and the load resistance. However, a high voltage gain deteriorates the linearity in that the output voltage is clipped earlier when the input power increases. The tradeoff is set to a gain of 10 dB and an input P_{1dB} of better than -10 dBm.

5.1.3 Output buffer

The Gilbert cell alone is not able to drive a 50 Ω load (in a single-ended measurement system) and the output impedance is not matched. Two emitter followers with small output impedances and high output currents are used as a differential output buffer, which have the same voltage swing and can deliver more output power. However, wide resistors are used for the loads in order to carry sufficient current increasing the capacitive parasitics. It is observed in simulation that

the imaginary part of the output impedance is large enough to cause a loss even at 5 GHz. An inductor of 1.8 nH is introduced to match the output to a 100 Ω differential impedance. This inductor is taken directly from the design kit, which has been measured and curve fitted. The buffer stage and output matching is shown in figure 5.3.

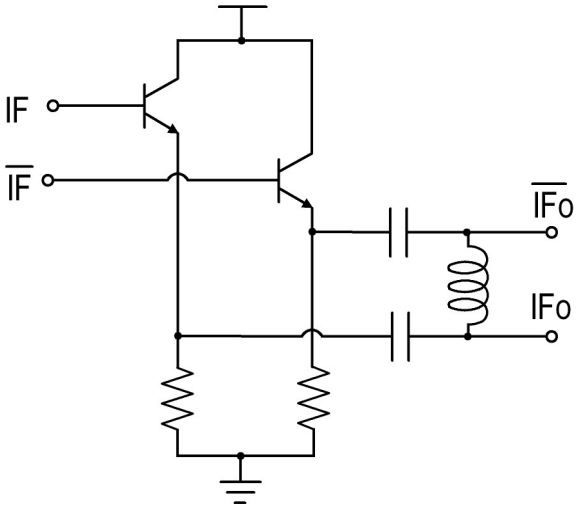


Figure 5.3. Output buffer with matching components.

This output matching topology is also used to shape the IF frequency response eliminating the use of an IF filter. The combination of the output capacitor and the matching inductor is a high-pass topology. For analysis purpose, a real ground is placed in the middle of the inductor which does not affect the signal, as shown in figure 5.4. The Gilbert cell core and the emitter-follower buffer have a low-pass characteristic due to the parasitic capacitance and the drop in transistor g_m. A band-pass characteristic can be obtained by the combination of the high-pass output matching topology and the low-pass characteristic of the output buffer. This will be shown in simulation and measurement results.

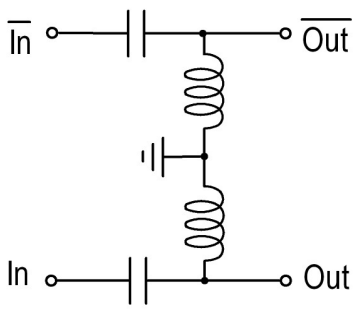


Figure 5.4. High-pass structure of the output matching circuit.

5.1.4 Mixer layout

In the mixer layout, special care is given to reduce both inductive and capacitive parasitics. At high frequencies, the post layout simulation of cadence does not work properly because the extraction procedure does not take inductive effects into account. It becomes worse if there are many long inter-connections. The accumulation of many long connection metal-wires can cause a serious error. Even though these connection wires can be modelled accurately by using either distributed or lumped components, it is always preferable to make the connection wires as short as possible. The mixer core transistors are placed with minimum allowed separation defined in the design kit documentation. All the connection wires are short enough and can be neglected reducing the design complexity. Capacitive parasitics mainly come from the overlap of metal to metal or metal to substrate which can be calculated according to the technology specification. In this layout, the capacitive parasitics in the most critical ports (LO and RF) are manually extracted and included in simulation, so that the post layout simulation is not necessary in this design. The final layout is shown in figure 5.5. It occupies a chip area of 0.6 mm^2 with bond-pads and 0.25 mm^2 without bond-pads.

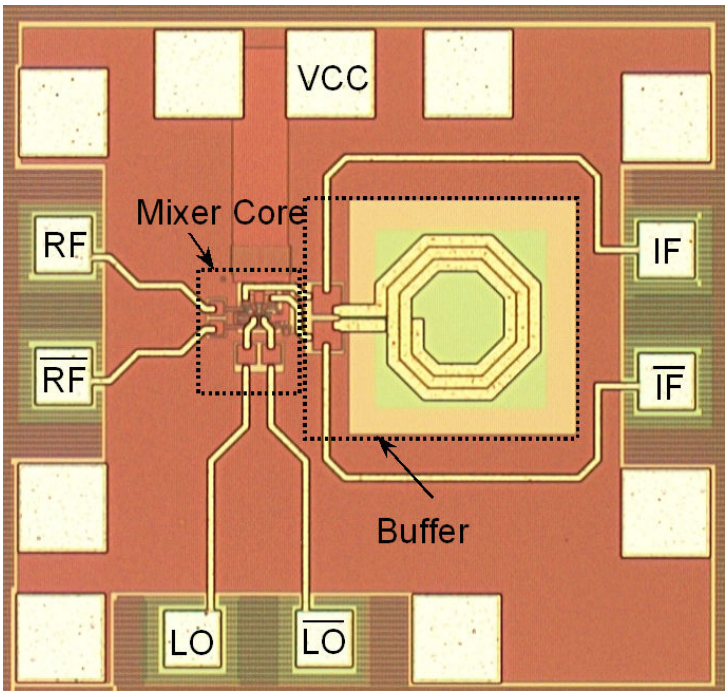


Figure 5.5. Chip photo of the Gilbert cell mixer.

5.1.5 Experimental results of the Gilbert cell mixer

The Gilbert cell mixer draws 30 mA from a 3.5 V DC supply, among which 6 mA is used for the mixer core and 24 mA for the output buffer and biasing circuit. The noise figure of the mixer has not been measured due to the lack of noise measurement system. A noise figure of 14 dB has been simulated. Its conversion gain is simulated and measured in two scenarios. The first one is to check the frequency response of one RF channel, and the second one is to check the conversion gain among all RF channels. The first scenario is shown in Figure 5.6, where LO frequency is fixed at 55 GHz and RF frequency is swept from 57 to 65 GHz. The solid markers with a dashed line are the measurement results and the empty markers with a solid line are from simulation. As mentioned before, the frequency response is due to the output matching structure. The peak at 60 GHz corresponds to an IF frequency of 5 GHz. The conversion gain achieved from 60 GHz to 5 GHz is 10.3 dB. A 2 GHz 1-dB bandwidth is measured, which is sufficient for a gigabit-per-second communication system. Simulation predicts the same center frequency of the output buffer but with a slower roll-off at both sides. It is caused by the parasitic components at IF port, where both the bond-pads and the inter-connection transmission lines are not taken into account. This tells us that the parasitic components can affect the performance even at 5 GHz, although the parasitic effect gives a better frequency response in this design.

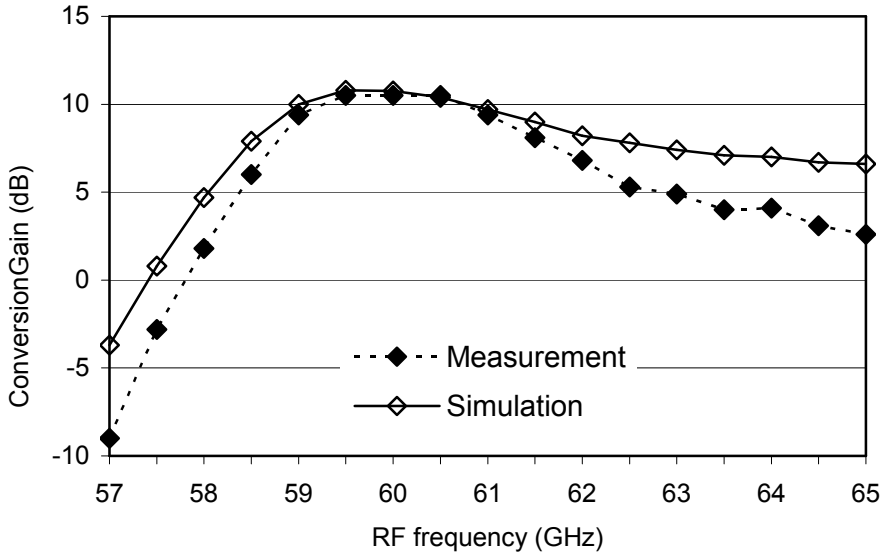


Figure 5.6. Frequency response of one RF channel.

The second scenario in conversion gain measurements is shown in figure 5.7, where both RF and LO frequencies are swept to give a fixed IF of 5 GHz. RF and LO ports are matched to a wide-band because there are no strong resonant components at these two ports. This can be seen in both measurement and simulation. The gain at 52 GHz (RF: 52 GHz, LO: 47 GHz) is 12 dB, which is 2 dB higher than that of 68 GHz (RF: 68 GHz, LO: 63 GHz). The conversion gain decreases smoothly with frequency increase due to the damping in transistor g_m. The simulation agrees well with the measurement in all the measured frequency range. This is achieved by properly modelling the parasitics including the bond-pads and inter-connection transmission lines at RF and LO ports.

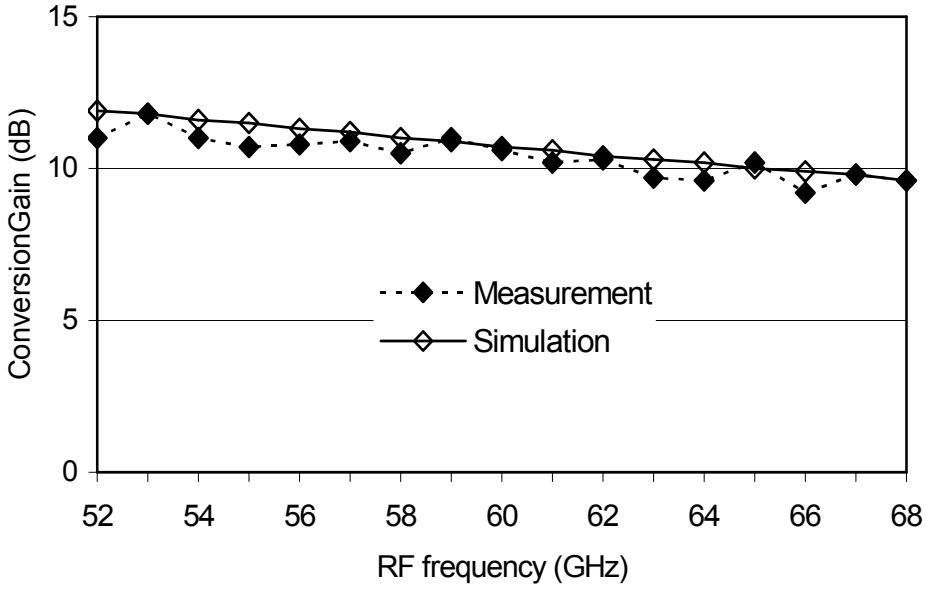


Figure 5.7. Frequency response for all RF channels.

Figure 5.8 is the 1_dB compression point measurement and simulation. In measurement, a single-ended output power is measured and a 3 dB is added to get a differential power. Fully differential configurations at all three ports are used in simulation. The measured output compression point is –1 dBm corresponding to a –10 dBm input power, and the simulated output compression point is 2 dBm corresponding to a –7 dBm input power. Simulation predicts a 3 dB higher 1-dB compression point. The reason of this difference might be the tolerance in large signal model (VBIC) of the used transistors [38].

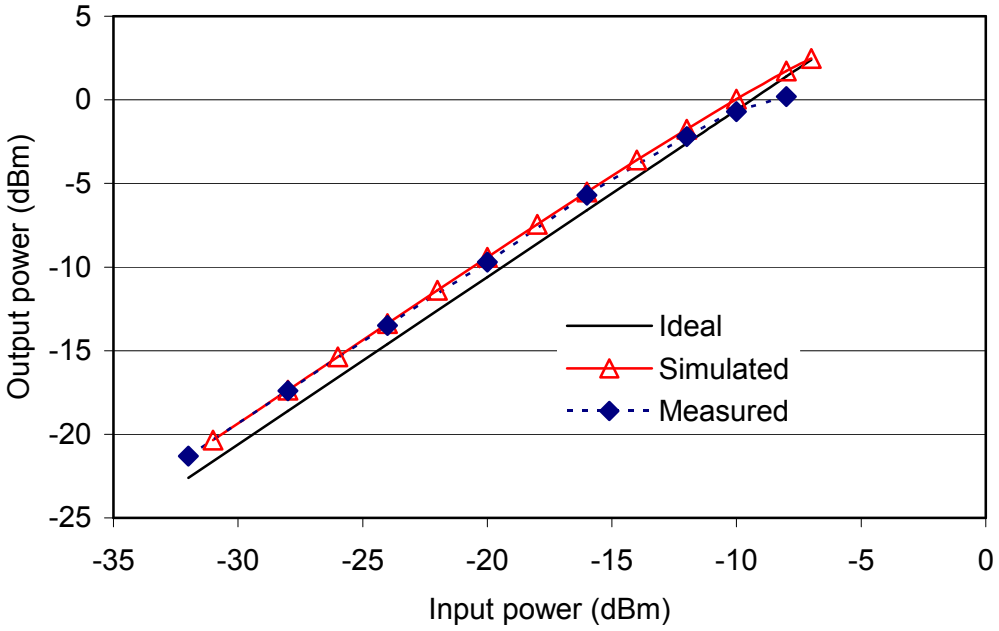


Figure 5.8. Simulated and measured compression point (RF: 60 GHz, LO: 55 GHz).

5.2 Design of a single-ended mixer

A Gilbert cell mixer can work in a single-ended configuration, but it is not best optimized for it. In order to work together with a single-ended LNA, a mixer with a topology of half of a Gilbert cell has been designed. Its schematic is shown in figure 5.9. The design procedure is the same as that of the Gilbert cell mixer. The size of the switching transistors is doubled because the transistor count is halved in this design, which will keep the same input impedance at the LO port. The size of the transistors in the lower differential pair is not changed because RF input impedance is now 50 Ω instead of 100 Ω. This topology works with a single-ended RF input, and its IF and LO ports are differential eliminating the use of a balun or a transformer if a single-ended LNA and differential IF circuitry are to be used. It is optimized to have a similar gain as the previous Gilbert cell mixer. The output buffer and matching structure are taken directly from the Gilbert cell mixer to drive the measurement system. Noise figure is similar to that of the Gilbert-cell mixer in simulation, about 14 dB. A current mirror with a resistive divider similar to that in the cascode LNA is used for biasing. All ports are AC coupled so that there is no problem of DC mismatch.

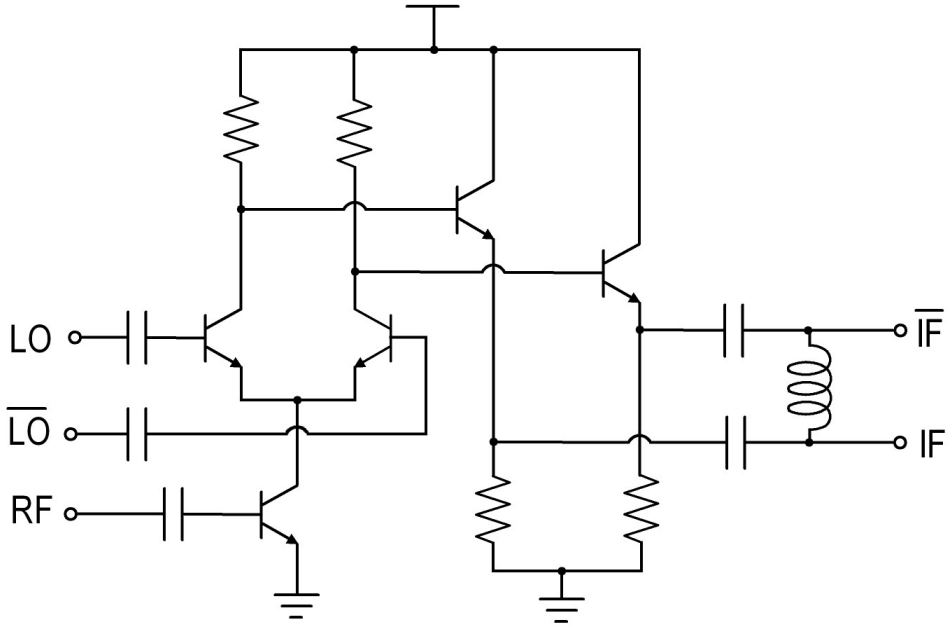


Figure 5.9. Schematic of the single-ended mixer.

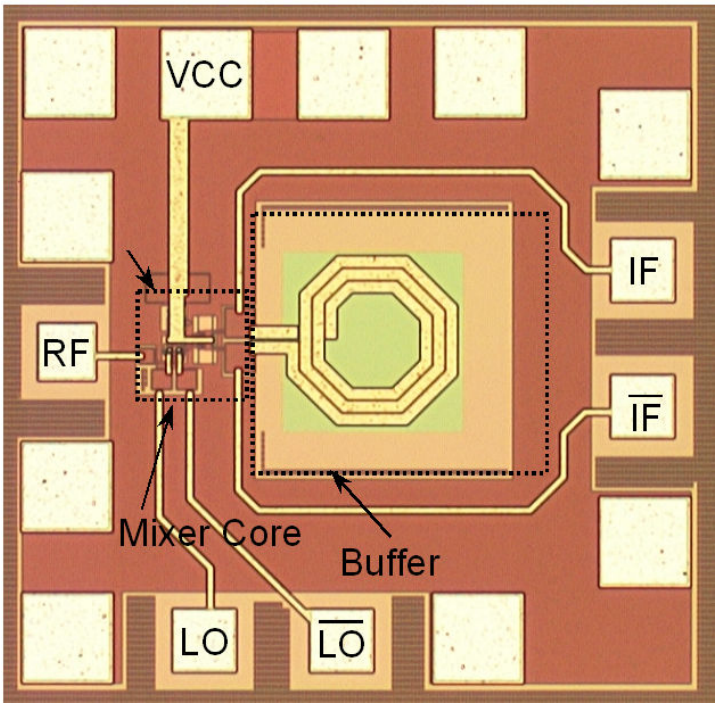


Figure 5.10. Layout of the single-ended mixer.

Via contacts have little effect and a via-array is always used wherever it is possible. They are simply treated as a short in simulation. The layout of the single-ended mixer is shown in figure 5.10. It occupies a chip area of 0.4 mm^2 with

bond-pads and 0.16 mm^2 without bond-pads. This chip draws 25 mA from a 3.5 V supply, among which 3 mA is for the mixer core, 20 mA for the buffer and 2 mA for the biasing circuit. The measured conversion gain is 10.8 dB and the measured output 1-dB compression point is –2 dBm, which are similar to those measured in the Gilbert-cell mixer. Similar frequency responses as in the Gilbert cell mixer have been obtained.

In all the above measurement, the LO power is zero dBm. The variation in conversion gain is less than 2 dB with a LO power variation from -3 dBm to 3 dBm, which has been observed both in measurement and simulation.

Summary

The design details of two mixers have been presented in this chapter, a Gilbert-cell mixer and a single-ended mixer. The single-ended mixer employs half of a Gilbert-cell as the mixer core, and shares the same output buffer and matching structure as in the differential mixer. Both mixers have a conversion gain of above 10 dB and an output compression point of above –2 dBm. The IF 1-dB bandwidth is 2 GHz due to the combined response of the output high-pass matching and the low-pass effects of the mixer core and buffer. It is sufficient for gigabit-per-second communication system. Simulation results are plotted in the corresponding measurements and good agreements are obtained. Post layout simulation has not been performed because all of the significant parasitic components have been manually extracted according to the process specification and added into the simulation. The Gilbert-cell mixer is designed for a fully differential system. And the single-ended mixer can work together with a single-ended LNA and has a differential output eliminating the use of a balun or a transformer.

Chapter VI Transceiver Integration

Designs of receiver building blocks have been presented in the precious chapters. In this chapter, the integration procedure of a transceiver will be discussed. The final receiver includes three building blocks, an LNA, a mixer and a 56 GHz PLL. Up until now, only the differential receiver has been integrated. In order to test the receiver in a real environment, a 60 GHz transmitter is also designed, which comprises three building blocks, an up-mixer, a 60 GHz buffer and a 56 GHz PLL identical to the one used in the receiver. All of the transmitter building blocks are designed and integrated into a single chip in the first run in order to catch the project schedule. Both the receiver and transmitter have been designed for a chip-on-board (COB) application with bond-wire connections. Board design issues and bond-wire compensation techniques will be discussed in the next chapter.

6.1 Receiver integration

The 60 GHz receiver has a fully differential topology, which utilizes the previous designed differential LNA and Gilbert-cell mixer. A 56 GHz PLL [39] is also integrated into the receiver chip. The integration is done in two steps: integration of LNA and mixer, and integration of the whole front-end.

6.1.1 Integration of LNA and mixer

As discussed in LNA and mixer designs, the parasitic components are well modelled and they are a part of the LNA and mixer circuits. The input and output impedances will be changed after removing the bond-pads and changing the length of the interconnection transmission lines. The conjugate matching between LNA and mixer is realized by re-optimizing the matching circuits at the output of the LNA and the input of the mixer. After removing its output bond-pads, the LNA has an inductive output impedance, while the mixer input is capacitive without any matching structure. The inter-connection transmission lines are optimized to move the LNA output to the conjugate input impedance of the mixer. The center frequency would shift a bit lower

had the LNA and mixer conjugately matched at 60 GHz due to the drop in g_m. In this design, the conjugate matching point is at around 62 GHz. The chip photo of the LNA-mixer combination is shown in figure 6.1. It consumes an area of 0.8 mm^2 including bond-pads and 0.4 mm^2 without bond-pads. The DC current consumption is the sum of the LNA and the mixer with 2.2 V and 3.5 V DC supplies respectively. The two measurement scenarios in mixer measurement are performed. Figure 6.2 shows the conversion gain versus RF frequency with LO frequency fixed at 55 GHz.

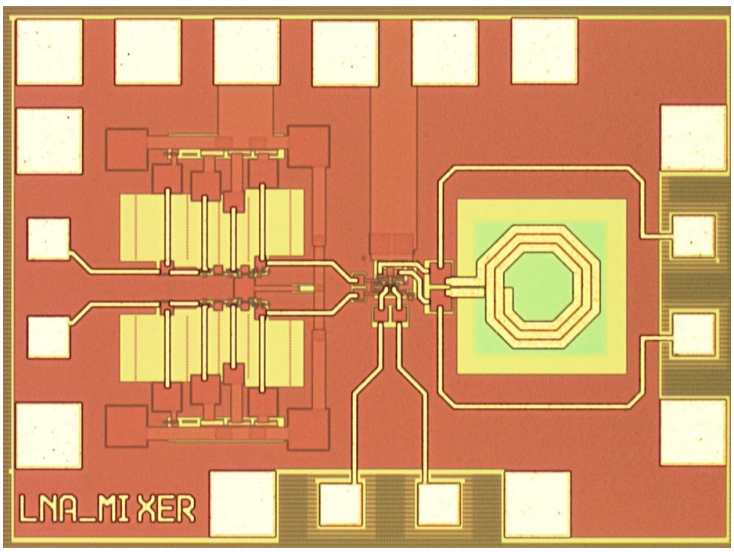


Figure 6.1. Chip photo of LNA-mixer combination.

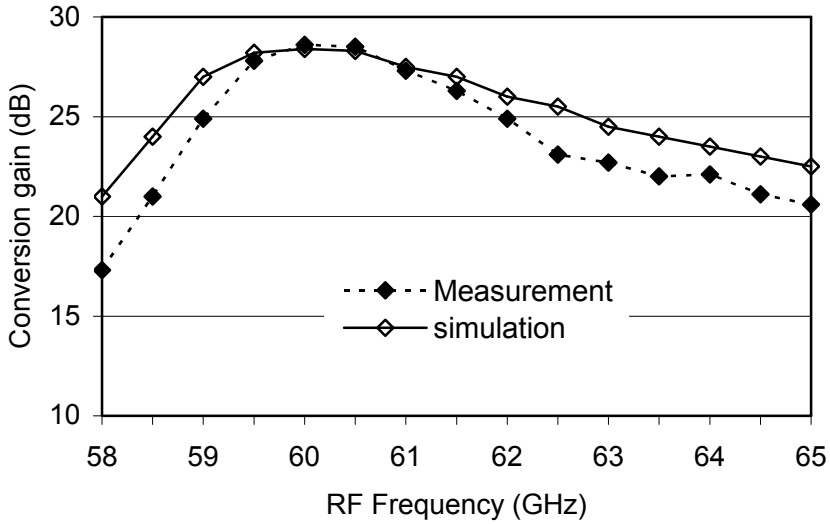


Figure 6.2. Simulation and measurement of the LNA-mixer combination with a fixed 55 GHz LO frequency.

At RF center frequency of 60 GHz, the measured conversion gain is 28.6 dB while the simulated conversion gain is 28.4 dB, which is the sum of the LNA gain and the mixer gain. The frequency response is similar to that of the Gilbert-cell mixer. The mismatch between measurement and simulation at high and low frequencies are mainly from the Gilbert-cell mixer.

Figure 6.3 is a conversion gain plot versus RF frequency with both RF and LO frequency swept to have a fixed 5 GHz IF frequency. RF frequency is swept from 56 GHz to 66 GHz with a corresponding LO frequency from 51 GHz to 61 GHz. A wideband frequency-response is measured. The gain ripple is within 1 dB in the 60 GHz ISM band, which guarantees the front-end works equally well in all the 60 GHz sub-channels. Simulation agrees well with the measurement in the whole measured frequency range.

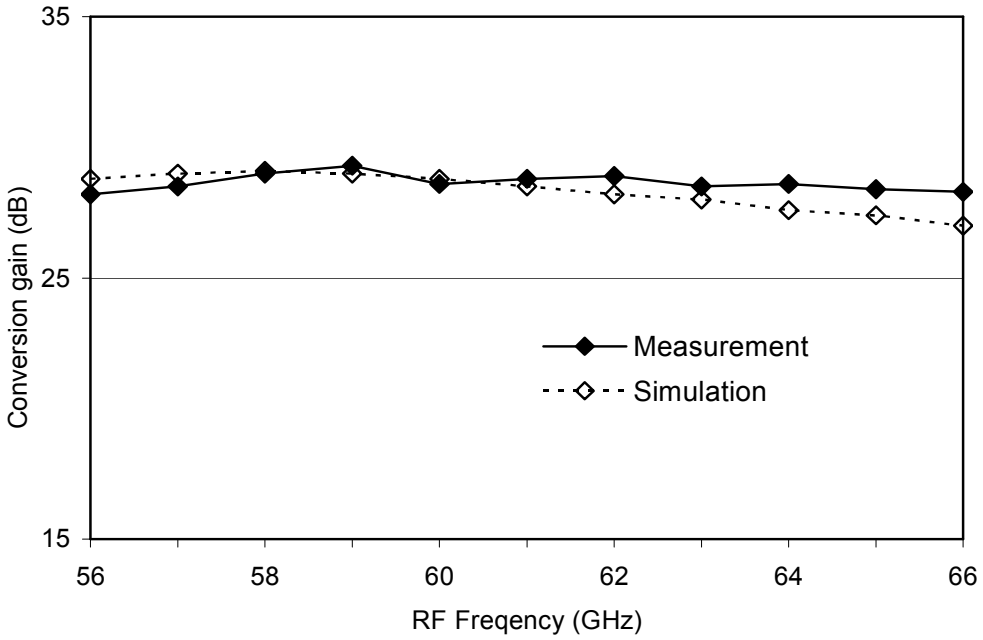


Figure 6.3. Simulation and measurement result of the LNA-mixer combination with a fixed 5 GHz IF.

6.1.2 Integration of receiver front-end

The used 56 GHz PLL features a fourth order topology [39]. It consists of a 56 GHz VCO [40], a divider with a division ratio of 512, a third-order loop filter and a charge pump. Its building block diagram is shown in figure 6.4. A wide bandwidth

of 4.5 MHz is used in the loop filter to suppress the phase noise of the VCO. This requires a very-low-phase-noise reference signal. The phase noise of the reference signal is amplified by 54 dB for a division ratio of 512 if the phase noise slope is assumed to be 20 dB per decade. In an OFDM system, it is very important to have a low phase noise LO. The measured phase noise of the PLL at 1 MHz offset is –90 dBc/Hz. The PLL consumes a DC power of 600 mW.

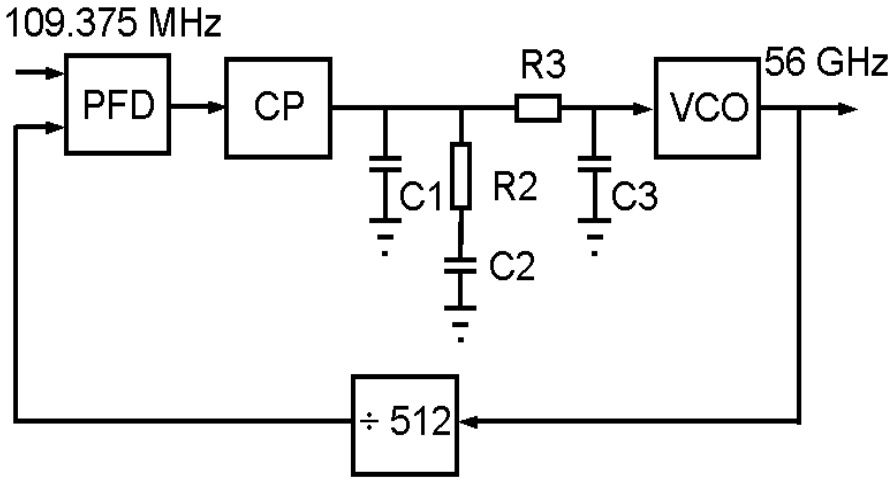


Figure 6.4. Diagram of the 56 GHz PLL.

The interface between the PLL and the mixer is rather strait forward. All the bond-pads from the PLL are kept in the layout, so that the PLL can be tested separately after cutting the connection transmission lines. The two 56 GHz differential transmission lines are optimized to have identical electric lengths to the LO inputs of the mixer.

The chip photo of the whole front-end is shown in figure 6.5, where all the building blocks have been marked out by the dashed boxes. As can be seen from the chip photo, many redundant bond-pads are placed around the chip as ground connections. The two PLL outputs are aligned with the two LO inputs to achieve a perfect symmetry, and they are connected by two transmission lines. The whole front-end chip consumes a chip area of 1.6 mm^2 with bond-pads and 1.1 mm^2 without bond-pads.

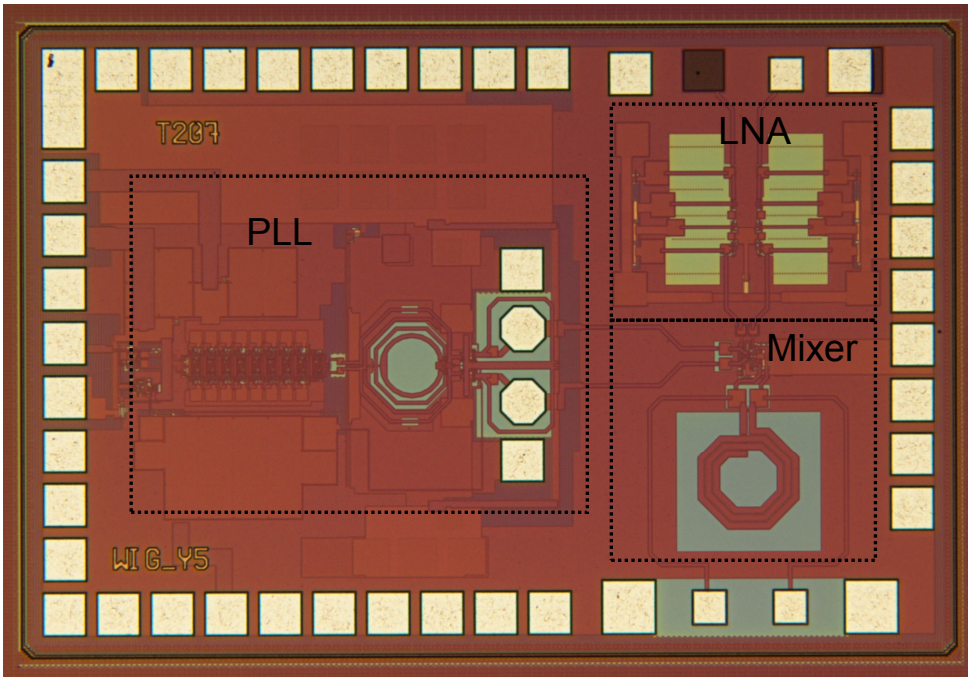


Figure 6.5. Chip photo of the complete 60 GHz front-end.

After integration, however, LO frequency is limited to the PLL tuning range and its power is fixed to the PLL output power. This receiver chip is measured in the whole PLL locking range from 54.3 to 56.5 GHz by varying the reference frequency. In figure 6.6, the conversion gain with a fixed 5 GHz IF is plotted, where RF is from 59.3 to 61.5 GHz. The measured conversion gain is from 22.1 dB to 19.3 dB. The difference in conversion gain between LNA-mixer combination and the front-end is due to the LO power mismatch. If LO power is below –3 dBm, it is not sufficient to switch the RF current between the two loads. In this case, it works more like a four-quadrant multiplier. If we compare its frequency response with figure 6.3, this complete front-end has a bigger ripple, which is due to the ripple in PLL output power. The conversion gain is almost constant at an LO power between –3 dBm to 3 dBm, and it drops quickly with the decrease of LO power. Low LO power effect can also be seen in figure 6.7, which is the output 1-dB compression point measurement. The output P_{1dB} happens at –5 dBm, which is about 4 dB earlier than that of the LNA-mixer combination.

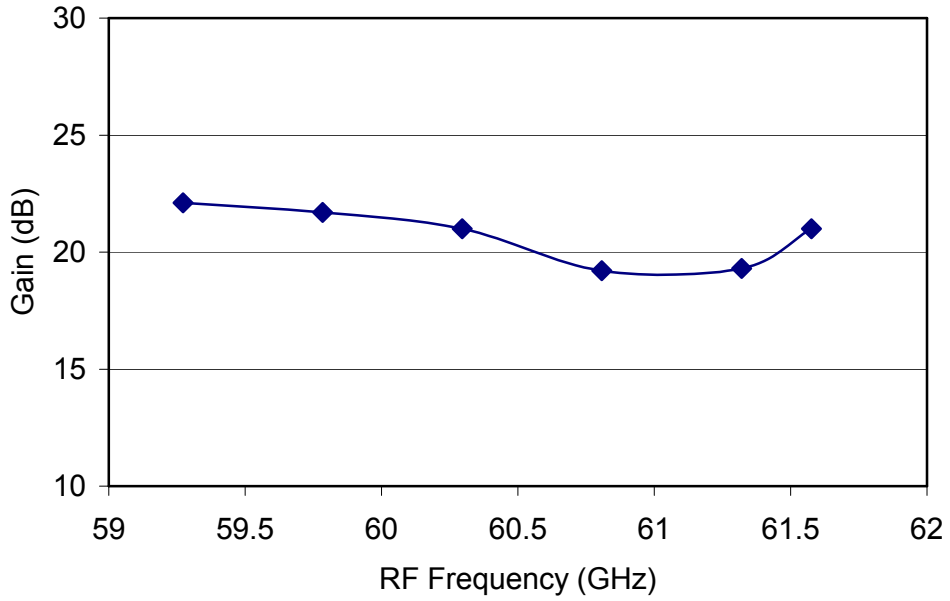


Figure 6.6. Conversion gain of the complete front-end with a fixed 5 GHz IF by varying PLL output frequency and RF frequency.

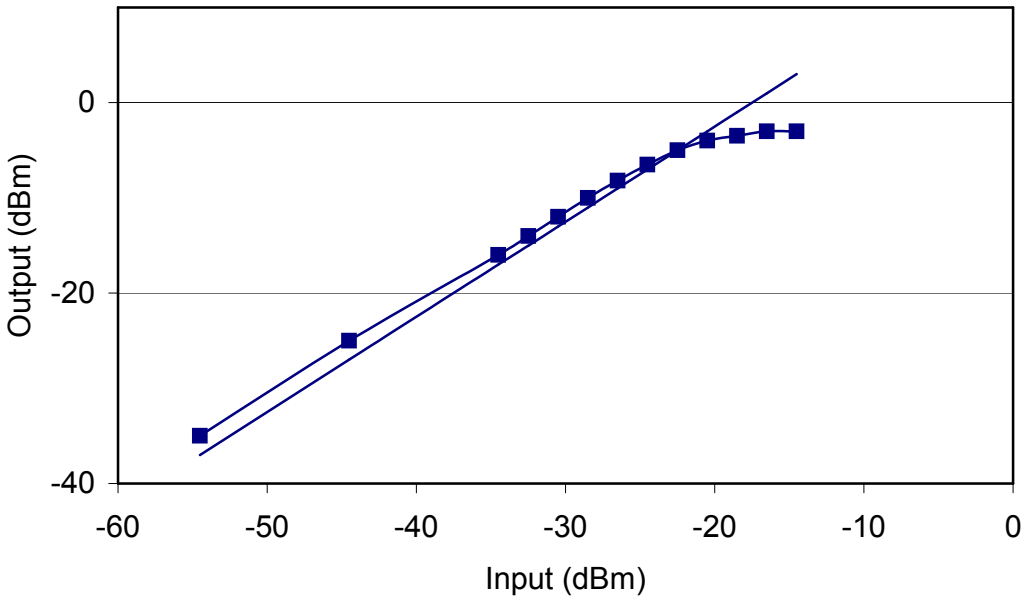


Figure 6.7. Measured output 1-dB compression point of the complete front-end with LO and RF frequencies of 56 and 61 GHz.

6.2 Design and integration of the transmitter chip

In order to test the previous designed receiver chip and the whole 60 GHz wireless link, a 60 GHz transmitter chip is also designed and fabricated in the same technology. This chip includes three building blocks, an up-converter, a 60 GHz buffer and a 56 GHz PLL identical to the one used in the previous designed receiver. The block diagram is shown in figure 6.8. All of the building blocks are designed and integrated into a single chip in the first shot due to the project schedule.

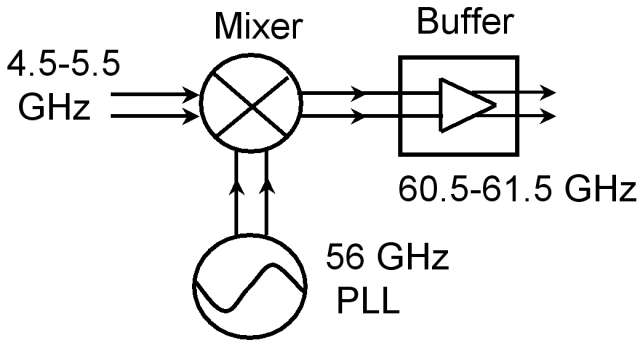


Figure 6.8. Building block diagram of the 60 GHz transmitter front-end.

6.2.1 Design of up-converter mixer

A Gilbert-cell is again used as the up-converter core, but with an emphasis on output power and DC power consumption. In an up-converter, the noise figure and conversion gain become less important due to the fact that it is easier to get a large IF input power. The same DC operation points are used as those in the Gilbert-cell down-conversion mixer. However, the AC voltage is not able to reach the same amplitude as in the down-conversion mixer due to the high output frequency. The main reasons of smaller output signal are the low g_m of the transistors and the low-pass characteristic at the output. R-C type low-pass structure exists at the output of the up-converter core, where R comes from the combination of the load resistor and the collector resistance and C comes from the parasitic capacitances of the load resistor and of the collector of the transistors. In simulation, the highest output signal at 60 GHz is -10 dBm and its 1-dB compression point is –15 dBm. The schematic is similar to figure 5.1, however, with the input and output ports optimized for 5 GHz and 60 GHz, respectively. A DC blocking capacitor is introduced between the

up-converter and the output buffer avoiding DC mismatch. The up-converter core is optimized to consume a DC current of 10 mA from a 3.5 V supply.

6.2.2 Design of the 60 GHz output buffer

A high gain 60 GHz buffer is introduced to amplify the weak output signal from the up-converter. A two-stage cascode topology is chosen for the buffer. A cascode amplifier is essentially a two-stage amplifier, the lower CE configuration and the upper CB configuration. For a low base resistance, the break-down voltage of a CB stage is much higher than that of a CE configuration [41]. In the first cascode stage, a four-finger transistor is used as the lower transistor and an eight-finger transistor is used as the upper transistor. Two eight-finger transistors are used in the second cascode stage. The half circuit of the buffer is shown in figure 6.9.

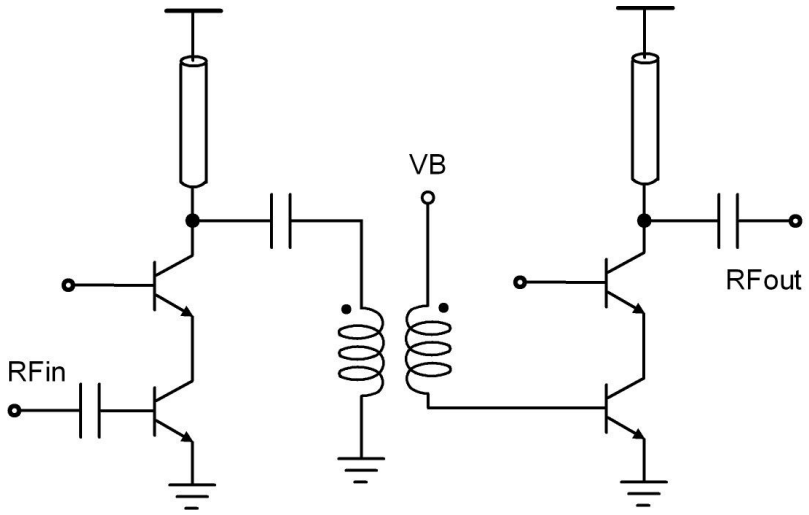
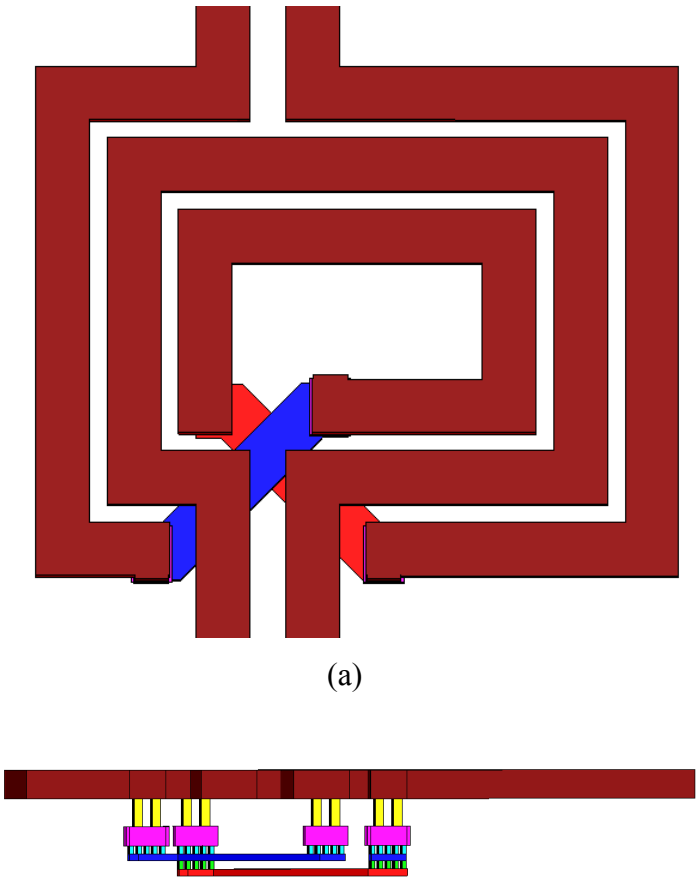


Figure 6.9. Half circuit of the output buffer.

The matching between the up-converter and the buffer is realized by a low impedance transmission line transforming the capacitive input impedance of the buffer to an inductive impedance to achieve a conjugate match to the up-converter core. The transmission line is realized in a spiral way in metal3 instead of in top-metal layer in order to save chip area and to reduce the coupling between the spiral sections. Meandered microstrip transmission lines are used for all the load inductors because meandered lines have less overall lengths than the lengths of strait lines. A 2:1 ratio transformer is used between the two stages transforming the high output impedance of

the first stage to the low input impedance of the second stage. It is realized in top metal layer, which has the lowest loss due to its thickness and the smallest parasitic capacitance to the lossy silicon substrate. Under-paths are realized in metal4 and metal3. Its physical routing is shown in figure 6.10. Minimum line spacing of 2 um is used to increase the coupling factor. A transformer is the most compact way for impedance transformation. It consumes an area of 70 um by 60 um. If, otherwise, a quarter-wave transmission line were used, the length would be 600 um. Moreover, it is difficult to design a low-loss transmission line with a characteristic impedance of more than 70 Ω in the used technology due to the high resistive loss.



(a)

(b)

Figure 6.10. The 2:1 ratio transformer, (a) top view, (b) side view.

One end of the two-turn primary is connected to the output of the first cascode stage, and the other end is grounded. As shown in figure 6.9, the DC bias current flows through the one-turn secondary to bias the second cascode transistors. The transformer is designed to be inductive at the 60 GHz band, which allows it to

compensate for the parasitic capacitances of the second stage without requiring inductive matching components. Figure 6.11 is the EM simulation results of the transformer. In the simulation, the primary port impedance is 200 Ω and the secondary is 50 Ω. The blue dashed lines with solid markers are the simulation results of the transformer before adding parasitic capacitances, and the red solid lines with empty markers are the simulation results after adding the parasitic capacitances. In primary, a series capacitor is added to block DC current and to match it. In secondary, the parasitic capacitances from the bases of the transistors to ground are extracted and added into the schematic.

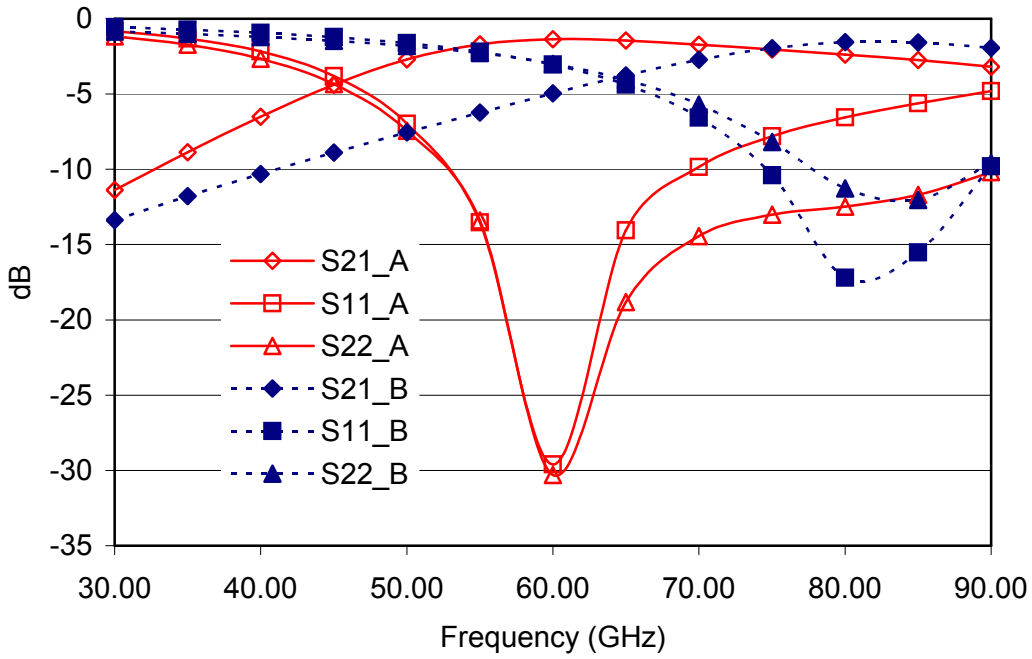


Figure 6.11. EM simulation results of the transformer before and after adding parasitic capacitances (A: after, B: before).

The output of the two-stage buffer is matched to a 100 Ω differential impedance. Its DC currents are optimized to be 8 and 2 mA for the first and second cascode stages. The first stage is biased to class A configuration providing the highest possible gain for the small input signal. However, the drawback is that it is compressed earlier than the class B and class AB configurations. The second stage is biased at class AB, which has a lower gain for a small input power and a peaking effect with the increase of the input power. The highest linearity can be achieved by properly optimizing the second stage, so that the gain damping in the first stage and

the gain peaking in the second stage happen simultaneously. This pushes P-1dB close to its saturation power. The simulated small signal gain of the buffer is shown in figure 6.12.

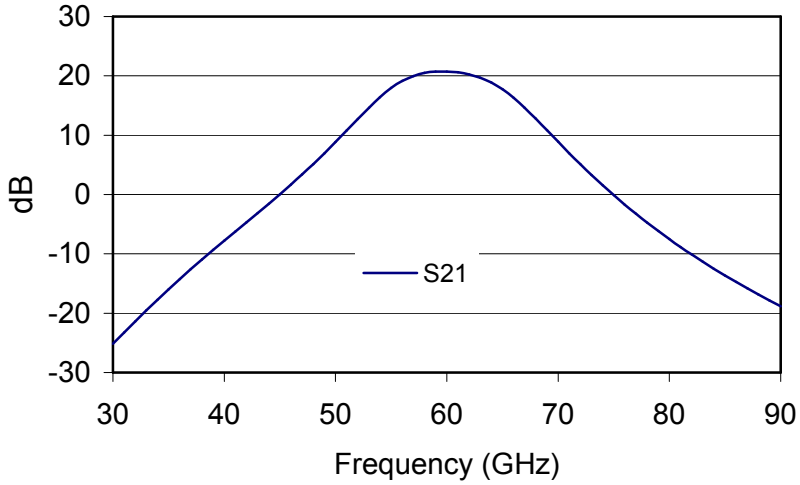


Figure 6.12. Simulated small-signal gain of the two-stage cascode buffer.

6.2.3 Integration of transmitter building blocks

The up-converter and the output buffer are integrated together and conjugate matched in between. Figure 6.13 is the simulated small signal conversion gain of the front-end. Figure 6.14 is simulated P-1dB of the front-end, where the compression is due to the up-converter core. In the simulation, a 0 dBm LO power is used.

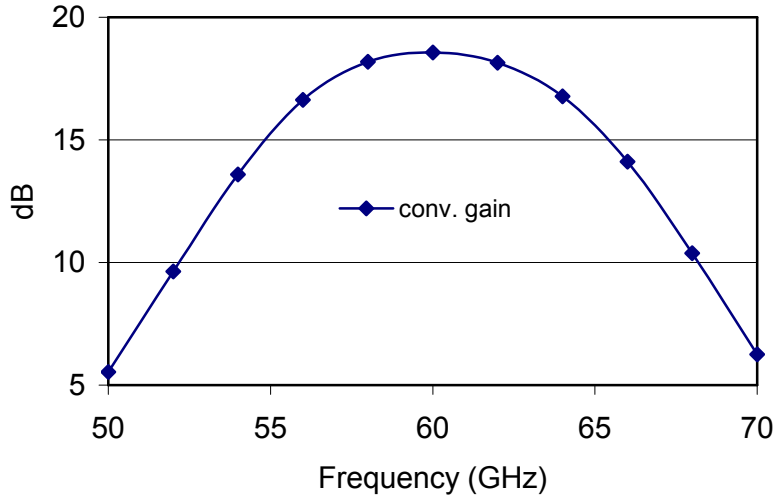


Figure 6.13. Simulated small-signal conversion-gain of the transmitter front-end with 0 dBm LO power (input frequency is 5 GHz and LO frequency is swept from 45 GHz to 65 GHz resulting an RF output frequency from 50 GHz to 70 GHz).

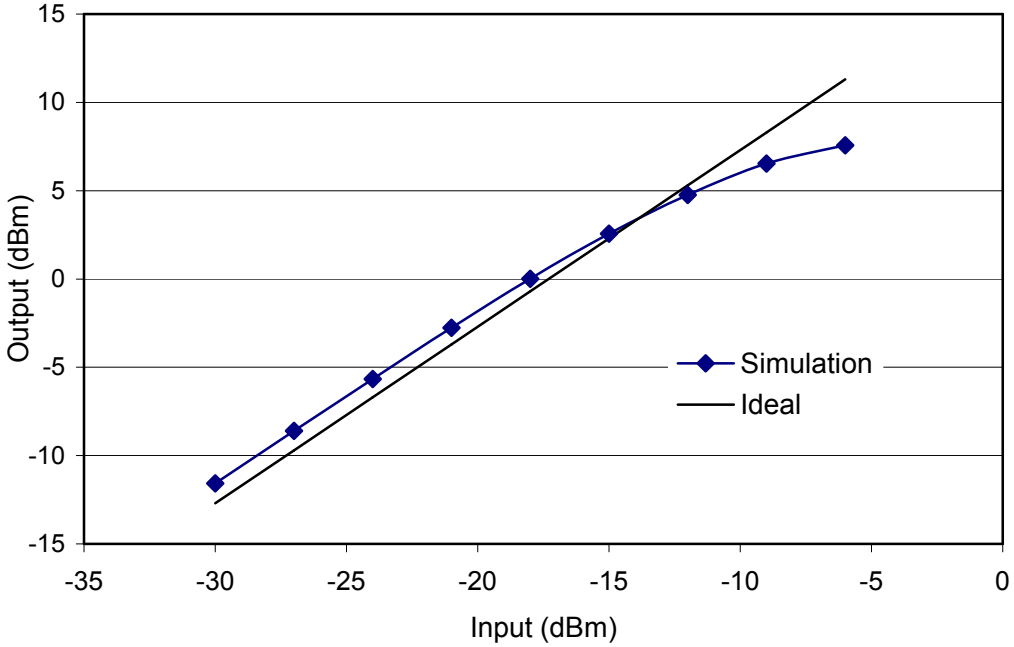


Figure 6.14. Output P-1dB simulation of the transceiver front-end (input: 5GHz, LO: 56 GHz, 0 dBm).

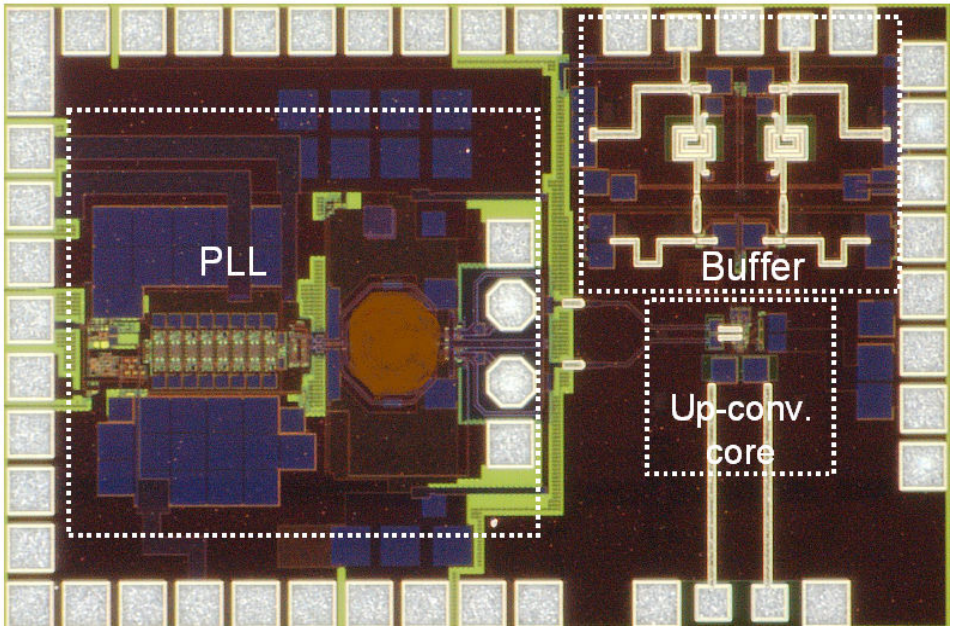


Figure 6.15. Chip photo of the complete transceiver front-end.

The PLL is integrated in the same way as in receiver integration. The chip photo is shown in figure 6.15 with all building blocks marked out by the dashed boxes. It occupies an area of 1.8 mm^2 with bond-pads. The measurement of the transmitter

chip is carried out after the chip is assembled onto an application board with a 60 GHz Vivaldi antenna and will be shown in the next chapter.

Summary

In this chapter, some of the building blocks designed in the previous chapters have been integrated into a complete receiver FE. This receiver FE is a differential design by utilizing the differential CE LNA and the Gilbert-cell mixer. The building blocks of a differential transmitter FE are designed and integrated in the first shot. There are three building blocks in the transmitter FE: an up-converter, an output buffer and an identical PLL as in receiver. The transmitter and receiver chips are designed for a chip-on-board application.

Chapter VII Board Design and Wireless Measurement

Transmitter and receiver chips have been integrated in the previous chapter. They are to be assembled onto transmitter and receiver application boards. The substrate loss at 60 GHz is critical preventing the use of the standard PCB materials. Rogers substrates have a low cost compared to ceramic materials and an acceptable performance at 60 GHz. The Rogers 3003 with a thickness of 5 mil is employed as the application boards. Since the chips are designed for COB applications, packaging issues are considered before the board designs. The cheapest packaging technique is the use of bond-wires. However at millimeter wave, the loss due to inductive mismatch is high. A cavity is designed to hold the chips in order to make the connection bond-wires as short as possible minimizing the inductance of the bond-wires. A batch of bond-wires are used to guarantee a low inductance between the chip ground and board ground. Two bond-wires in parallel are used for RF connections to reduce the inductance. Furthermore, a compensation structure is introduced on-board to overcome the inductive mismatch. Vivaldi antennas are also integrated onto the boards. The transmitter and receiver boards are tested separately with a wave-guide horn antenna. The measurement results agree with the predictions calculated in the link budget analysis.

After the chips are mounted onto the boards, they are measured in a real indoor environment together with a 5 GHz direct QPSK modulator/demodulator pair. Both OFDM single carrier QPSK signals are applied for the constellation measurements. The maximum achieved error-free data-rate is 1080 Mbit/s at a distance of 0.15 meter with an OFDM 64 QAM modulation and a ¾ coding scheme. At a distance of 1 m, the error-free transmission can reach 480 Mbit/s with an OFDM QPSK modulation and a ½ coding scheme. The lack of an on-chip or off-chip PA limits the output power so as to the maximum transmission distance. In order to achieve a linear amplification required by OFDM modulation scheme, output power is further reduced from the P_{1dB} of the transmitter. The minimum back-off is 6 dB. A fast commercial DA converter is used for data generation, which gives a maximum SNR of 32 dB setting the upper limit of data transmission.

7.1 Board design and COB Assembly

7.1.1 Cavity design

The substrate material is Rogers 3003 with a thickness of 5 mil (127 um) and a thick layer of FR4 at the backside for mechanical support. In order to achieve the shortest connections for grounds and the 60 GHz signal, the chip is put into a cavity so that the chip and the board have the same top surface. The profile of the cavity is shown in figure 7.1. Bottom copper layer of Rogers substrate is assigned to be the board ground, and it is connected by the copper wall of the cavity to the top metal layer, which gives the shortest connection to bottom. A 100 um intermediate layer is inserted in between the Rogers and FR4 boards. The depth of the cavity is about 270 um, which is the sum of two 18 um copper layers and the thicknesses of the Rogers and intermediate layers. The two metal layers of the FR4 substrate is connected by a via array for a better heat dissipation.

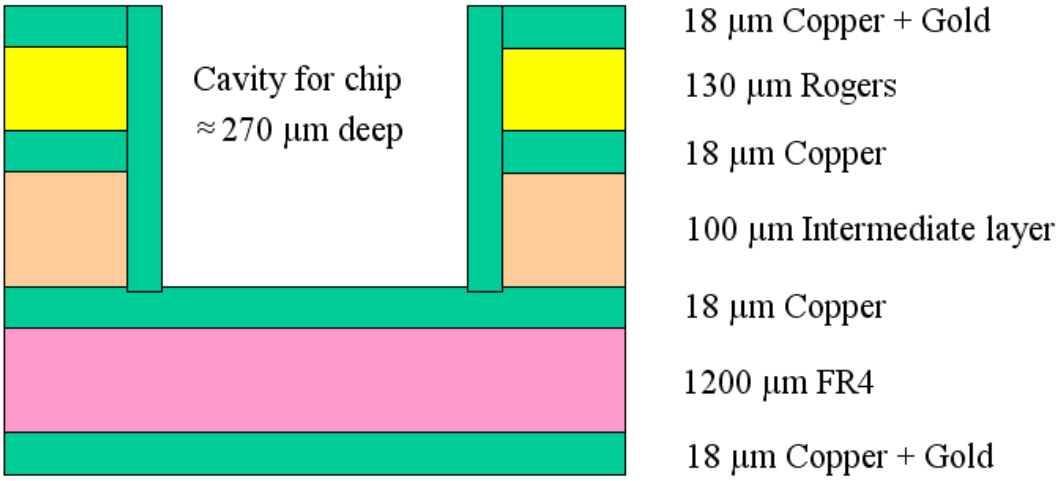


Figure 7.1. The cavity profile.

7.1.2 Bond-wire compensation structure

The transceiver chips are designed to work with bond-wires. It is of extreme importance that the bond-wire inductance between the on-chip ground and the board ground is as small as possible to avoid oscillation. In signal paths, the extra bond-wire

inductance may cause an unnecessary loss due to the mismatch, which will deteriorate the chip performance.

The main idea of putting the chip into a cavity is to reduce the inductance of the bond-wire. The shortest bond-wire length can be realized is about 300 um, and its empirical inductance is 0.3 nH. This inductance will cause a serious mismatch at 60 GHz. A microstrip transmission line (MTL) can be modelled by a lumped LC ladder as shown in figure 7.2. Each ladder unit represents a small length of the MTL. For an electrical short MTL, a single lumped unit models it well. The idea of compensation is to incorporate the bond-wire inductance into a unit of the lumped LC ladder. With the increase of electrical length, a single unit becomes not accurate. However, its parameters can be tuned to give a low-loss within a limited bandwidth. There are two ways of splitting the ladder network into sub-networks as shown in figure 7.3. A Π sub-network is obtained by splitting the shunt capacitors into two parallel capacitors, and a T sub-network is obtained by splitting the ladder in the middle of the inductors.

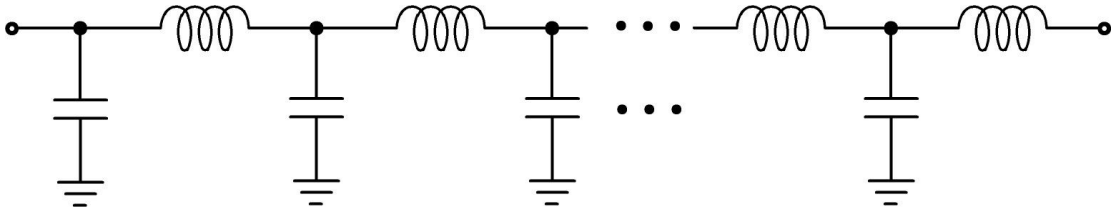
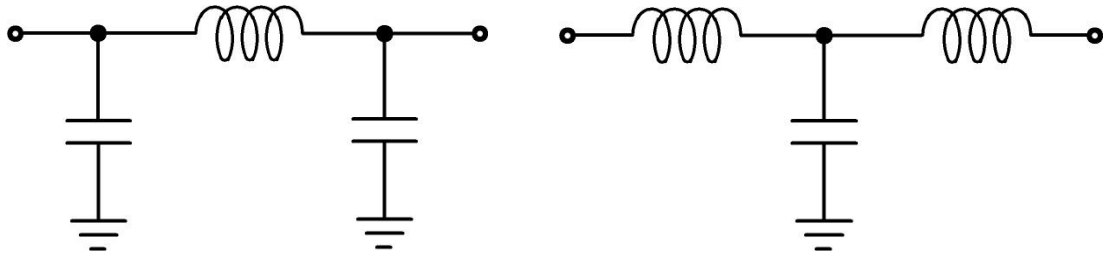


Figure 7.2. Lumped model for transmission line.



(a) (b)

Figure 7.3. Single unit lumped models of a TL, (a) Π-network, (b) T-network.

If the Π-network is to be used, the chip has to be redesigned to include a shunt on-chip capacitor. So the T-network approach is adopted in this design, where the first inductor is replaced by the bond-wire inductance and the second one is realized

on-board by a high-impedance microstrip transmission line. The capacitor is realized by the capacitance of the on-board bond-pad. This network can compensate up to 200 pH inductance in simulation. Figure 7.4 shows its layout drawing, and figure 7.5 shows the simulated insertion loss and return loss after adding the compensation structure to a 200 pH bond-wire inductance.

Note all the above discussions are based on an ideal connection between the on-chip and on-board grounds. The compensation is not valid should any significant inductance exist between the two grounds. To guarantee a low ground inductance, many bond-wires in parallel are used and they are connected in a shortest distance as discussed in the cavity design.

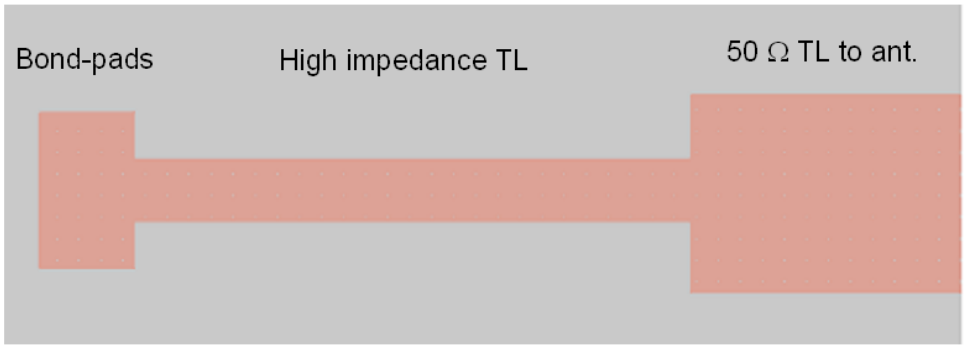


Figure 7.4. Layout drawing of the compensation structure.

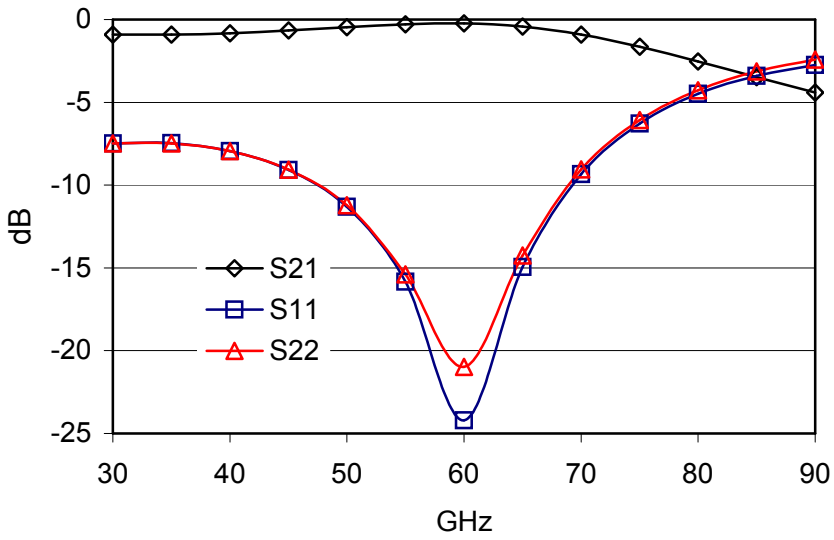


Figure 7.5. Simulated results after adding the compensation structure.

7.1.3 Board layout

The layout of the receiver board is shown in figure 7.6. RF and analogue signals are connected by MTLs. A 50 Ω MTL has a width of 300 um in the used Rogers substrate. The minimum line width and spacing are specified to be 100 and 110 um by the manufacturing factory. The compensation structure in figure 7.4 is introduced right before in LNA input, which is connected to an MTL to feed a 50 Ω on-board antenna. All other connection lines have microstrip tapers in the end towards the chip. A 60 GHz Vivaldi antenna designed in the University of Karlsruhe has been integrated into the board. The upper part of the antenna is shown in the figure, and another part is realized in the bottom metal layer of the Rogers substrate. The supporting FR4 is cut off along the antenna box to allow a better radiation. This antenna has a gain of about 9 dB. Two SMA connecters opposite to the antenna are used for 5 GHz IF port. The differential IF MTLs are placed close to each other to reduce external interferences. Another SMA connector is used for the 109 MHz reference signal. The pads in the middle of the board are reserved for a Quartz oscillator, which replaces the external generator. DC connectors are placed on two sides of the boards as shown in the figure.

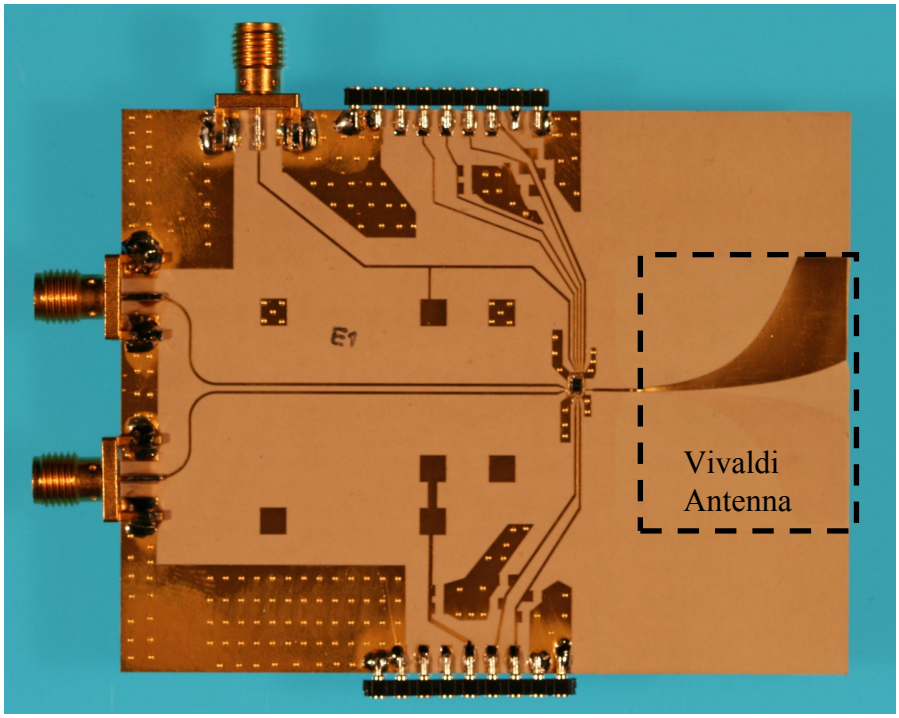


Figure 7.6. Receiver board.

7.1.4 Chip assembly

The chip is first glued on the bottom of the cavity, and then connected to the board by bond-wires. Two parallel bond-wires are used for the 60 GHz signal in order to reduce the bond-wire inductance. Figure 7.7 shows a chip that has been mounted into a cavity with the connection bond-wires. The compensation structure is also shown in the figure. Because the Vivaldi antenna is single-ended, only one path of the LNA is connected to the board. The other path is connected to a 50 Ω on-chip resistor. Ground connections are realized by the short bond-wires around the chip. The chip is positioned close to the antenna side to minimize the inductance at 60 GHz. A transmitter board is designed in the same way, as shown in figure 7.8. However, DC supplies for the output buffer of the transmitter chip need to be AC de-coupled to prevent low frequency oscillations caused by the inductances of the DC feeding lines. The planned GaAs PA is not used in the TX board. However, the footprints are already integrated in the board. Bond-wires are used to shortcut the input and output pins of the PA footprints.

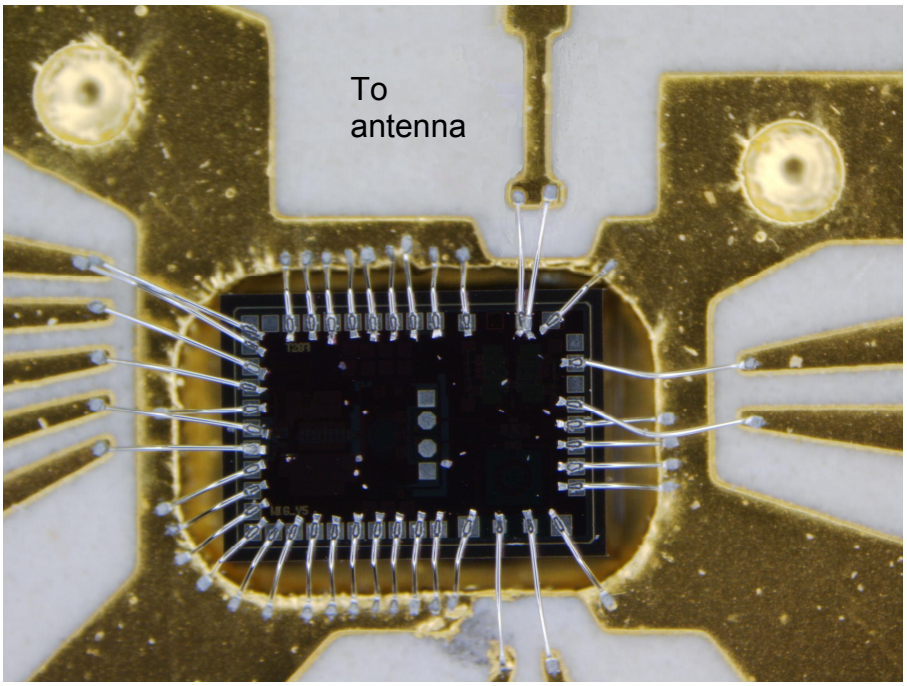


Figure 7.7. Receiver chip mounted into the cavity.

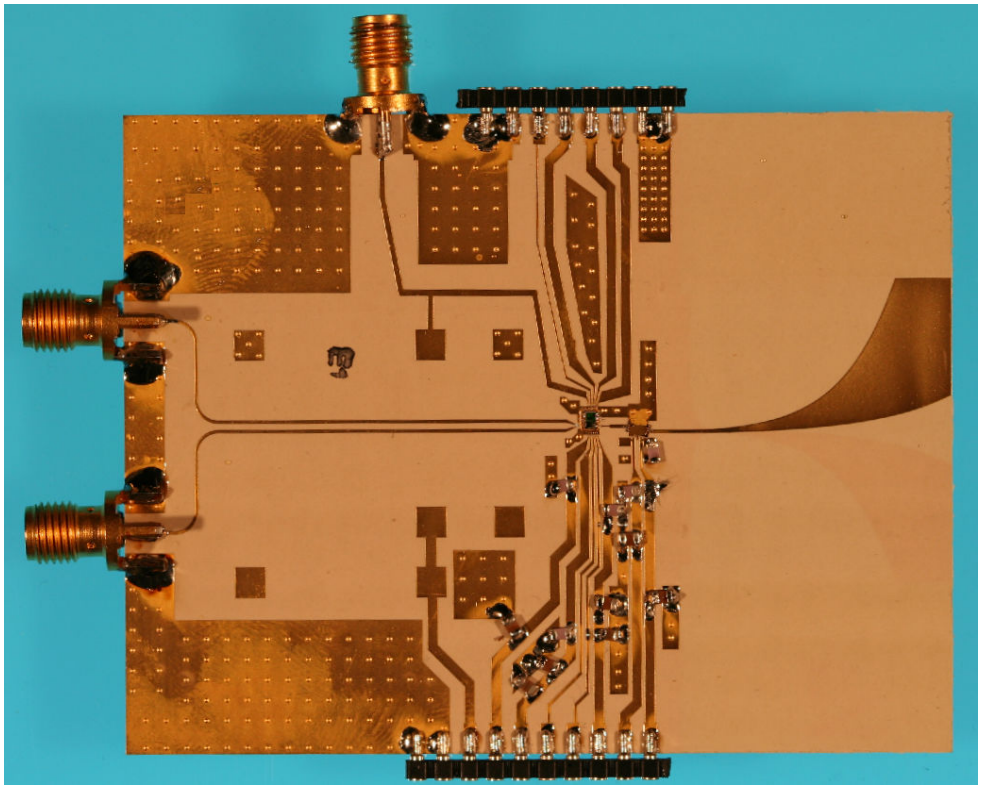


Figure 7.8. Transmitter board.

7.2 Single tone measurements

7.2.1 Transmitter board

The single-tone measurement setup for the transmitter is shown in figure 7.9. The 5 GHz single-tone signal is generated by a signal source and it is up-converted to 60 GHz by the transmitter. It is then fed into the Vivaldi antenna and radiate into the space. A waveguide horn antenna receives the transmitted 60 GHz signal. This signal is the down-converted by a harmonic mixer and fed into a spectrum analyzer. The 109.375 MHz reference frequency is generated by a low-phase-noise source.

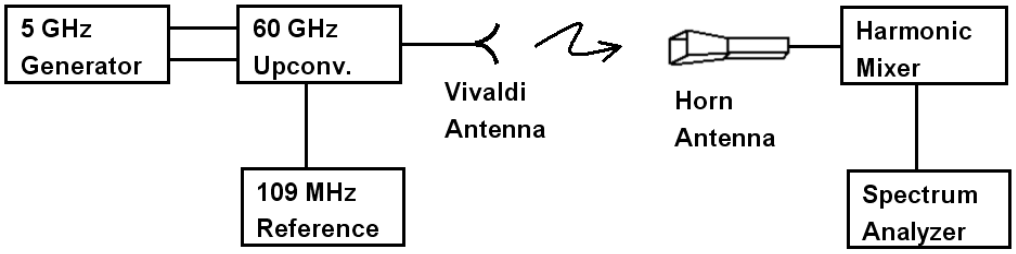


Figure 7.9. Transmitter single-tone measurement setup.

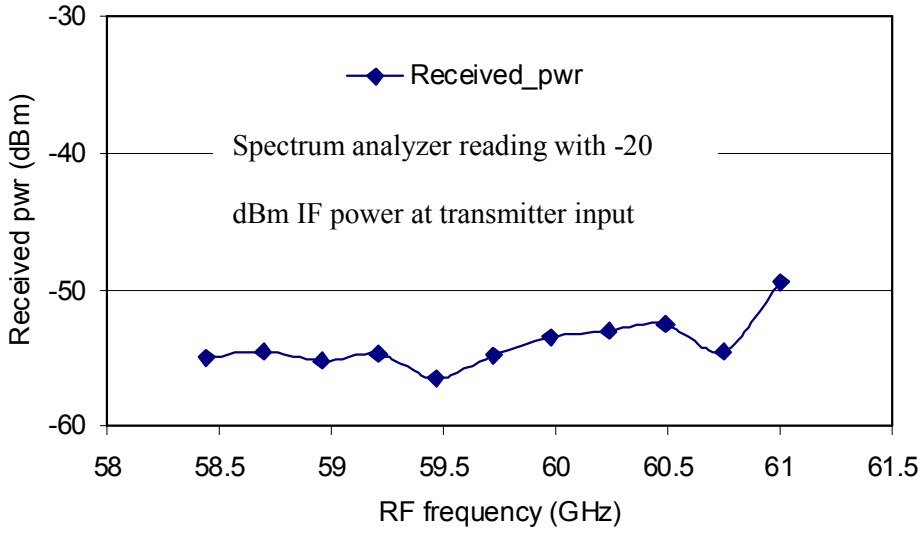


Figure 7.10. Received power by horn antenna at 1 m distance between transmitter board and horn antenna.

In this transmitter chip, the PLL locks from 53.4 to 56 GHz corresponding to 58.4 to 61 GHz RF frequency with a fixed 5 GHz IF frequency. Figure 7.10 shows the transmitter frequency response including bond-wires, antennas and a free-space line-of-sight (LOS) wireless channel of one meter. Its input signal is fixed at 5 GHz and the power is set to be –20 dBm, which is right before P_{1dB}. The reference frequency is changed in the whole PLL locking range so as to the RF transmitting frequency. Within the whole locking range, the received power is ranging from -49.4 (at 61 GHz) to –56.5 (at 59.5 GHz) dBm. The antenna gains are 9 and 12 dB for Vivaldi and horn antennas, respectively. If the 1 m free-space loss is assumed to be –68 dB at 61 GHz, we can calculate back the output power before Vivaldi antenna. The power fed into Vivaldi antenna at 61 GHz is:

$$P_{Vivaldi} = -49.4_{\mathrm{Re}ceiverdPower} - 12_{Horn} - 9_{Vivaldi} + 68 = -2.4dBm\,.$$

This power is after the bond-wire and its compensation structure. Since the Vivaldi antenna is single-ended, an on-chip 50 Ω resistor is used to connect one output path to ground in order to achieve a balance between the two differential paths. We can expect a 3 dB higher output power if a differential antenna is available.

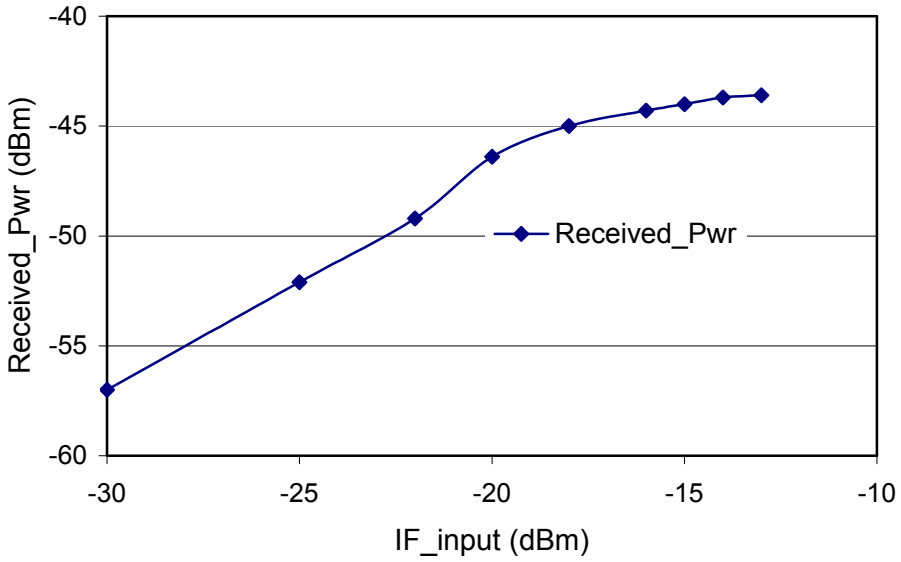


Figure 7.11. Transmitter linearity measurement, received by horn antenna with PLL locked to 56 GHz, 5 GHz IF and 1 m distance.

Transmitter linearity measurement is shown in figure 7.11 with the setup of figure 7.9. Input IF power is swept from –30 dBm to –13 dBm. Measurement shows a P_{1dB} of –46 dBm corresponding to –19 dBm of IF input power. At –13 dBm, the transmitter is fully saturated.

Figure 7.12 shows the maximum output power for a fixed LO frequency of 56 GHz, where the free-space distance is one meter and the input power is fixed at –13 dBm. The maximum received power is –38 dBm at an IF frequency of 6.5 GHz, which corresponds to an RF frequency of 62.5 GHz. The measured 3 dB bandwidth is from 5 to 8.5 GHz corresponding to an RF frequency from 61 to 64.5 GHz.

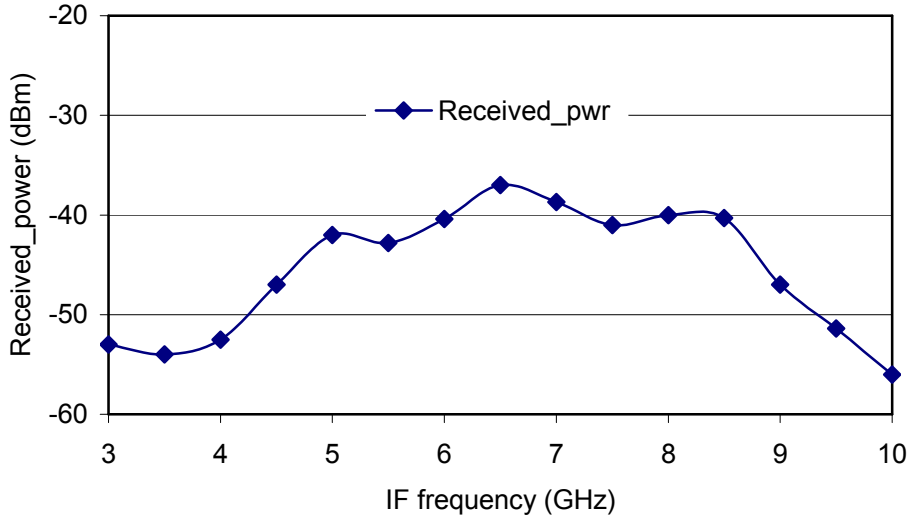


Figure 7.12. Maximum received power with 1 m distance at –13 dBm IF power.

7.2.2 Receiver board

A single tone measurement is also performed for the receiver board. The measurement setup is depicted in figure 7.13. The single tone signal is generated by a generator and fed into a horn antenna. The radiated signal is received by the on-board Vivaldi antenna and down-converted to 5 GHz IF by the receiver chip. An external 180-degree power combiner is used to transform the differential IF signal to a single-ended signal, which is then measured by a spectrum analyzer. The reference signal is generated by a low-phase-noise source.

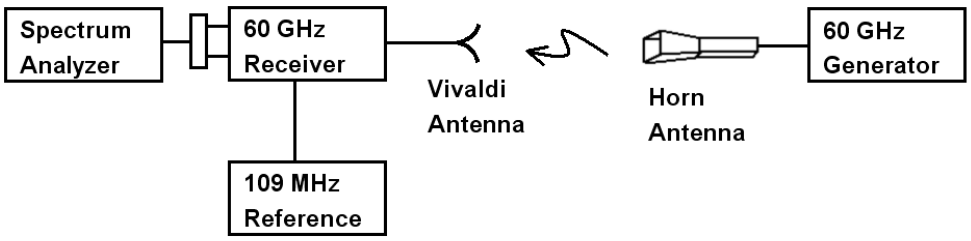


Figure 7.13. Receiver-board single-tone measurement setup.

The RF frequency response is plotted in figure 7.14 within the whole PLL locking range, where the free-space distance is one meter. PLL output frequency is changed via tuning the reference frequency. The frequency of 60 GHz generator is

changed accordingly to obtain a fixed 5 GHz IF. RF power is fixed to be 12 dBm before the horn antenna. The 5 GHz IF output power is plotted with respect to RF frequency. It has a variation of about 3 dB in the whole PLL locking range. The frequency response is similar to that in figure 5.5 implying a flat 60 GHz channel response. To verify the link budget, we calculate receiver output power by using the previous assumptions. Receiver output power at 5 GHz is:

$$Rx_{output} = 12_{source} + 12_{antt.} - 68_{FreeSpace} + 9_{antt.} + 19_{\mathrm{Receiver}} = -16dBm .$$

In a wireless measurement, there are many types of errors, such as antenna misalignments in direction or polarization, channel variations with time and reflections of the measurement environment. A small mistake can lead to a big error. In reality, the measured output power is –17.5 dBm which agrees with the calculation.

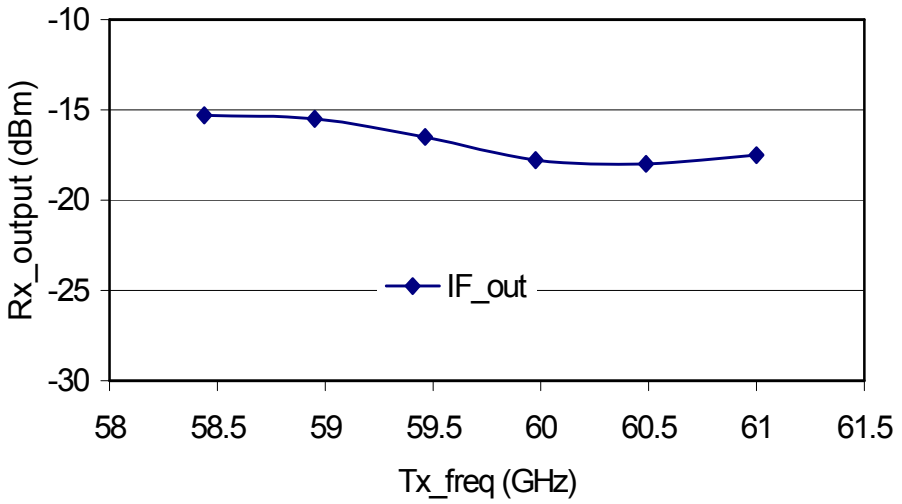


Figure 7.14. RF frequency response of the receiver board.

Another wireless measurement is performed corresponding to the on-wafer measurement in figure 6.2. The measurement result is shown in figure 7.15. PLL is fixed at 56 GHz and the transmitted frequency is swept from 58 GHz to 67 GHz. The measured peak is at 61 GHz corresponding to a 5 GHz IF. It has a measured 3 dB bandwidth from 59.5 to 63.5 GHz. This frequency response is similar to that in figure 6.2, where the band-pass response is due to the IF output matching topology. The small ripples in the measurement are mainly due to the errors of the wireless channel as mentioned above.

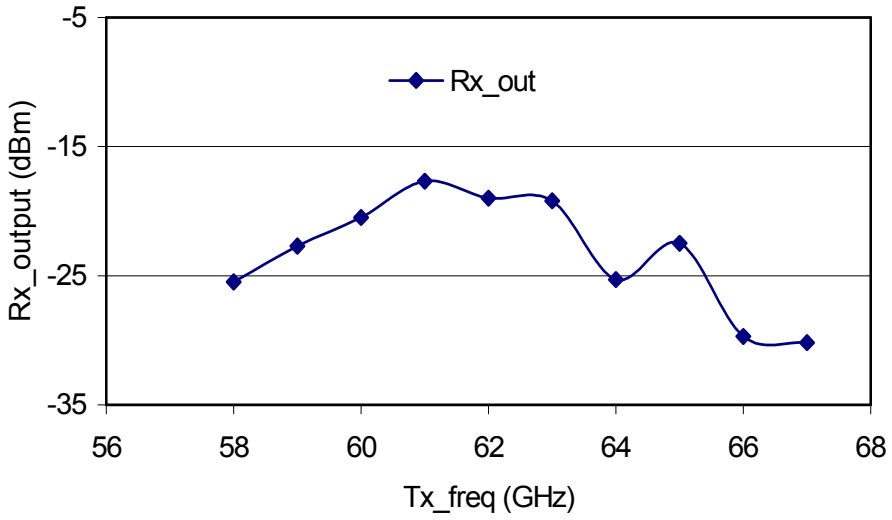


Figure 7.15. Frequency response of the receiver board with fixed LO frequency (PLL is fixed at 56 GHz, 12 dBm power at horn-antenna input, distance is 1 m).

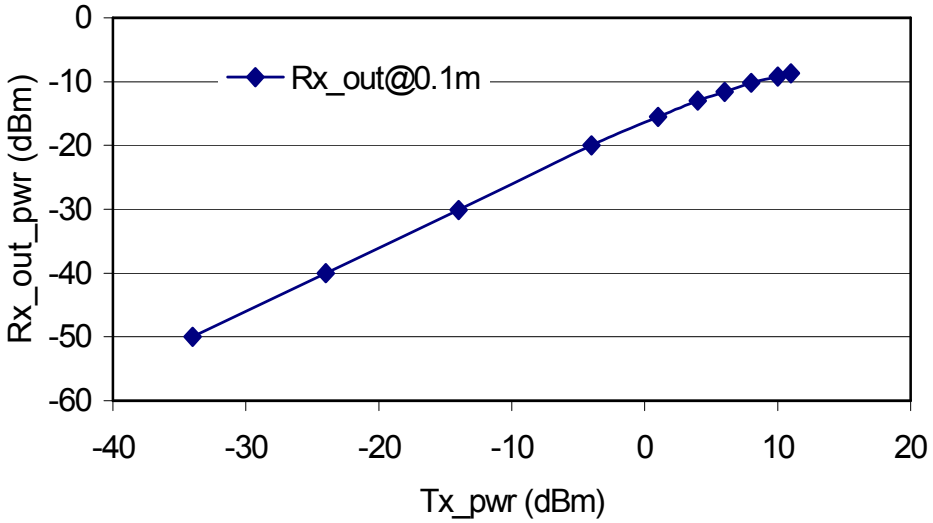


Figure 7.16. Linearity of the receiver board in a 0.1 m free-space channel.

The linearity measurement of the receiver is shown in figure 7.16, where the space distance is reduced to 0.1 meter in order to have the receiver saturated. The PLL is fixed at 56 GHz, and RF is 61 GHz. Measurement shows an output P_{1dB} of –13 dBm with 4 dBm transmitted power.

7.3 Single carrier QPSK measurement

A single-carrier QPSK measurement is carried out before the OFDM measurement. The measurement setup is shown in figure 7.17, where the 5 GHz

modulator and demodulator have been reported in [42]. The base-band (BB) signal is generated by a vector signal generator and fed into the 5 GHz QPSK modulator. The BB signal sink is a vector signal analyzer, which displays the received data constellation.

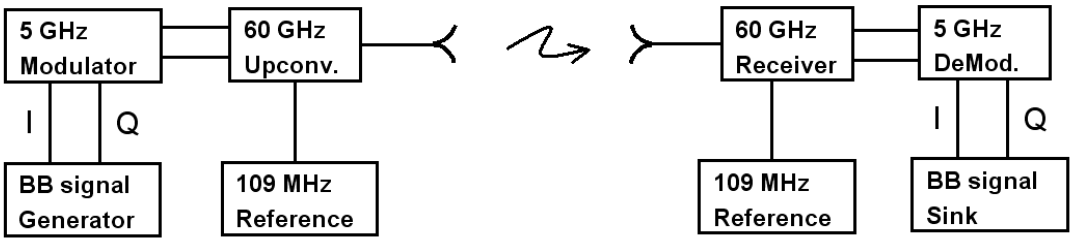


Figure 7.17. Transceiver measurement setup.

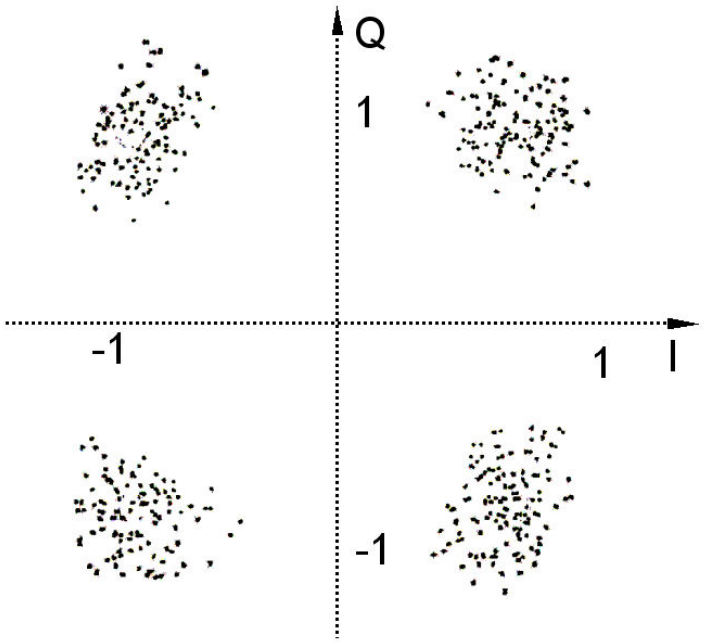


Figure 7.18. Transceiver constellation measurement for single-carrier QPSK.

The measured single-carrier constellation is plotted in figure 7.18, where a 250 Mbit/s single carrier QPSK signal is used. The distance between the transmitter and the receiver is one meter and the measured SNR is about 15 dB. According to the measured constellation diagram, an error-free-transmission is possible even without any coding and decoding technique. In the previous measurement, the transmitter is working close to its P_{1dB}. The constellation becomes worse with increase of distance. Without coding and decoding techniques, an error-free-transmission is not possible above 2 meters. A PA would be very helpful for a longer distance transmission. In this setup, the highest data-rate is limited by the signal source to 480Mbit/s.

7.4 OFDM measurement

The measurement setup in figure 7.17 is used for the OFDM test, where the OFDM signal is generated from a commercial FPGA board with a digital-to-analogue converter (DAC). The BB sink is another FPGA board with an analogue-to-digital converter (ADC). A 500 MHz low-pass-filter (LPF) is inserted before the receiver ADC. The received data are converted into digital signals and stored into the receiver memory. FFT transformation is used to separate the sub-carriers, and Matlab is used to process the stored data and to compare them with the source data.

An OFDM QPSK constellation is shown in figure 7.19, where the space distance is one meter and the data-rate is 240 Mbit/s with a ½ coding scheme. After the use of coding and decoding technique, an error-free transmission is achieved. The SNRs for each sub-carrier are calculated by Matlab after demodulation, and they are plotted in figure 7.20. The measured average SNR is 12.5 dB. It becomes worse with increase of distance because of the low transmission power. Note that the transmitted power is approximately 6 dB less than that in the single-carrier QPSK measurement because OFDM signals require a linear amplification. Error-free transmission is possible up to 2.5 meters for a data-rate of 240 Mbit/s.

In order to achieve a higher throughput, more sophisticated modulation schemes have to be adopted. However, this requires a higher linearity in transmitter, or more power back-off. Figure 7.21 is the constellation of an OFDM 16 QAM measurement and its sub-carrier SNRs are plotted in figure 7.22. The data-rate is 720 Mbit/s with a ½ coding scheme at a distance of 0.5 meter. The measurement shows an error-free transmission and an average SNR of 15 dB. A maximum data-rate of 1080 Mbit/s is achieved with a distance of 15 cm, as is shown in figure 7.23, where an OFDM 64 QAM signal with a 3/4 coding scheme is used. Its average SNR is about 23 dB, which is shown in figure 7.24. The short distance is because more back-off is required by the OFDM 64 QAM signal, so that the transmitter works in its linear region. This demonstrator achieved less transmission distance than the one developed in IBM due to the lack of a power amplifier.

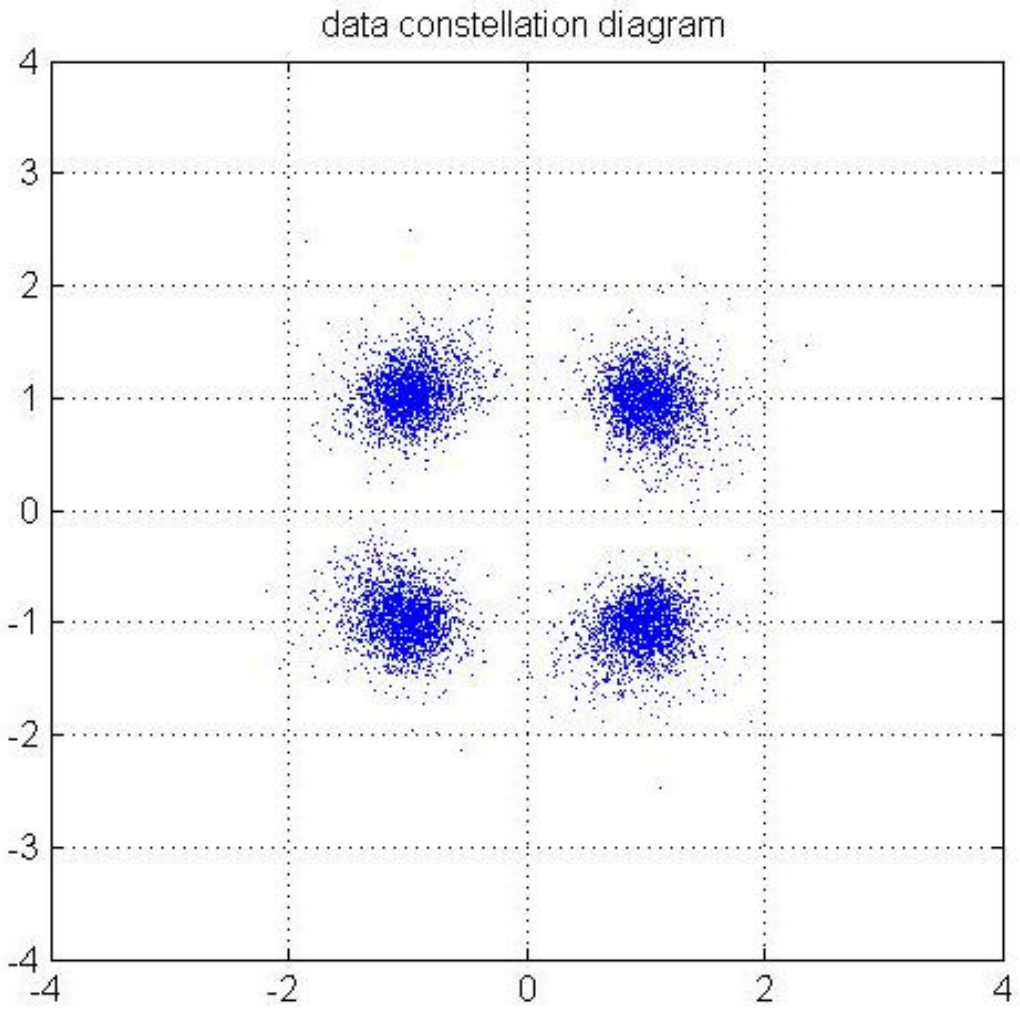


Figure 7.19. OFMD QPSK constellation measurement.

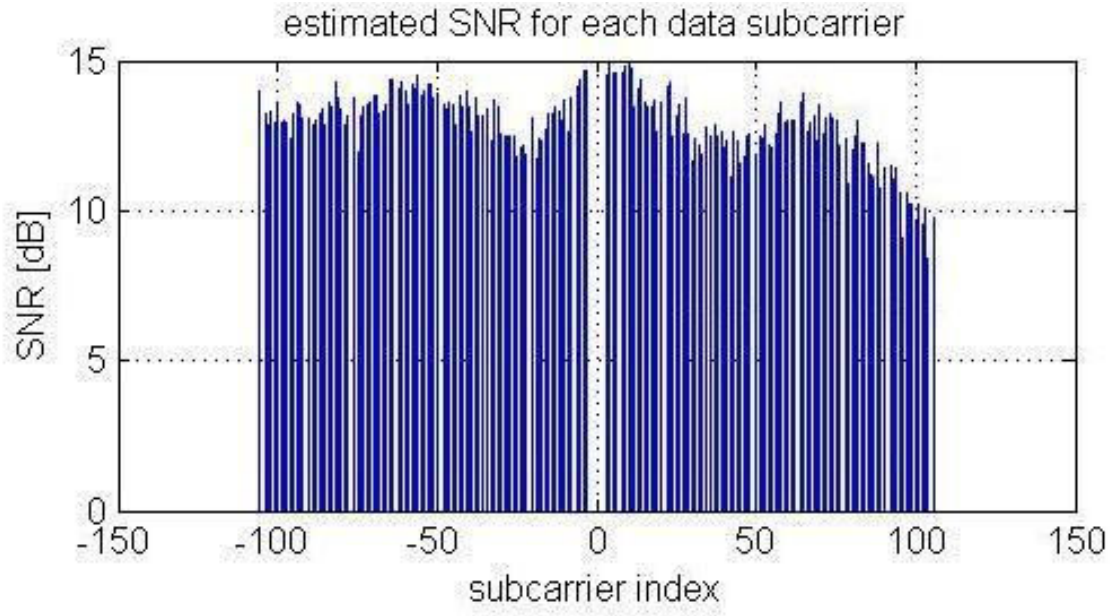


Figure 7.20. Sub-carrier SNR measurement of OFDM QPSK.

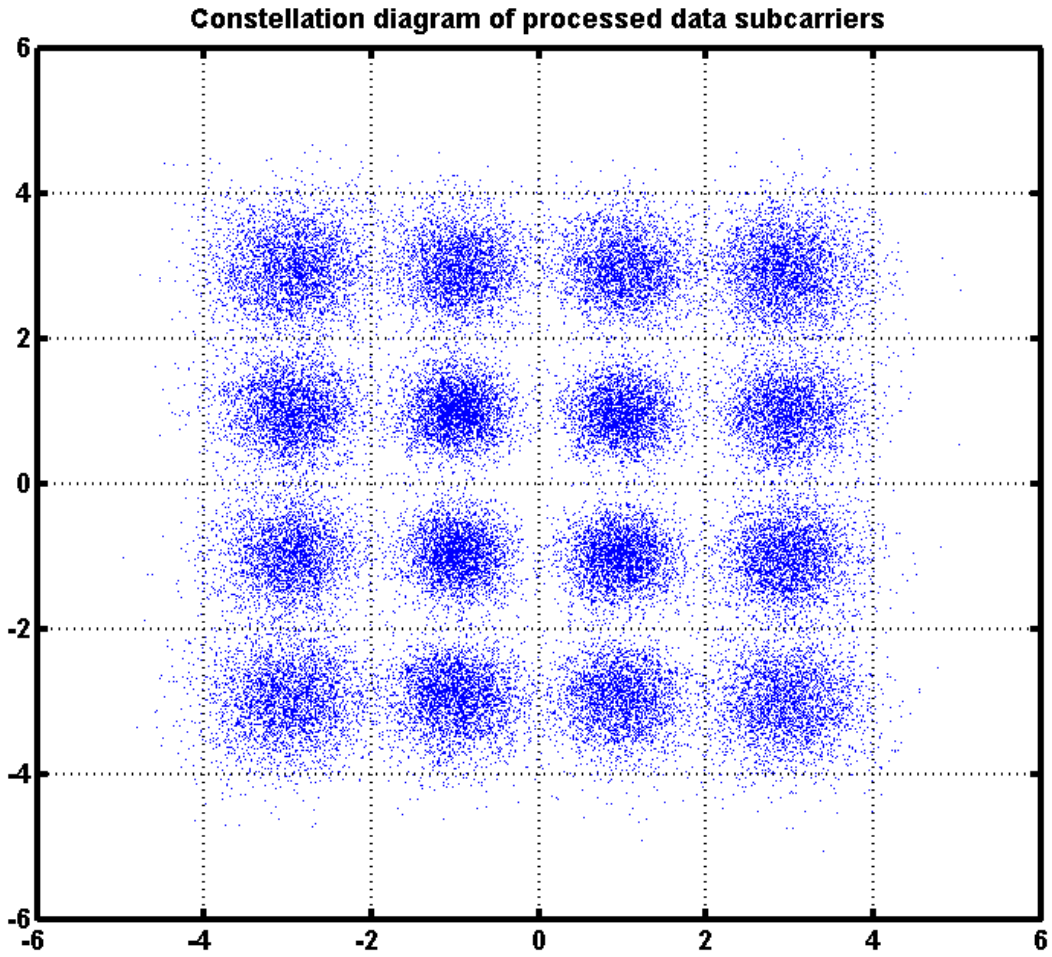


Figure 7.21. OFDM 16 QAM constellation measurement.

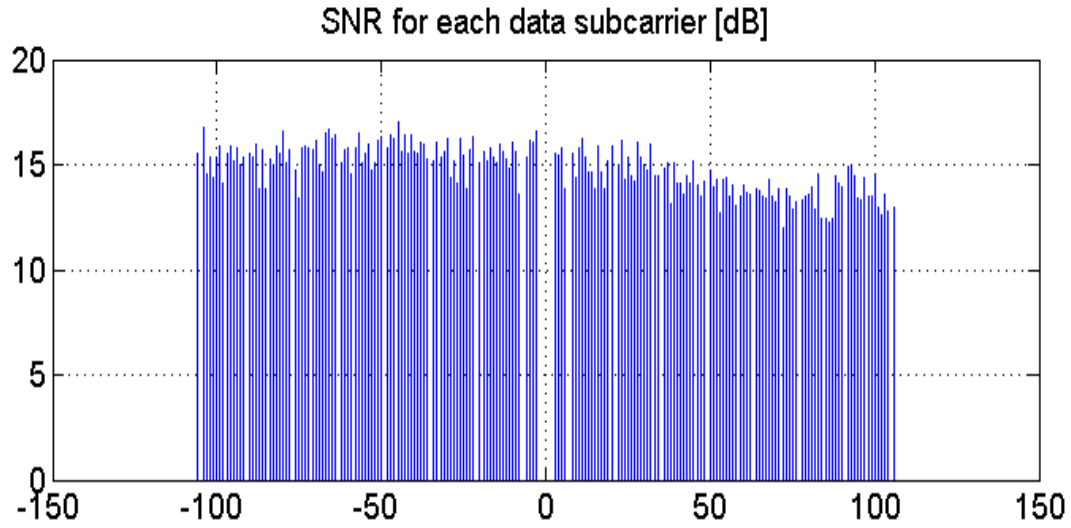


Figure 7.22. Sub-carrier SNR measurement of OFDM 16 QAM.

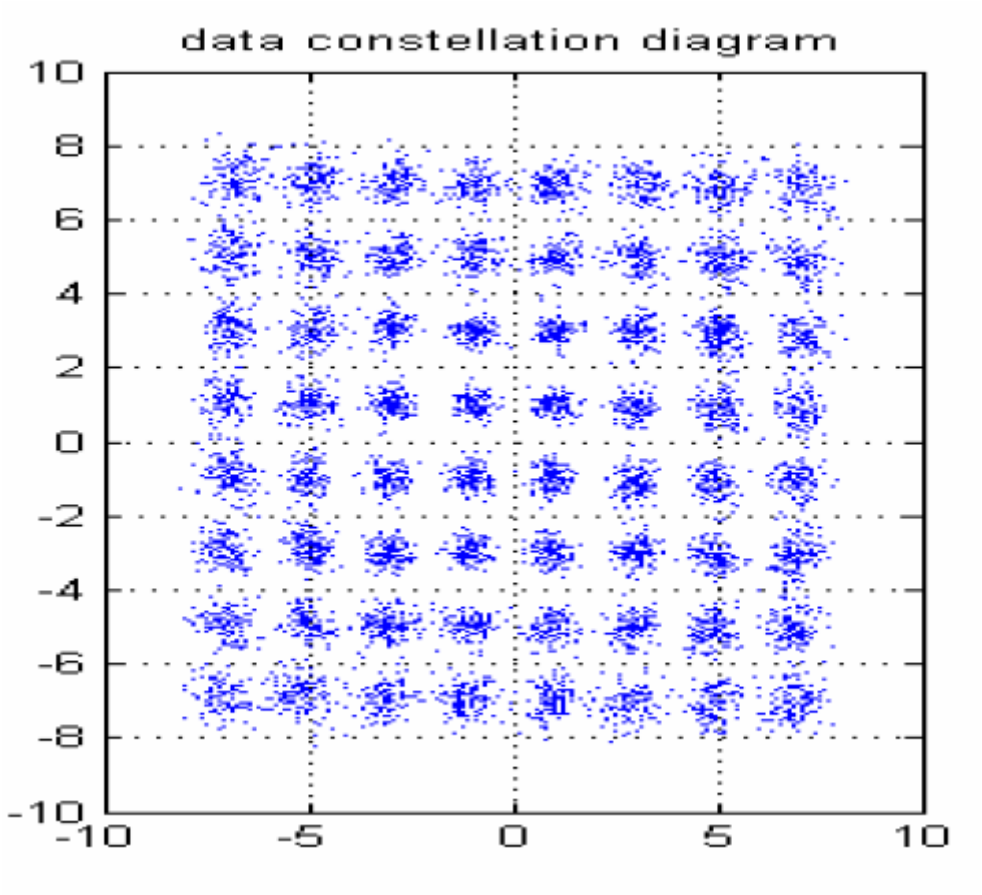


Figure 7.23. OFDM 64 QAM constellation measurement.

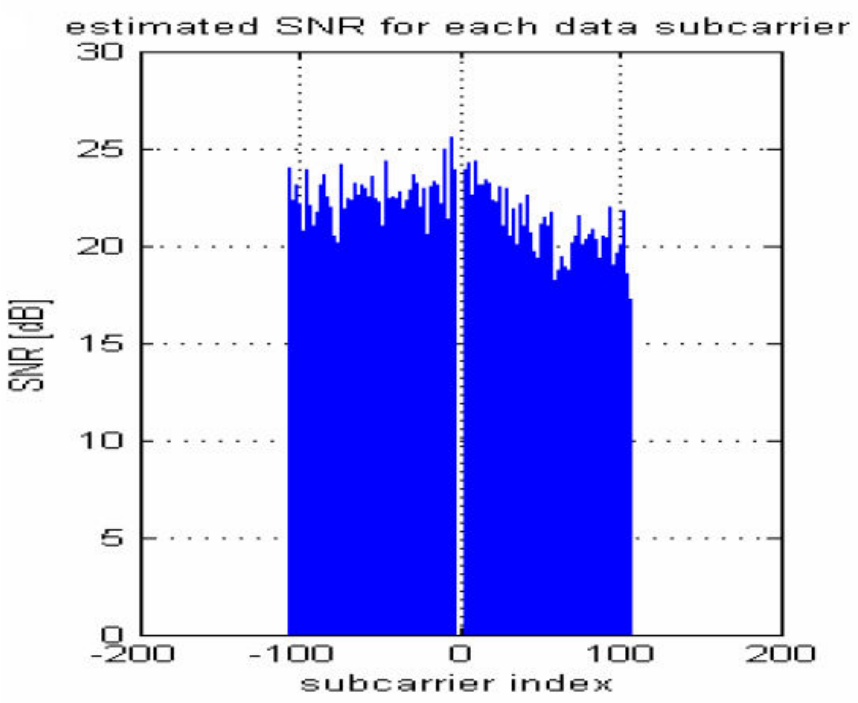


Figure 7.24. Sub-carrier SNR measurement of OFDM 64 QAM.

Summary

The board design issues and the system level measurements of the two 60 front-end chips have been discussed in this chapter. The transmitter and receiver boards are designed in low-loss Rogers material with a carefully designed cavity to hold the chips and to reduce the bond-wire inductances. A bond-wire compensation structure is introduced on board. Vivaldi antennas are integrated on-board, which are placed very close to the chips. Horn antennas are used as a reference for the transmitter and receiver tests. The measurement results agree with the link budget estimation. The transmitter and receiver boards have been measured together with a 5 GHz transmitter/receiver pair. They are used as IF modulator and demodulator. Both single-carrier and OFDM signals are applied to the system. Up to 2 meters, an error-free transmission is measured for a single-carrier QPSK signal of 250 Mbit/s and an OFDM signal of 480 Mbit/s. The highest measured throughput is 1080 Mbit/s with an OFDM 64 QAM modulation scheme.

Chapter VIII Conclusion

A complete design of a 60 GHz front-end demonstrator has been presented in this thesis. It has been tested in a real in-door environment and error-free data transmissions have been achieved. The maximum achieved data-rate is 1080 Mbit/s. Furthermore, this demonstrator has the lowest cost among the existing 60 GHz demonstrators. In mass productions, silicon technologies have the lowest cost. All III/V based 60 GHz demonstrators have higher chip costs and a low integration level, thus a higher overall cost. The only other silicon-based demonstrator developed in IBM has similar chip cost. However, a special technique is used in their antenna assembly, which increases the packaging cost.

The necessary information concerning transceiver architectures from literatures are summarized and a heterodyne architecture with a 5 GHz IF is proposed. It is compatible to IEEE 802.11a allowing the reuse of some building blocks to build a 5 GHz transceiver. Its link budget is given according to the performances of the building blocks. Design theories of mixers and amplifiers are summarized since they are the main building blocks in a transceiver front-end. There are two main challenges in designing a 60 GHz transceiver system, which are the designs of building blocks and the packaging. They are solved through chapter IV to VII.

Two 60 GHz LNAs have been designed and fabricated: a common-emitter three-stage differential LNA and a two-stage cascode LNA. Different inductor structures have been simulated and compared with respect to their Q-factors and chip areas. As a result, the MTL and ML type inductors are used in these designs. Bond-pads are troublesome at millimeter wave because they introduce extra parasitic losses. They are shielded and incorporated into the input and output matching topologies. The gains of the CE and cascode LNAs are 18 and 20 dB, respectively. Their simulated noise figures are between 6 to 7 dB. Good agreements between simulation and measurement have been achieved, which is of importance for first-time-correct designs.

Two active mixers, a differential and a single-ended, have been designed with the topologies of a Gilbert cell and half of a Gilbert cell. The Gilbert cell mixer is a fully differential design, and it is optimized to work with the differential CE LNA. The single-ended mixer requires a single-ended RF input signal and has a differential output, which is optimized to work with the single-ended cascode LNA. They have similar output buffers and output matching structures. The mixers are optimized to have a filter-like frequency response eliminating the use of an IF filter. They have similar conversion gains of about 10 dB and noise figures of about 14 dB. The differential CE LNA and the Gilbert cell mixer have been integrated together with an existing 56 GHz PLL in a differential receiver front-end. In transmitter, the building blocks include an up-converter and an output buffer. They are designed and integrated in the first run.

Bond-wires are used for inter-connections between chips and boards because it is the cheapest way of packaging. A cavity is used to hold the chips, so that they have the same top surface as the boards reducing the length of the bond-wires. Many short bond-wires in parallel are used for ground pads to guarantee a low inductance connection. Furthermore, a bond-wire compensation structure is introduced on-board to compensate for the mismatch caused by the RF bond-wire. An existing Vivaldi antenna is also integrated into the application boards. The transmitter and receiver boards have been measured in an indoor wireless channel, the results agree with the link budget predictions. Both OFDM and single-carrier QPSK signals have been applied to the 60 GHz demonstrator, and clear constellations have been measured.

From the results of this thesis, it is feasible to design a low-cost integrated transceiver working at 60 GHz in silicon technologies. It is necessary to integrate a PA into the transmitter chip to achieve a longer distance. The cost can be further reduced if the antennas are designed by using bond-wires.

Appendix

List of abreviations

ADC	analog to digital converter
ADS	advanced design system
APDP	anti-P-parallel diode pair
ASK	amplitude shift keying
BB	baseband
BFSK	binary frequency shift keying
BPF	band pass filter
BPSK	binary phase shift keying
BMBF	Bundesministerium für Bildung und Forshcung
BVceo	collector emitter breakdown voltage with base open
CE	common emitter
CMOS	complementary metal-oxide-semiconductor
COB	chip-on-board
CPW	coplanar waveguide
DAC	digital to analog converter
EM	electromagnetic
FE	front end
FET	field effect transistor
FFT	fast Fourier transformation
FSK	frequency shift keying
GMSK	Gaussian minimum shift keying
H1	a high performance SiGe BiCMOS process from IHP
HB	harmonic balance
HBT	heterojunction bipolar transistor

HDTV	high definition television
IC	integrated circuits
IF	intermediate frequency
IFFT	inverse fast Fourier transformation
IQ	in-phase and quadrature
IRM	image rejection mixer
ISM	industrial, scientific and medical
KCL	Kirchoff's current law
LNA	low noise amplifier
LO	local oscillator
LOS	line of sight
LPF	low pass filter
MAC	media access control
MIM	metal-insulator-metal capacitor
MIMO	multi-in-multi-out
ML	metal line
MMIC	microwave monolithic integrated circuit
MSK	minimum shift keying
MTL	microstrip transmission line
NF	noise figure
NFmin	minimum noise figure
NLOS	non-line-of-sight
OFDM	orthogonal frequency division multiplexing
OOK	on off keying
PA	power amplifier
PCB	printed circuit board
PLL	phase locked loop
QPSK	quatrature phase shift keying

RF	radio frequency
RFIC	radio frequency integrated circuits
RMSDS	rms delay spread
rpnd	n-type poli-resistor
rppd	p-type poli-resistor
rsil	siliside resistor
RX	receiver
SNR	signal to noise ratio
SPM	subharmonically pumped mixer
SSB	single side band
TCL	tail current source
TG3c	IEEE 802.15 Task Group 3c
TPN	two port network
TX	transmitter
USC	unity smith chart
VBIC	vertical bipolar inter-company
VCO	voltage controlled oscillator
VGA	variable gain amplifier
WLAN	wireless local area network
WPAN	wireless personal area network
ZIF	zero intermediate frequency

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