CMOS SOI technology for WPAN. Application to 60 GHz LNA

A.Siligaris, C.Mounet, B.Reig, P. Vincent and A.Michel

***Abstract*—This paper discusses the design of a 60 GHz Low Noise Amplifier (LNA) using a standard low power SOI CMOS process from ST Microelectronics. First, we outline the technology as well as the mm-wave design challenges. Using recent work on Coplanar Waveguide (CPW) modeling, we describe how it's possible to use parametric, 3D electromagnetic simulation to complete or replace analytical models of on-chip passive devices. A short description of the transistor model is also provided. Finally, we discuss the details of the LNA design and show how the simulation results compare to the measurements.**

***Index Terms*—LNA, 60GHz, RF modeling, CMOS, SOI.**

I. Introduction

Recently, much effort has been performed in order to develop millimeter wave circuits for 60 GHz wireless applications. SOI CMOS technology is a good candidate for such applications because it offers high quality passive elements and good substrate isolation due to high resistivity substrate [1]. Accurate modeling up to high frequency of passive as well as active devices of a technology is needed for robust circuit design. Moreover, models have to be available for both steady state (harmonic balance) and transient simulations.

In this paper we show the modeling flow for passive and active elements applied to a standard industrial SOI CMOS 65nm technology from STM. The generated models are used to design circuits for 60 GHz applications. Finally, we discuss the design of an LNA at 60GHz and show how the simulation compares to the measurements.

II. Modeling SOI CMOS 65nm Technology

The LNA was implemented in low power SOI 65nm SOI process. This technology features a back-end with six copper metal layers on which an aluminum cap-layer is added.

One key parameter for reliable design at millimeter wave frequencies is accurate modeling of the transistors as well as the transmission lines (TL) and parasitic. The 65nm SOI design kit provides a BSIM4 model for the standard CMOS design flow. Nevertheless, the model has not been extracted and validated for high frequency applications. For that reason, we have used an empirical model with the benefit of fast extraction and accuracy which has been verified from DC to 110 GHz [2], [3]. Figure 1 shows a comparison of the measured and simulated S parameters of a 50µm large transistor (40 gate fingers). The transistor is biased at moderate inversion (Vg=0.8V) and saturation (Vd=1.2V). A good matching is obtained from low frequency to 110GHz. The model was implemented in Nexxim, state of the art circuit simulator (Ansoft), with care taken to make the model to work seamlessly and accurately in both time and frequency domain. As an example, figure 2 shows the time domain output voltage of the transistor simulated with both a transient simulation and HB in steady state.

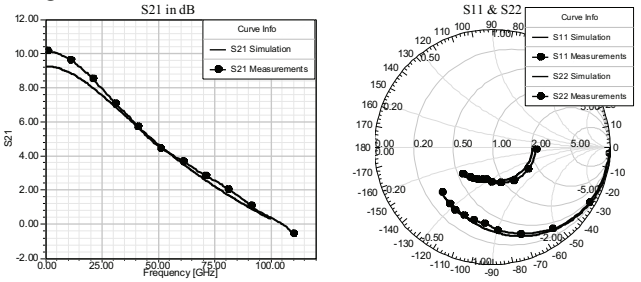

Fig. 1. Measured and simulated S parameters of a 50µm SOI CMOS65nm transistor up to 110GHz.

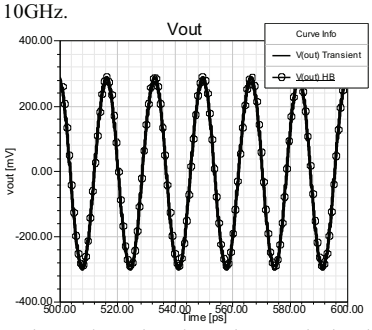

Fig. 2. Output voltage time domain voltage calculated with transient simulation and steady state HB.

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A.Siligaris, C.Mounet, B.Reig, P. Vincent are with the CEA/LETI-MINATEC, Grenoble, 38054, France (phone: +33 4 38 78 17 38; e-mail: alexandre.siligaris@cea.fr).

A.Michel is with Ansoft Corporation, 153 Rue Fourny BP 513, 78535 Buc, France.

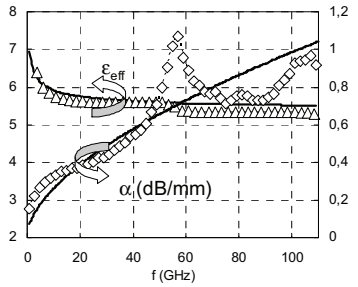

Fig. 3. Measured (symbols) and simulated (solid lines) insertion loss and effective permittivity.

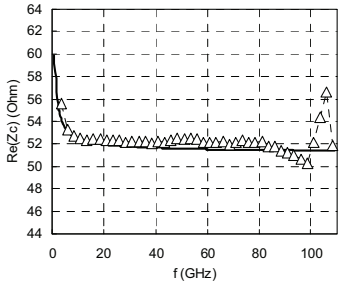

Fig. 4. Measured (symbols) and simulated (solid line) real part of the characteristic impedance up to 110 GHz.

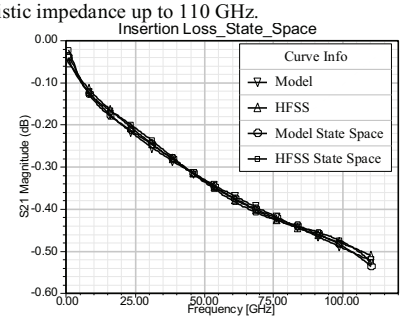

Fig. 5. State Space compared to originated S parameters.

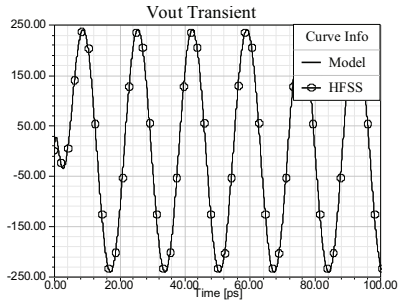

Fig. 6. Transient simulation results.

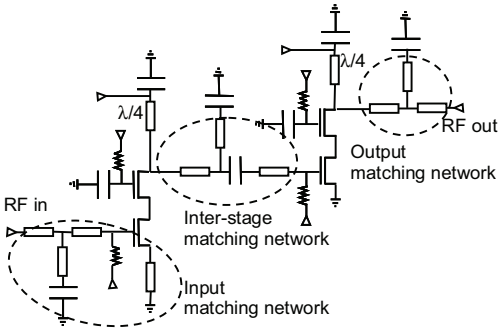

Fig. 7. Schematic of electrical circuit of a 60 GHz 2-stage LNA implemented in SOI CMOS technology.

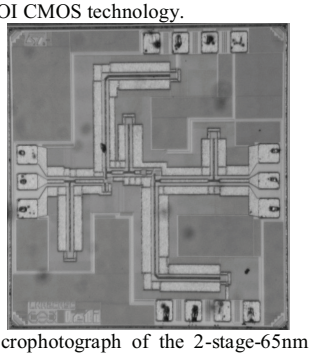

Fig. 8. Chip microphotograph of the 2-stage-65nm 60 GHz LNA. Dimensions : 0.96x1.05 mm2.

CPW modeling is undertaken through 3D full wave simulations with HFSS of Ansoft. We use the flexibility and accuracy of 3D EM analysis to build accurate analytical model using previous work done on CPW modeling [4]. Figure 3 compares simulations and measurements of the attenuation, and the effective permittivity of a CPW line. The characteristic impedance is shown in figure 4. Very good agreement is observed between measured and simulated data.

Some of the blocks of the transceiver, like the VCO or the frequency Divider (frequency synthesis), will need to be simulated both in frequency domain (harmonic balance) and time domain (transient). So, it is very important at the modelling stage to validate the model in both frequency and time domain. The analytical and HFSS models are frequency dependent and are seen as an S parameter file by the simulator. Nexxim's standard transient solution for S-parameters uses a state-space formulation to represent the model in the time domain, which is also guaranteed to be causal. This is highlighted in figure 5 which shows perfect match between S parameter and state space formulation of the insertion loss of the CPW transmission line. We also run a transient simulation with analytical model and HFSS model as shown in figure 6. We observe that transient simulation works with the transmission line even though the line model is defined in the frequency domain.

III. Low Noise Amplifiers in 65-nm SOI CMOS

A 2-stage low noise amplifier was implemented in the CMOS65nm SOI technology. The amplifier uses a cascode topology for each stage (figure 7), because it offers higher isolation and gain than the common source (CS) topology. Moreover, the cascode topology ensures an unconditional stability for the amplifier in the 0-110GHz frequency range. The input, the output, and the inter-stage matching networks are constructed from series CPW transmission lines and short ended stubs. The drain biasing of each stage is achieved through λ/4 at 60 GHz short ended stubs. The circuit has been designed with the help of the previously described models. The photograph of the chip is shown in figure 8. On wafer measurements were performed with an HP-8510XF VNA up to 110 GHz. Figure 9 shows the simulated and the measured

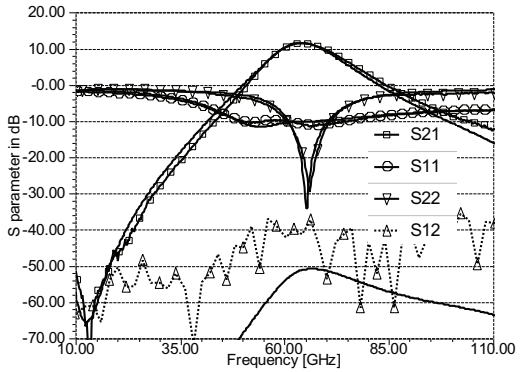

Fig. 9. Simulated and measured S parameters of the 2-stage-65nm LNA. Symbols: measured. Solid lines: simulated.

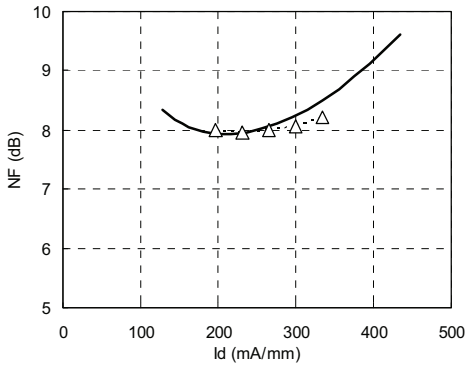

Fig. 10. Measured (symbols) and simulated (solid line) noise figure at 60 GHz versus the current density of the first cascade stage.

S-parameters of the 2-stage-65nm LNA. The gain of the amplifier is 12 dB at 64 GHz, while the input and output matching are better than -10 dB. From figure 9 we observe that very accurate simulation is obtained for the full chip, thanks to accurate active and passive models. The LNA consumption is 36mW under 2.2V voltage supply.

The noise figure of the LNA was measured at only one frequency point. Indeed, with the available noise measurements facilities it was only possible to measure at 60GHz. The measured noise figure of the LNA is shown in figure 8 versus the current density of the first stage of the LNA. We observe that the noise figure is 8dB and shows a very small variation when the first stage transistor is biased at weak or moderate inversion.

Table 1 summarizes the LNA's performances in which we have added the input power compression point which was measured at 64GHz.

IV. Conclusion

In this paper we have described the design flow of a 60GHz LNA in a standard CMOS SOI technology. First we presented the modeling approach for transmission lines as well as for transistors. Passive elements are modeled with the help of HFSS 3D electromagnetic simulator, whilst the transistors use an empirical high frequency oriented CMOS model. Finally, we describe the design and the performances of a key element, the LNA.

TABLE I
Summary of the LNA's measured performances.

S21	S11	S22	NF	ICP_{1dB}	P_{dc}
12 dB (64GHz)	<-10dB (64GHz)	<-20 dB (64GHz)	8dB (60GHz)	-5dBm (64GHz)	36mW

Acknowledgement

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References

[1] F.Gianesello et al., "State of the art integrated millimeter wave passive components and circuits in advanced thin SOI CMOS technology on high resistivity substrate," IEEE SOI Conference Proceedings, pp. 52 – 53, Oct. 2005.

[2] A.Siligaris, G.Dambrine, D.Schreurs, F.Danneville, "A new empirical nonlinear model for sub-250 nm channel MOSFET ," IEEE Microwave and Wireless Components Letters, Vol. 13, Issue 10, pp:449 – 451, Oct. 2003

[3] A.Siligaris, G.Dambrine, D.Schreurs, F.Danneville, "130-nm partially depleted SOI MOSFET nonlinear model including the kink effect for linearity properties investigation," IEEE Transaction on Electron Devices, Vol. 52, Issue 12, pp:2809 – 2812, Dec. 2005.

[4] Siligaris et al, "CPW and discontinuities modeling for circuit design up to 110 GHz in SOI CMOS technology," IEEE Radio Frequency Integrated Circuits (RFIC)Symposium proceedings, pp: 295 – 298, June 2007.