35–65-GHz CMOS Broadband Modulator and Demodulator With Sub-Harmonic Pumping for MMW Wireless Gigabit Applications

Jeng-Han Tsai, *Student Member, IEEE*, and Tian-Wei Huang, *Senior Member, IEEE*

***Abstract*—Sub-harmonic modulator and demodulator are presented in this paper using 0.13-μm standard CMOS technology for millimeter-wave (MMW) wireless gigabit direct-conversion systems. To overcome the main problem of local oscillator (LO) leakage in direct-conversion systems, the sub-harmonically pumped scheme is selected in this mixer design. An embedded four-way quadrature divider is utilized in the sub-harmonic Gilbert-cell design to generate quadrature-phases LO signals at MMW frequency. For broadband applications, a broadband matching design formula is provided in this paper to extend the operational frequency range from 35 to 65 GHz. To improve the flatness of conversion loss at high frequency, high-impedance compensation lines are incorporated between the transconductance stage and LO switching quad of the Gilbert-cell mixer to compensate the parasitic capacitance. The sub-harmonic modulator and demodulator exhibit 6 $\pm$ 1.5 dB and 7.5 $\pm$ 1.5 dB measured conversion loss, respectively, from 35 to 65 GHz. For MMW wireless gigabit applications, the gigabit modulation signal test is successfully performed through the direct-conversion system in this paper. To our knowledge, this is the first demonstration of the MMW CMOS sub-harmonic modulator and demodulator that feature broadband and gigabit applications.**

***Index Terms*—CMOS, demodulator, direct conversion, millimeter wave (MMW), modulator, sub-harmonically pumped.**

I. Introduction

RECENTLY, the Federal Communications Commission (FCC) announced 7 GHz of unlicensed band in millimeter-wave (MMW) frequency bands from 57 to 64 GHz [1]. The FCC allocation provides the possibility of the wireless gigabit communication services, such as wireless personal area networks (WPANs) [2], wireless gigabit Ethernet [3], and point-to-multipoint MMW fiber-radio communication systems [4]. Furthermore, these 60-GHz short-range links provide extra benefits of security, spatial isolation, and frequency reuse, which results from the significant oxygen absorption at kilometer range [2]. To meet the MMW market demands, many researchers have developed highly integrated MMW monolithic integrated circuits. In the past, this research was dominated by III–V semiconductors. Due to the possibility of low-cost silicon and back-end integration, modern CMOS technology with downscaling of transistor dimensions is an interesting alternative for MMW applications. Today 0.13-μm bulk CMOS technology is capable of high-gain amplifications in the 60 GHz [5].

Direct-conversion architecture with advantages of minimal hardware, no image frequency, and wider bandwidths [6] is attractive for broadband MMW applications. Therefore, passive de-modulator and modulator have been reported in various processes [7]–[10] for MMW direct-conversion systems, even gigabit data rate. However, the main problem of local oscillator (LO) leakage must be considered carefully when designing direct conversion transceivers [6]. To minimize the problem, the sub-harmonic pumping technique whose LO frequency is one-half of the desired RF frequency is considered as a potential solution [11]–[15]. In addition, using relatively low LO frequency can decrease the design challenge of a high-power and low phase-noise LO in MMW frequencies [12].

The mixer is a critical component in the demodulator and modulator designs that translates the RF signals to and from baseband signals. Traditionally, mixers using passive topologies in the MMW regime have high conversion loss and large chip size due to the quarter-wave length matching stubs and baluns [16]. Now the high-performance CMOS devices make it possible to consider the fundamental Gilbert-cell mixer for low conversion loss and compact die size in MMW [17]. However, the CMOS sub-harmonic Gilbert-cell mixer has not been demonstrated in MMW for the following reasons.

1) The switching quad of the sub-harmonic Gilbert-cell mixer consists of four parallel connected transistors introduce a larger parasitic capacitance than the fundamental Gilbert-cell mixer, which limits the operation frequencies and bandwidth in the MMW regime.
2) The lack of accurate quadrature-phase LO signals generator in the MMW limits the operation frequencies of sub-harmonic Gilbert-cell mixers.

Furthermore, the MMW CMOS Gilbert-cell-based demodulators and modulators with gigabit direct-conversion capabilities have not been demonstrated.

This paper presents an MMW broadband sub-harmonic modulator and demodulator using 0.13-μm standard CMOS technology for MMW direct-conversion systems. The sub-harmonically pumped technique is selected to minimize the LO leakage problem. For broadband applications, a broadband matching design formula is provided to extend the operational frequency range. To compensate the parasitic capacitance of the CMOS

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The authors are with the Department of Electrical Engineering and Graduate Institute of Communication Engineering, National Taiwan University, Taipei, 106 Taiwan, R.O.C. (e-mail: twhuang@cc.ee.ntu.edu.tw).

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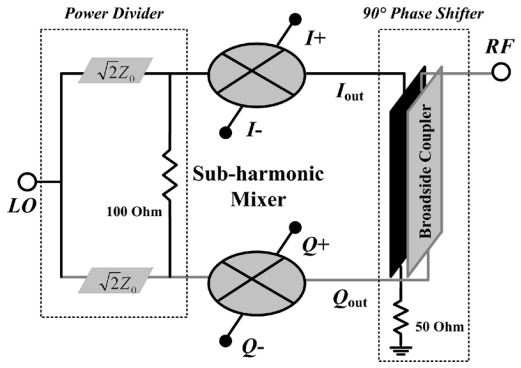

Fig. 1. Block diagrams of the CMOS broadband sub-harmonically pumped modulator and demodulator.

transistor, a high-impedance compensation line is incorporated between the transconductance stage and switching quad to form a third-order Butterworth *LC* ladder network. In addition, an MMW four-way quadrature divider using a 90° coupler and 180° balun have been implemented in the CMOS process to provide equal amplitude and quadrature-phases LO signals for the sub-harmonically pumped modulator and demodulator. Finally, the experimental results show the MMW CMOS sub-harmonic modulator and demodulator MMICs feature good direct-conversion quality up to the gigabit data rate.

II. Operation Principle

The direct-conversion architecture is a promising approach for single-chip transceivers for the following reasons. First, the elimination of the IF circuitry reduces design complexity and minimal hardware. Second, with zero IF, there is no image frequency. Third, the radio channels have wide bandwidths, which make it more suitable for high data-rate systems. However, a well-known problem is the LO leakage because of poor reverse isolation through the mixer. As an upconverter, the LO leakage should be minimized since an unwanted carrier signal at the RF output can degrade the modulation quality. As a downconverter, the LO leakage from the receiver into the antenna becomes an in-band interferer to other nearby receivers tuned to the same band. In addition, LO leakage self-mixing to dc through the mixer cause a more serious dc offset problem in receiver. To minimize these problems, the sub-harmonically pumped technique is considered as a potential solution. With sub-harmonic pumping, the fundamental LO frequency is one-half of the desired RF frequency, therefore, the fundamental component of LO leakage does not appear in the concerned signal frequency bands [13]–[15]. In fact, the LO leakage does not completely eliminate due to the imperfections in the circuit mismatch. However, the sub-harmonically pumped technique is beneficial to reduce LO leakage in the modulator and dc offset in the demodulator.

A block diagram of the sub-harmonic modulator and demodulator are shown in Fig. 1. The sub-harmonic modulator consists of a 90° broadside coupler, a Wilkinson power divider, and two sub-harmonically pumped mixers. The Wilkinson power divider is used to provide good isolation between the input ports of two mixers. The broadside coupler provides a 90° phase shifter at the RF port. The mixers can perform the modulation of the LO with the baseband in-phase (I) and quadrature (Q) modulating signals. Both mixed signals are combined at the output to provide a composite modulated signal. All signals are fully differential, except for the RF and LO input signals. Using the following notation for the LO, in-phase (I) and quadrature (Q) signals:

$$LO(t) = \cos(\omega_c t) \tag{1a}$$

$$I_{\rm in}(t) = \cos(\omega_{bb} t) \tag{1b}$$

$$Q_{\rm in}(t) = \cos(\omega_{bb} t + 90^\circ) \tag{1c}$$

the mixed signals $I_{\rm out}$ and $Q_{\rm out}$ are

$$I_{\rm out}(t) = \frac{1}{2}[\cos(2\omega_c + \omega_{bb})t + \cos(2\omega_c - \omega_{bb})t] \tag{2a}$$

$$Q_{\rm out}(t) = \frac{1}{2}\left\{\cos[(2\omega_c + \omega_{bb})t + 90^\circ] + \cos[(2\omega_c - \omega_{bb})t - 90^\circ]\right\} \tag{2b}$$

after the mixed signals $I_{\rm out}$ and $Q_{\rm out}$ pass through the broadside coupler, the modulated signal is given by

$$\mathrm{RF}(t) = \cos(2\omega_c - \omega_{bb})t. \tag{3}$$

However, due to the amplitude and phase imbalance of practical circuit implementation, complete suppression does not occur [6].

The block diagram of the modulator shown in Fig. 1 can also be operated as a demodulator with the replacement of downconversion mixers. Modulated signals entering the 90° phase shifter from the RF port are separated into two equal amplitude components with 90° phase shift and mix with the sub-harmonic LO by the sub-harmonic mixer to produce baseband signals.

III. Circuit Design

The mixer is a critical component in the demodulator and modulator designs that translates the RF signals to and from baseband signals. Circuit design of the broadband sub-harmonic direct up/downconversion mixer is described here. The quality factors of the matching networks [18] are designed to have a low value for broadband impedance matching. Although a higher quality factor of the matching networks has better conversion loss, the circuits become more narrowband and sensitive to process variations. The sub-harmonic modulator and demodulator are fabricated in a 0.13-μm 1P8M bulk CMOS process. This process provides a single poly layer for the gates of the MOS and eight metal layers for inter-connection. Using optimized CMOS topology and deep n-well (DNW), this topology provides an f_t of 85 GHz and $f_{\max}$ of 90 GHz at maximum-transconductance bias. The transmission lines were implemented using thin-film microstrip (TFMS) lines [5]. The TFMS consists of metal 1 (bottom layer) in the 1P8M CMOS process as the ground plane and metal 8 (top layer) as the microstrip signal line with the thick SiO_2 layer as the substrate. The TFMS can be meandered in a very compact area to reduce the circuit size without suffering the coupling effect. In this 0.13-μm CMOS process, the TFMS linewidth of 50-Ω characteristic impedance is approximately 10 μm. The circuits were simulated with Agilent's Advanced Design System (ADS).

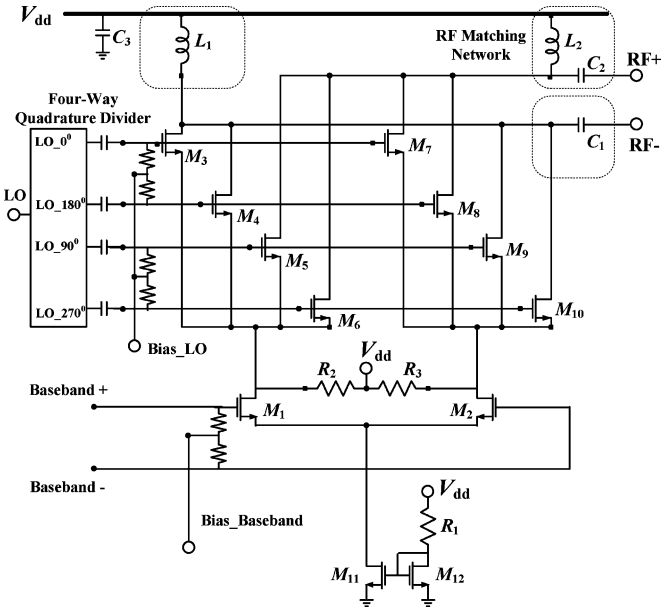

Fig. 2. Schematic of the 35–65-GHz CMOS sub-harmonic direct upconversion Gilbert-cell mixer.

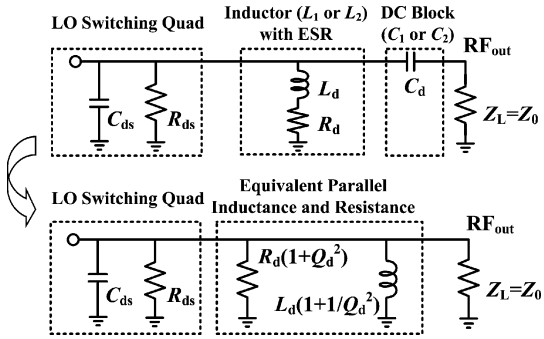

Fig. 3. Equivalent circuit of output matching network of the sub-harmonic direct upconversion Gilbert-cell mixer.

The passive components include the discontinuities of the TFMS lines, inductors, and capacitors and were simulated by a full-wave electromagnetic (EM) simulator (Sonnet software) [19].

A. Broadband Sub-Harmonic Direct Upconversion Mixer

The sub-harmonically pumped mixing in a direct upconversion mixer is selected in this design. Since the LO leakage of the sub-harmonic mixer does not appear in the RF band and the $2 * \text{LO}$ leakage of the sub-harmonic mixer is much smaller than the LO leakage of the fundamental mixer, the signal distortion due to large LO leakage to the RF port can be significantly reduced [13]–[15]. The schematic of the broadband sub-harmonic direct upconversion Gilbert-cell mixer is showed in Fig. 2. The mixer consists of the several passive and active components. The Gilbert-cell configuration is selected for its double-balanced implementation, which offers high spur suppression in a very compact die size. The main transconductor, which converts the baseband input signal to output current, is composed of nMOS M_1 and M_2 (144 μm/0.13 μm, which is a 72-finger device with 2 μm unit finger length). The sub-harmonic LO switching quad consists of four parallel connected nMOS pairs, shown as M_3–M_{10} (36 μm/0.13 μm). Each transistors of the LO switching quad turn on and off alternatively during one period of the applied LO signal, thus, the RF signal can be switched on every quarter cycle of the LO signal, which creates an effective $2 * \text{LO}$ signal. In order to minimize the noise of the active mixer, the bias current of the LO switching quad should be small enough to lower the magnitude of noise pulses. Therefore, a current bleeding circuit, which is composed of R_2 (400 Ω) and R_3 (400 Ω) is incorporated to bleed the drain current flowing into main transconductors and reduce the bias current of the LO switching quad [20]. The bias current of the transconductor stage is determined by a current mirror source, which is composed of M_{11} (72 μm/0.13 μm), M_{12} (12 μm/0.13 μm), and R_1 (2000 Ω). A single mixer draws total 11.5-mA dc current from a 3.3-V supply voltage. There is 4-mA dc current bled through R_2 and R_3, respectively, from a 3.3-V supply voltage.

To achieve broadband frequency response at the RF output port, the quality factor of the output impedance matching network is kept low to cover the 35–65-GHz band. The output matching networks consist of a shunt inductor L_d (L_1 or L_2) and a series dc blocking capacitor C_d (C_1 or C_2). One terminal of the inductor L_d is connected to V_{dd} with a bypass capacitor C_3. For low quality factor output impedance matching analysis, each output side equivalent circuit of the double-balanced sub-harmonic mixer is shown in Fig. 3. $R_{\rm ds}$ and $C_{\rm ds}$ are resistance and capacitance looking into a drain of LO switching quad transistors. The dc-blocking capacitor C_d (2 pF) is ac short. The load impedance Z_L is 50 Ω. The inductor L_d at each output side along with its equivalent series resistance (ESR) R_d are transformed to a parallel combination of $L_d\,(1 + 1/Q_d^2)$ and $R_d(1 + Q_d^2)$ [18] for parallel *RLC* resonant circuit analysis, where the quality factor of the drain inductor Q_d is given by

$$Q_d = \frac{\omega_{\rm RF} L_d}{R_d}. \tag{4}$$

The quality factor $Q_{\rm rfout}$ of the parallel *RLC* resonant circuit shown in Fig. 3 at the resonant frequency ($\omega_{\rm RF}$) is given by

$$Q_{\rm rfout} = \frac{R_d(1+Q_d^2)||R_{\rm ds}||Z_L}{\omega_{\rm RF} L_d \left(1 + \dfrac{1}{Q_d^2}\right)}. \tag{5}$$

To match the impedance at the output port, $R_d(1 + Q_d^2)||R_{\rm ds}$ should be equal to Z_L of 50 Ω. From the definition of the quality factor $Q = \omega_0/\text{BW}$ [18], the quality factor of output matching network $Q_{\rm rfout}$ was determined to be 1.5 in this study to cover the 35–65-GHz bandwidth. The inductor L_d needs to be 0.055 nH along with its ESR R_d of 1.3 Ω. Finally, the simulation helps in choosing the device size of the LO switching quad transistors.

B. Broadband Sub-Harmonic Direct Downconversion Mixer

Most direct conversion receivers suffer degradation of signal-to-noise ratio (SNR) performance due to the problems of LO self-mixing. To mitigates the LO self-mixing problem, the sub-harmonically pumped mixing scheme is selected to separate the fundamental LO and RF frequency band. The schematic

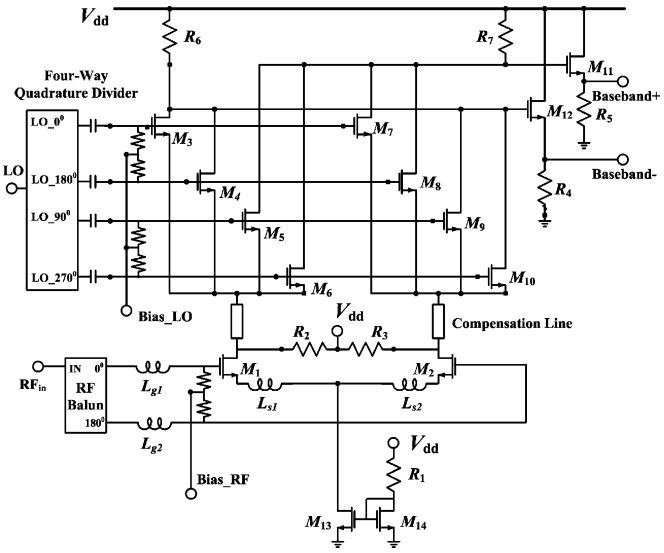

Fig. 4. Schematic of the 35–65-GHz CMOS sub-harmonic direct downconversion Gilbert-cell mixer.

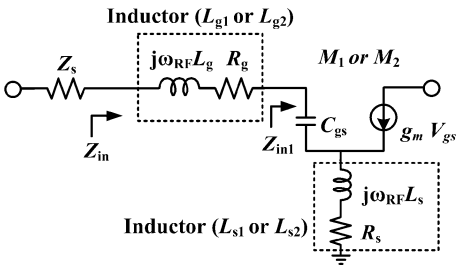

Fig. 5. Equivalent circuit of input matching network of the sub-harmonic direct downconversion Gilbert-cell mixer.

of the sub-harmonic double-balanced direct downconversion Gilbert-cell mixer is shown in Fig. 4. The main transconductor, which converts RF input signal to output current, is composed of nMOS M_1 and M_2 (32 μm/0.13 μm). The bias current of the transconductor stage is determined by a current mirror source, which is composed of M_{13} (72 μm/0.13 μm), M_{14} (12 μm/0.13 μm), and R_1 (2400 Ω). The sub-harmonic LO switching quad consists of four parallel connected nMOS pairs, shown as M_3–M_{10} (12 μm/0.13 μm). A current bleeding circuit, which is composed of R_2 (400 Ω) and R_3 (400 Ω), are incorporated to bleed the drain current flowing into main transconductors. With this current bleeding circuit, the drain current of the input transistors M_1 and M_2 can be partially supplied through it, which reduces the drain current of the switching quad transistors and the voltage drop of load resistors (R_6 and R_7). Therefore, the value of these load resistors, R_6 and R_7 (1000 Ω), can be increased, thus the voltage conversion gain is raised. A source–follower buffer for baseband active matching is used. By selecting the transistor size of M_{11} (72 μm/0.13 μm) and M_{12} (72 μm/0.13 μm), the baseband modulation bandwidth of the downconversion mixer can be widened up to 1 GHz for gigabit applications.

For broadband RF input impedance matching, the quality factor of the input matching network is also kept low to cover the 35–65-GHz band. As shown in Figs. 4 and 5, gate inductors L_g (L_{g1} or L_{g1}) and source inductors L_s (L_{s1} or L_{s1}) are used to transfer the input impedance to Z_s of 50 Ω. The ESR of the

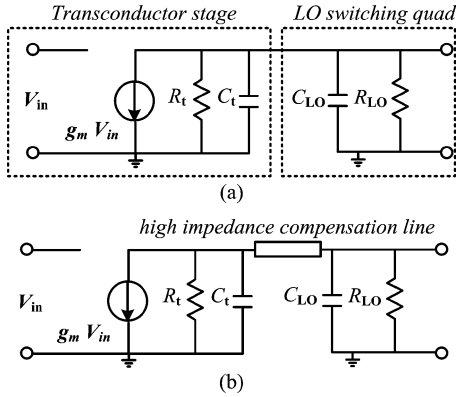

Fig. 6. (a) Small-signal model of the transconductor stage with the loading effect of the LO switching quad. (b) High-impedance compensation line is incorporated as inductances between transconductance stage and switching quad.

inductors L_g and L_s are R_g and R_s, respectively. The effect of parasitic shunt capacitances C_p of the inductors are too small to be reflected in calculation of input impedance. An expression of the impedance $Z_{\rm in}$ looking into the gate of transistor pairs M_1 or M_2 through the inductor L_g can be written as follow [21]:

$$Z_{\rm in} = R_g + j\omega_{\rm RF}L_g + R_s + j\omega_{\rm RF}L_s + \frac{1+g_mR_s}{j\omega_{\rm RF}C_{\rm gs}} + \frac{g_mL_s}{C_{\rm gs}} \quad (6)$$

where $C_{\rm gs}$ is the parasitic capacitor of the transistor M_1 or M_2. The quality factor ($Q_{\rm rfin}$) of the series *RLC* resonant circuit shown in Fig. 5 at the resonant frequency ($\omega_{\rm RF}$) including the source impedance Z_s is given by [18]

$$Q_{\rm rfin} = \frac{\omega_{\rm RF}(L_g+L_s)}{2Z_s} = \frac{1+g_mR_S}{2\omega_{\rm RF}Z_sC_{\rm gs}}. \quad (7)$$

The quality factor of output matching network $Q_{\rm rfout}$ was also determined to be 1.5 to cover 35–65 GHz. Once $Q_{\rm rfin}$ is set, the size of transistor M_1 and M_2 (32 μm/0.13 μm) are determined by (7). Finally, the simulation helps in choosing the values of the components. The selected size of transistor M_1 and M_2 is a 16-finger device with a 2-μm unit finger length. Both M_1 and M_2 are minimum length devices (0.13 μm). $C_{\rm gs}$ of the transistor M_1 or M_2 is 0.031 pF in this study. L_g is 0.42 nH with R_g of 8 Ω and $L_s = 0.05$ nH with R_s of 1.2 Ω.

The parasitic capacitance of CMOS technology results in degradation of the performance at a high operation frequency. To compensate the parasitic capacitance and improve the conversion loss at high frequency, a compensation line as inductance is incorporated between transconductance stage and switching quad. Fig. 6(a) shows the small-signal model of the transconductor stage with the loading effect of the following LO switching quad stage. R_t and C_t are the parasitic resistance and capacitance, respectively, of the transconductor stage transistor, while $R_{\rm LO}$ and $C_{\rm LO}$ are the parasitics of the LO switching quad. The gain-bandwidth product (GBW) of this transconductor stage is given by

$$\text{GBW} = \frac{g_m}{2\pi \cdot C} \quad (8)$$

where $C = C_t + C_{\rm LO}$. As can be observed, large parasitic capacitances limit the GBW of the Gilbert-cell mixer. The switching

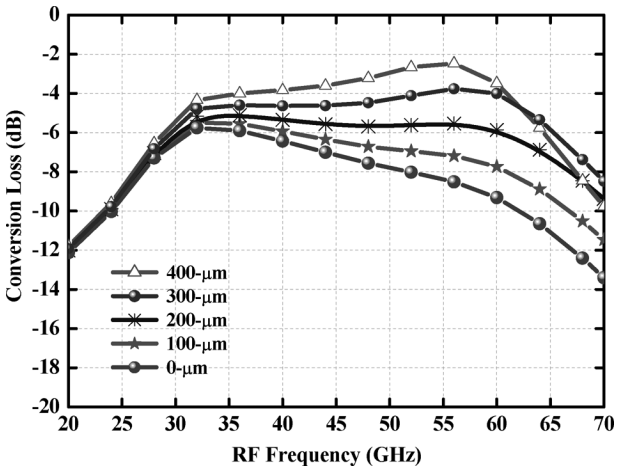

Fig. 7. Simulated conversion loss versus RF frequency of the sub-harmonic downconversion Gilbert-cell mixer for different compensation-line lengths.

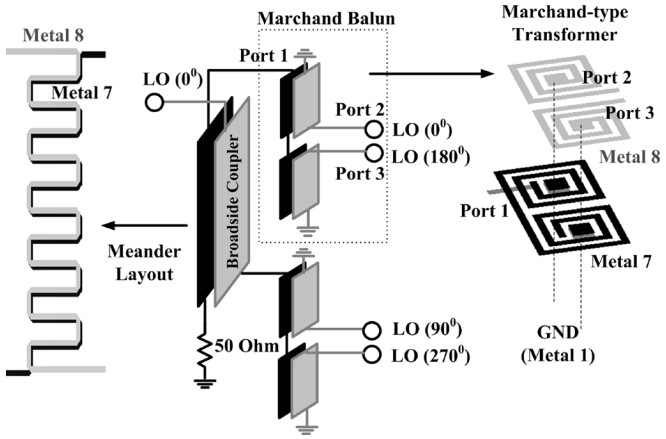

Fig. 8. Proposed MMW LO four-way quadrature divider.

quad of the sub-harmonic Gilbert-cell mixer especially consists of four parallel connected nMOS pairs, which introduce a larger parasitic capacitance than a fundamental Gilbert-cell mixer. To overcome the problem, a high-impedance compensation line, as shown in Figs. 4 and 6(b), is incorporated as an inductance between the transconductance stage and switching quad to compensate C_t and $C_{\rm LO}$. The parasitic capacitance of the transistor is combined with the inductance of the compensation line to form a third-order Butterworth *LC* ladder network in Fig. 6(b) [22]. The network absorbs the parasitic capacitance at resonant frequency. Therefore, the use of a series inductor between the transconductor and the switching transistors can extend the bandwidth above the limit in (8). In general, it is complicated to calculate the values of the high-impedance compensation line for optimizing the *LC* ladder network directly. Instead, the simulation helps in optimizing choosing the values of the compensation-line lengths. The simulated conversion loss of the complete mixer is shown in Fig. 7 with various compensation-line lengths from 0 to 400 μm and width of 2.5 μm. A significant improvement can be achieved for the flatness of conversion loss over frequencies by a proper selection of compensation-line length. Without the compensation line, the conversion loss will slope down from 6 to 11 dB when the RF and LO frequency sweeps from 35 to 65 GHz. For a flat conversion loss over frequency, the compensation-line length of 300 μm is selected, the conversion loss will slope down from 5 to 6 dB when the RF frequency sweeps from 35 to 65 GHz.

C. MMW Quadrature-Phases LO Generation Scheme in the CMOS Process

The phase-shifting network plays an important role in the generation of equal amplitude and quadrature-phases LO signals for the sub-harmonically pumped Gilbert-cell mixer. However, it is difficult to generate the accurate quadrature-phases LO by using an external balanced phase shifter or surface mount balun, particularly in the MMW frequency. Furthermore, using a conventional embedded *RC* poly-phase filter at the LO signal path attenuates the LO power significantly in the MMW frequency. An additional differential LO buffer amplifiers should be added between the poly-phase filter and mixer in order to compensate the losses [23].

For the MMW sub-harmonic Gilbert-cell mixer, an embedded LO four-way quadrature divider using a 90° coupler and 180° baluns in the CMOS technology is proposed. The structure and layout of the LO four-way quadrature divider is shown in Fig. 8. A Marchand-type transformer is used as 180° baluns due to its excellent amplitude/phase match and broadband response [10], [24]. Two coupled lines in the Marchand balun are constructed of broadside coupled lines using metal layers 7 and 8 in this 0.13-μm CMOS process. These two coupled lines are wound into two coils, shown in Fig. 8, with a width and gap both of 3 μm. Port 1 of the 180° balun was connected through two coils to open circuit, and ports 2 and port 3 were connected from ground to coil. At the operation frequency, the signal of port 1 will couple to the top side coils, and port 2 and port 3 will be 180° out-of-phase.

For the 90° coupler of the four-way quadrature divider, a broadside coupler with a tight coupling factor of 3 dB is also implemented using the TFMS structure [10]. It is constructed with two strip lines using different metal layers, i.e., metal layer 7 and 8. Since the gap between the edge coupler is too small to be fabricated for the required coupling, metal layer 8 and 7 are used for the coupled lines of the broadside coupler due to the thick dielectric layer. To obtain the appropriate coupling, an additional offset distance of 2 μm between metal 7 and 8 is added. The linewidth of the coupled line is 4 μm. Its size can be reduced by using meander-like layout. The 90° coupler and 180° baluns are both calculated using the full-wave EM simulator (Sonnet software) [19].

IV. Experimental Results

The microphotographs of the modulator and demodulator are shown in Figs. 9 and 10. Overall die size of the modulator and demodulator are 0.98 mm × 0.8 mm and 1 mm × 1 mm, respectively. The MMIC are tested via on-wafer probing. The measurement results are shown here.

A. Modulator Characteristics

The key performances of the modulator are suppression, conversion loss, and intermodulation. Fig. 11 shows the measured

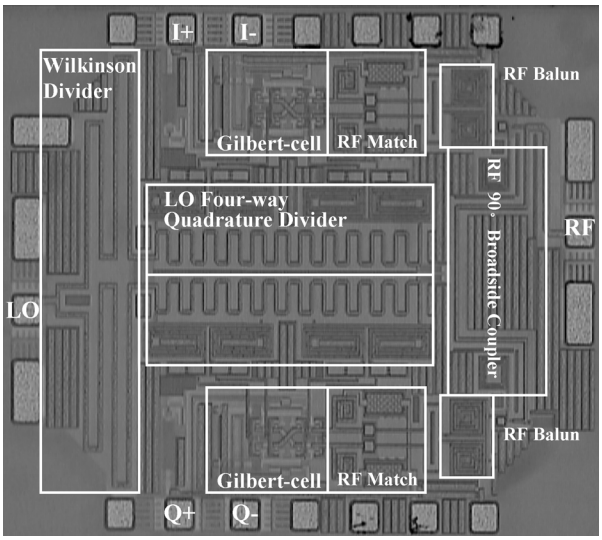

Fig. 9. Chip photograph of the CMOS sub-harmonic modulator with chip size of 0.98 mm × 0.8 mm.

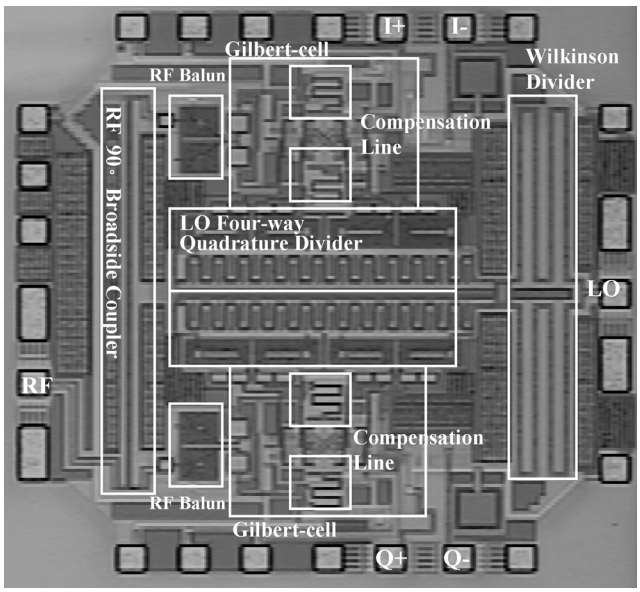

Fig. 10. Chip photograph of the CMOS sub-harmonic demodulator with chip size of 1.0 mm × 1.0 mm.

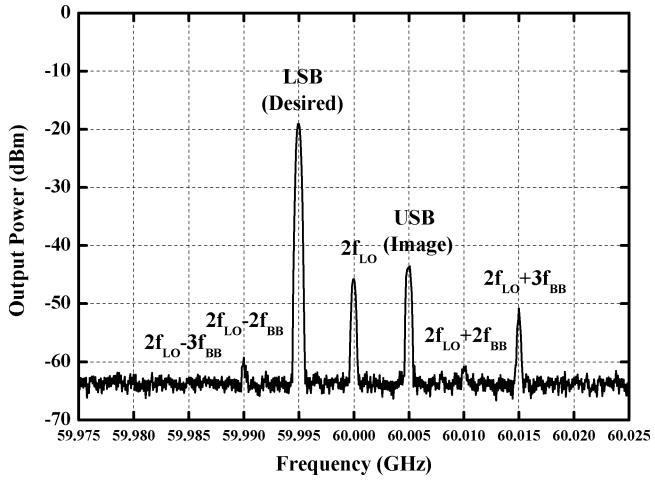

Fig. 11. Measured output spectrum of the sub-harmonic IQ modulator with an 2 ∗ LO frequency of 60 GHz and a baseband frequency of 5 MHz.

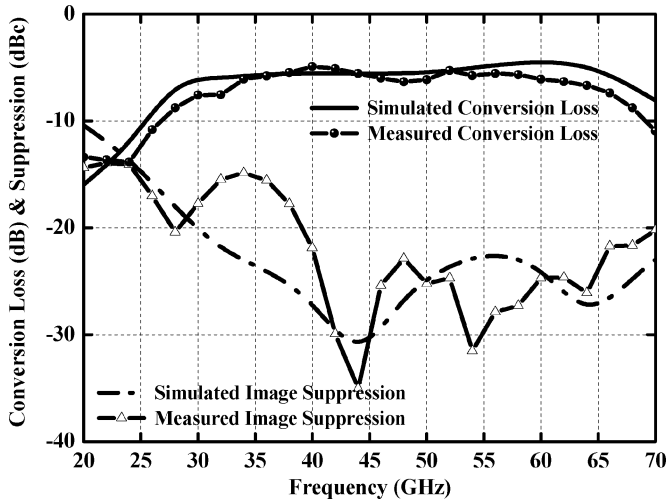

Fig. 12. Simulated and measured conversion loss and USB suppression versus the RF frequency from 20 to 70 GHz for the sub-harmonic IQ modulator.

output spectrum of the CMOS sub-harmonic IQ modulator with an RF frequency of 60 GHz, an LO frequency of 30 GHz, and a baseband frequency of 5 MHz, where the lower sideband (LSB) is the desired signal and the upper sideband (USB) is the image signal. The measured output power of the modulator signal is −19 dBm with the optimal LO drive power of 7 dBm and baseband input of −14 dBm. The measured USB suppression is −24 dBc, which indicates an amplitude error is within 0.6 dB and a phase error is within 6° [6], [10]. The measured 2 ∗ LO suppression is −27 dBc, referring to the desired output power. The LO driver power is 7 dBm at 30 GHz and the 2 ∗ LO leakage power is −45.7 dBm, as shown in Fig. 11. Therefore, the 2 ∗ LO to RF port isolation (LO leakage) is 52.7 dB. The third-order intermodulation ($2f_{\rm LO} \pm 3f_{BB}$) components are less than −31 dBc and the second-order intermodulation ($2f_{\rm LO} \pm 2f_{BB}$) components are less than −40 dBc referring to the desired output power.

The simulated and measured conversion loss and USB suppression of the IQ modulator from 20 to 70 GHz is plotted in Fig. 12. The measured conversion-loss results agree well with the simulated results, which demonstrate the conversion loss of 6 ± 1.5 dB from 35 to 65 GHz. The measured USB suppression is better than −20 dBc from 39 to 70 GHz. In addition, the USB suppression has the best performance, i.e., −30 dBc, from 42 to 45 GHz due to the low-imbalance (amplitude imbalance < 0.5 dB and phase imbalance < 3°) characteristics of the RF 90° broadside coupler. The simulated and measured 2 ∗ LO suppression of the modulator from 20 to 70 GHz is plotted in Fig. 13. The measured 2 ∗ LO suppression is better than −24 dBc from 30 to 65 GHz. The measured intermodulation ($2f_{\rm LO} \pm 2f_{BB}$ and $2f_{\rm LO} \pm 3f_{BB}$) of the modulator from 20 to 70 GHz is also plotted in Fig. 13. As can be observed, the third- and second-order intermodulation are better than −28 dBc and −40 dBc, respectively, from 35 to 65 GHz. The measured output $P_{\rm 1dB}$ is −19 dBm and the

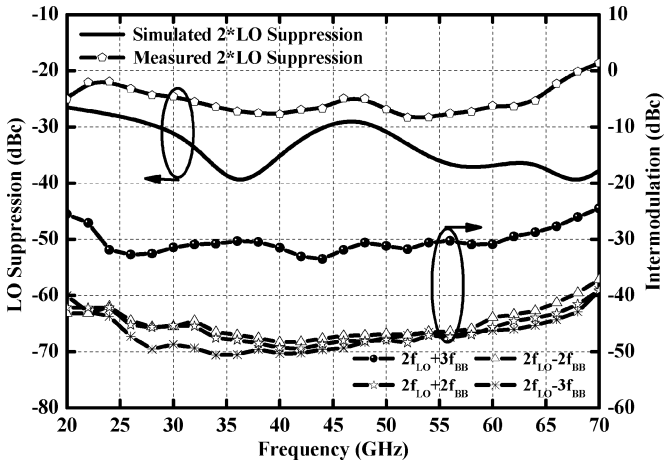

Fig. 13. Simulated and measured $2 * \mathrm{LO}$ suppression and measured intermodulation versus the RF frequency from 20 to 70 GHz for the sub-harmonic IQ modulator.

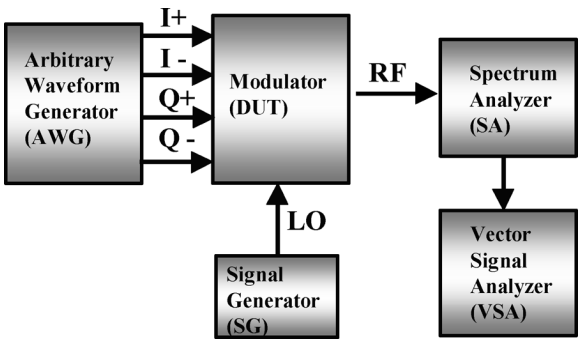

Fig. 14. Block diagram of the MMW vector signal measurement system for the MMW sub-harmonic modulator.

total dc power consumption of the sub-harmonic modulator is 75.9 mW.

To verify the high data rates digital modulation quality of the sub-harmonic IQ modulator, the MMW vector signal measurement system has been set up. The block diagram of the vector signal measurement system is plotted in Fig. 14. The baseband IQ sources are generated using Agilent's ADS software and downloaded into an arbitrary waveform generator (Agilent E4438C). The baseband IQ signals are fed into our modulator MMIC. The LO source of the modulator is provided by the signal generator (Agilent E8247C). The output spectrum can be observed by using a spectrum analyzer (Agilent E4448A). The spectrum analyzer is also used for high-quality downconversion of the output signal to an IF (70 MHz). This 70-MHz IF signal is fed into a vector signal analyzer (Agilent VSA 89601A) for the analysis of the digital modulation quality. The baseband overall input power, including I+, I−, Q+, and Q−, is −14 dBm. At a $2 * \mathrm{LO}$ frequency of 60 GHz, the sub-harmonic IQ modulator is evaluated by a quadrature phase-shift keying (QPSK) modulation with a data rate of 20 Ms/s. The measured output spectrum of the IQ modulator is plotted in Fig. 15, which demonstrated a channel power of higher than −20 dBm with a channel bandwidth of 20 MHz and an adjacent channel power ratio (ACPR) of better than −25 dBc. The measured constellation diagram of the IQ modulator at 60 GHz is plotted in Fig. 16. The points

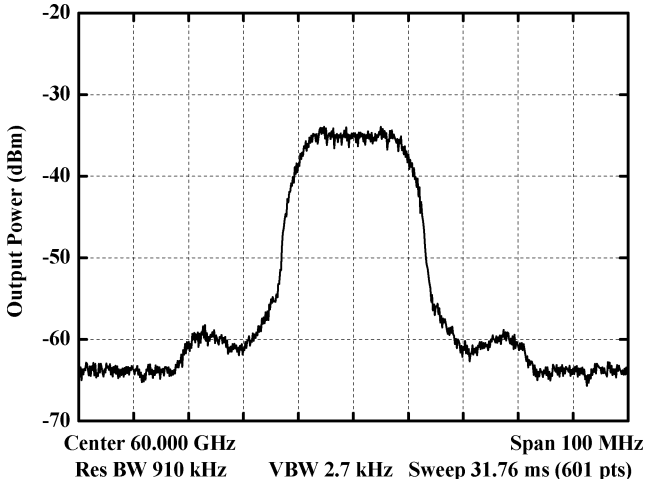

Fig. 15. Measured output spectrum of the sub-harmonic IQ modulator at 60 GHz with a 20-Ms/s QPSK modulation; the channel power is approximately −20 dBm with a channel bandwidth of 20 MHz.

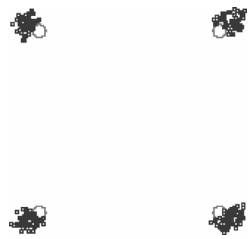

Fig. 16. Measured constellation diagram of the sub-harmonic IQ modulator at 60 GHz with a 20-Ms/s QPSK modulation.

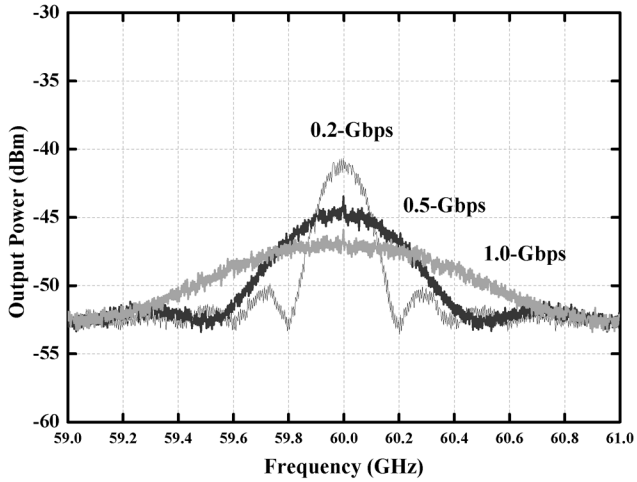

Fig. 17. Measured BPSK output spectrum of the sub-harmonic modulator at 60 GHz with 0.2-, 0.5, and 1.0-Gb/s data rates in PRBS.

in the QPSK constellation can be spread out uniformly into a "square." The measured error vector magnitude (EVM) of the QPSK modulation is within 6%. For wideband applications, the pseudorandom bit stream (PRBS) with 0.2-, 0.5-, and 1.0-Gb/s data rates is fed in to the sub-harmonic modulator. The differential baseband signals are generated from a pattern generator (Anritsu MP1763C), and the voltage swing of the baseband signal is 0.5 V. The measured binary phase-shift keying (BPSK) output spectrum at 60 GHz is plotted in Fig. 17 with good LO suppression. The spectrum is spread out due to the unfiltered baseband signals, resulting in a sinc-like spectrum.

TABLE I
COMPARISON OF MODULATOR IN VARIOUS TECHNOLOGIES AND TOPOLOGIES

	Ref. [8]	Ref. [9]	Ref. [10]	Ref. [11]	This work
Process	GaAs pHEMT	GaAs HBT	CMOS	Multilayer Thin-film Multichip Module	CMOS
Topology	Fundamental Reflection-Type	Fundamental Reflection-Type	Fundamental Reflection-Type	Sub-harmonic Antiparallel Diode Pair	Sub-harmonic Double-balanced Gilbert-cell
RF Frequency	66.5-86.5 GHz	50-110 GHz	20-40 GHz	13-15 GHz	35-65 GHz
LO Frequency	66.5-86.5 GHz	50-110 GHz	20-40 GHz	6.5-7.5 GHz	20-32.5 GHz
Modulation Bandwidth	> 6 Mbps	> 10 Mbps	> 1 Gbps	N/A	> 1 Gbps
Conversion Loss	< 12 dB	< 20 dB	< 13 dB	< 14 dB	6 ± 1.5 dB
LO to RF Port Isolation	> 10 dB (LO to RF port)	> 20 dB (LO to RF port)	> 40 dB (LO to RF port)	> 43 dB (2*LO to RF port)	> 50 dB (2*LO to RF port)
Sideband Suppression	< -24 dBc @ 75 GHz	< -20 dBc @ 55-95 GHz	< -20 dBc < -40 dBc@27-30GHz	-34 dBc@14.2GHz	< -20 dBc@39-65 GHz < -30 dBc@42-45 GHz
Intermodulation	N/A	< -20 dBc	< -30 dBc	<-30 dBc	<-30 dBc
ACPR / Output Power	N/A	-24.5 dBc / -22.5dBm @94GHz	-40 dBc / -18dBm @30GHz	N/A	-25 dBc / -20dBm @60GHz
Power Consumption	0	0	0	0	75.9mW
Chip Size	2 × 1.6 mm^2	2 × 2 mm^2	0.65 × 0.58 mm^2	7.6 × 16.9 mm^2	0.98 × 0.8 mm^2

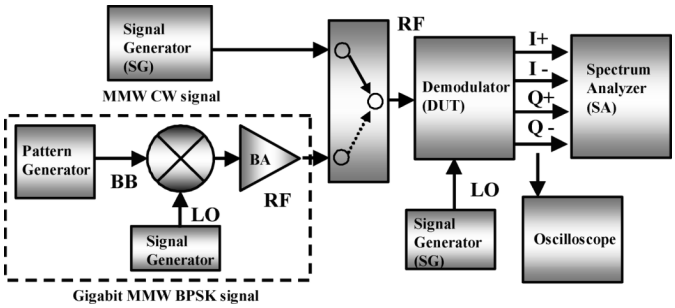

Fig. 18. Block diagram of the MMW measurement system for the MMW sub-harmonic demodulator.

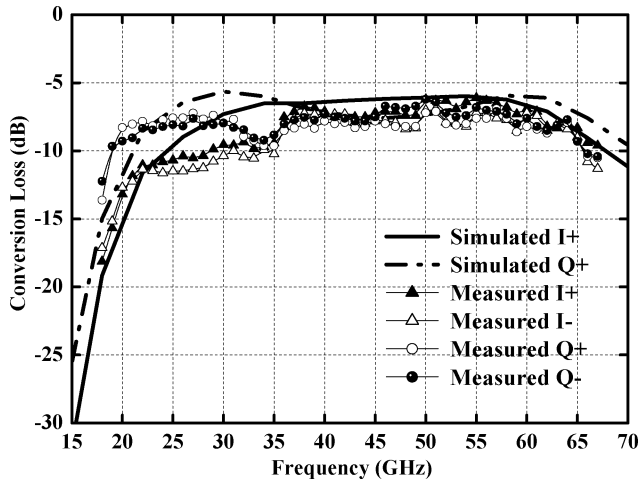

Fig. 19. Simulated and measured conversion loss versus the RF frequency from 15 to 70 GHz for the sub-harmonic demodulator.

Table I is the comparison of the previously reported modulator in various technologies and topologies. Our CMOS modulator formed by the sub-harmonic double-balanced Gilbert-cell mixer demonstrates smallest conversion loss and best 2∗LO to RF port isolation with a compact chip size.

B. Demodulator Characteristics

The common set of specifications for the direct downconversion demodulator are the conversion loss, intermodulation distortion, 2 ∗ LO leakage to the input port, and rejection of the LO at the input port. Fig. 18 shows the block diagram of the measurement system for the MMW sub-harmonic demodulator in this study. The MMW continuous wave (CW) signals, provided by signal generator (Agilent E8267C), are fed into our demodulator MMIC. The LO source of the demodulator is provided by another signal generator (Agilent E8247C). The output spectrum can be measured by using a spectrum analyzer (Agilent E4448A). An oscilloscope is used to observe the I+, I−, Q+, and Q− time-domain waveforms. At an RF of 60 GHz and baseband of 10 MHz, the conversion loss is measured as a function of LO power. The optimal LO drive is +8 dBm. Fig. 19 plots the simulated and measured conversion loss versus RF frequency corresponding to I+, I−, Q+, and Q− ports from 15 to 70 GHz. As can be observed, the simulation and measurement results have a good agreement. The measured conversion loss is 7.5 dB (to 50-Ω load) with the gain flatness of ±1.5 dB and the amplitude imbalance is within 1.5 dB from 35 to 65 GHz. The downconverted I+, I−, Q+, and Q− time-domain waveforms are shown in Fig. 20, where the RF unmodulated carrier signal is 60 GHz and the downconverted baseband signal is 10 MHz. Measured isolation between RF to LO port, LO to RF port, and 2 ∗ LO to RF port are shown in Fig. 21. The LO to RF port and 2 ∗ LO to RF port isolation are better than 45 and 50 dB, respectively, from 35 to 65 GHz. The measured input 1-dB compression point of the mixer is 0 and −5 dBm at an RF of 40 and 60 GHz, respectively. To investigate the intermodulation properties of the mixer, two-tone intermodulation measurements with the frequency offset of ±500 kHz are shown in Fig. 22. The typical input third-order intermodulation product (IIP3) is 9 dBm for an RF two-tone of 44.0005 GHz and 43.9995 GHz with an LO input of 21.995 GHz. The typical input second-order intermodulation product (IIP2) is 34 dBm. Fig. 23 is the measured conversion loss versus the baseband frequency from 1 MHz to 3 GHz with an LO frequency of 30 GHz

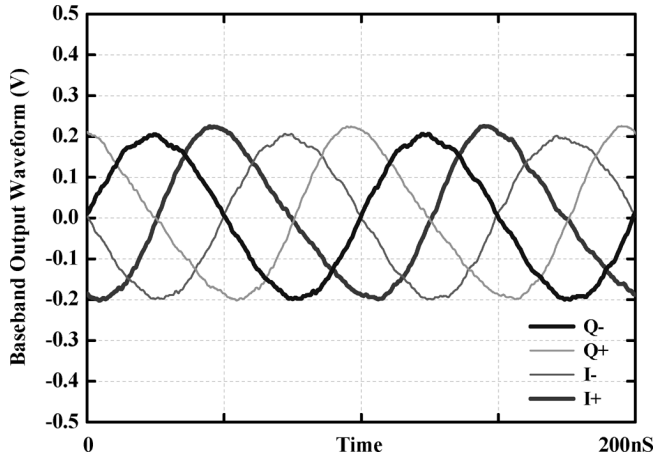

Fig. 20. Measured baseband time-domain quadrature signals at 10 MHz for the sub-harmonic demodulator.

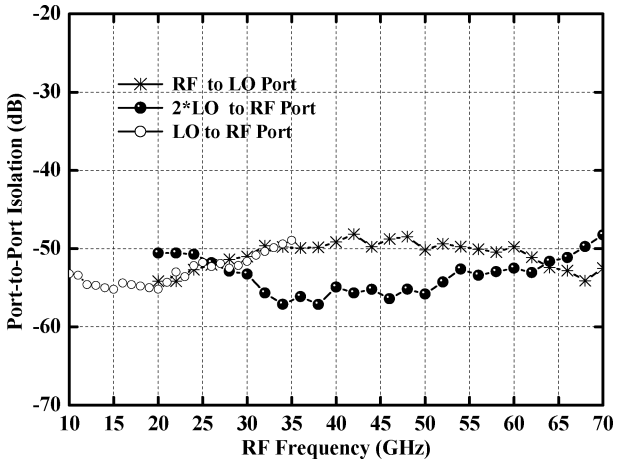

Fig. 21. Measured isolation between RF to LO port, LO to RF port, and $2*$LO to RF port.

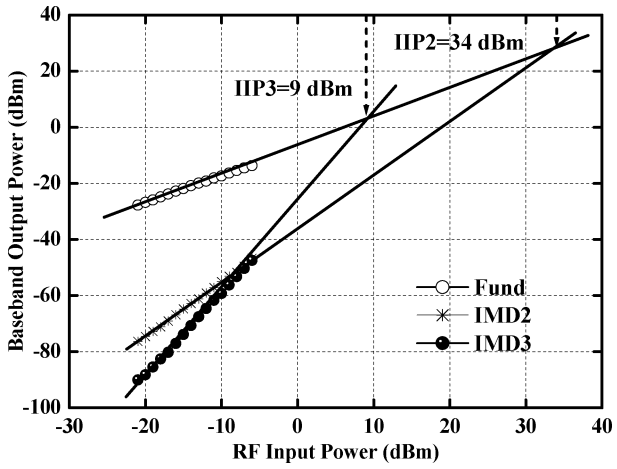

Fig. 22. Measured IIP3 and IIP2 for the sub-harmonic demodulator (IF $=$ RF $-$ 2 $*$ LO, RF $=$ 44 GHz $\pm$ 500 kHz, LO $=$ 21.995 GHz).

for the demodulator. The demodulator features a demodulation bandwidth above 1 GHz. The measured double-sideband noise figure of the demodulator is 14.5 dB at an IF of 100 MHz and

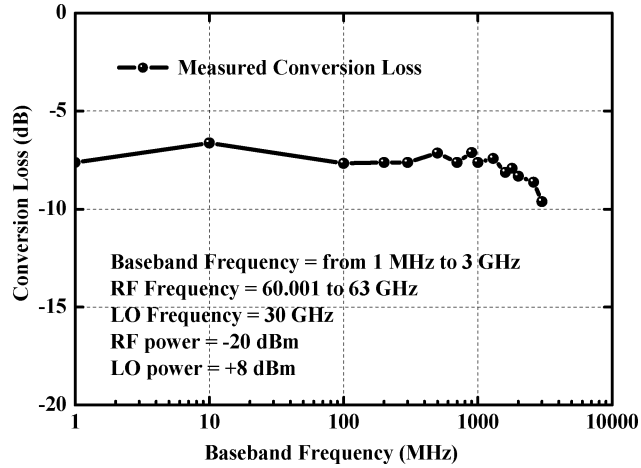

Fig. 23. Measured conversion loss versus the baseband frequency of the sub-harmonic demodulator.

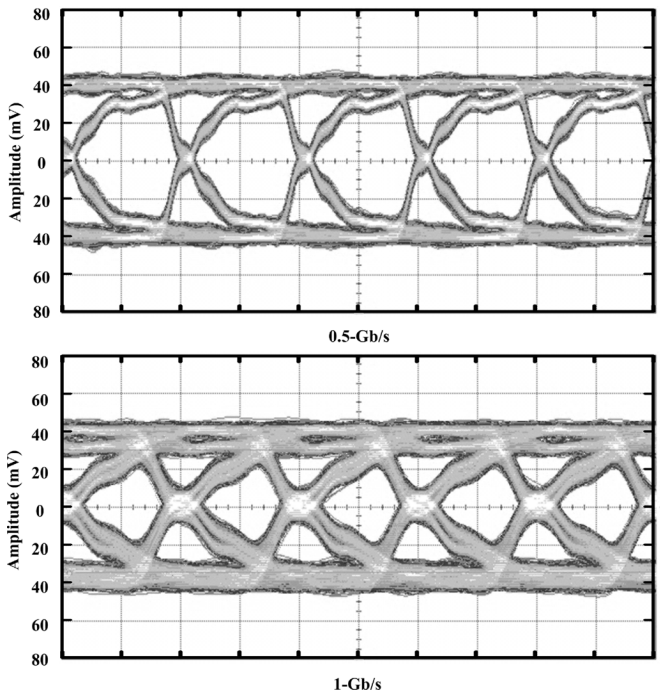

Fig. 24. Measured eye diagram of the 0.5-Gb/s and 1-Gb/s PRBS for the sub-harmonic demodulator.

RF of 40 GHz. The total dc power consumption of the sub-harmonic demodulator is 90.8 mW.

To verify the high data rates' digital demodulation quality, the sub-harmonic demodulator is evaluated with 1-Gb/s data rates in a PRBS. The block diagram of the gigabit measurement system for an MMW sub-harmonic demodulator is also plotted in Fig. 18. The baseband signals are generated from a pattern generator (Anritsu MP1763C) with a data rate of 1-Gb/s. The baseband signals are upconvert to the MMW frequency band (in this study, 44 GHz), by a custom design MMW upconverter. The 44-GHz gigabit modulation signal is fed into the sub-harmonic demodulator for a demodulation quality test. The measured eye diagram of the 0.5-Gb/s and 1-Gb/s PRBS demodulation signal are plotted in Fig. 24, while the 50-Ω input of the oscilloscope

is used as the load. To be observed, the clear eye opening is achieved for the satisfactory recovery of the baseband signal.

V. Conclusion

The first demonstration of the broadband sub-harmonic CMOS modulator and demodulator using 0.13-μm standard MS/RF CMOS technology for MMW wireless gigabit applications has been presented in this paper. The key component, i.e., the four-way quadrature divider of the sub-harmonically pumped mixer, has been embedded to generate the quadrature-phases LO signals in the MMW frequency. For broadband applications, a broadband matching design formula is provided in this paper to extend the operational frequency range from 35 to 65 GHz. To improve the conversion loss at high frequency, high-impedance compensation is incorporated between the transconductance stage and LO switching quad of the mixer to compensate the parasitic capacitance. A significant improvement can be achieved for the flatness of conversion loss over frequencies after adding the compensation line. The modulator exhibits 6 ± 1.5 dB measured conversion loss from 35 to 65 GHz with good sideband and $2 * \mathrm{LO}$ suppression. The demodulator exhibits 7.5 ± 1.5 dB measured conversion loss with amplitude imbalance within 1.5 dB from 35 to 65 GHz. Furthermore, for wireless gigabit applications, a digital modulation signal test is performed for the sub-harmonic modulator and demodulator. The experimental results show that the modulator and demodulator feature broadband and gigabit direct-conversion capabilities.

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Jeng-Han Tsai (S'04) was born in Tainan, Taiwan, R.O.C., on December 20, 1980. He received the B.S. degree in electric engineering from National Central University, Chung-Li, Taiwan, R.O.C., in 2002, and Ph.D. degree from the Graduate Institute of Communication Engineering, National Taiwan University, Taipei, Taiwan, R.O.C., in 2007.

He is currently a Post-Doctoral Research Fellow with the Graduate Institute of Communication Engineering, National Taiwan University. His research interests include microwave and MMW circuit designs.

Tian-Wei Huang (S'91–M'98–SM'02) received the B.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, R.O.C., in 1987, and the M.S. and Ph.D. degree in electrical engineering from the University of California at Los Angeles (UCLA), in 1990 and 1993, respectively.

In 1993, he joined the TRW RF Product Center, Redondo Beach, CA. From 1998 to 1999, he was with Lucent Technologies, where he was involved with the local multipoint distribution system (LMDS) fixed wireless systems. From 1999 to 2002, he was involved with RF/wireless system testing with Cisco Systems. In August 2002, he joined the faculty of the Department of Electrical Engineering, National Taiwan University. His current research interests are MMIC/RFIC design, packaging, and RF system-on-chip (SOC) integration. His research has focused on the design and testing of monolithic microwave integrated circuits (MMICs) and RF integrated circuits (RFICs).