A 245 GHz CB LNA in SiGe

Yanfei Mao, K. Schmalz, J.Borngräber, J.C. Scheytt

IHP, Im Technologiepark 25
Frankfurt (Oder), Germany

mao@ihp-microelectronics.com

***Abstract*—The paper presents a four stage 245 GHz LNA in SiGe technology. Common base (CB) topology is chosen for each stage. The amplifier takes advantage of passives like transmission lines and MIM capacitors to realize the input, output and inter-stage matching for the LNAs. The LNA has 12 dB gain at 245 GHz , a 3 dB bandwidth of 26 GHz. It has a supply voltage of 2V and power dissipation of 28mW. The amplifier is intended for the use in ISM band radar systems for consumer application and imaging radar.**

Keywords- LNA, mm-wave circuit, SiGe, transmission line, 245 GHz

I. INTRODUCTION

Silicon technology has made progress towards ever higher device cut-off frequencies , enabling the development of circuits in SiGe or even in CMOS for mm-wave applications beyond 100 GHz. [1] A ISM band at 245GHz with 2 GHz bandwidth is available in Europe, which could be mainly used for industrial, scientific, and medical applications, including low-cost radar systems for consumer applications, imaging radar for security applications and bio-medical sensors for medical diagnostics.

Various LNAs with different topologies like common emitter or cascode are reported. In [2] using SiGe technology, a differential 3 stage common emitter LNA at 60 GHz with 18 dB gain and 22 GHz 3dB bandwidth is reported. With differential topology the circuit can work robustly to bondwire inductances and variations of the on-chip ground potential are less harmful. In [3] a two stage cascode SiGe LNA with 13.5 dB gain and a noise figure of 9.6 dB at 122 GHz is reported. The cascode configuration is chosen for its high gain, high isolation and wide bandwidth.

For frequency as high as 245 GHz, gain achieved by each stage in case of common emitter topology is reduced dramatically compared to 60 GHz. Cascode topology although still provide high gain nevertheless the noise figure degrades with the increase of the operating frequency. In order to obtain high gain and while maintaining low noise figure for 245 GHz, this paper investigates another topology : common base and presents a four stage LNAs with high gain and low noise figure.

II. CIRCUIT DESIGN

Common base topology (CB) is chosen for each stage for its wide bandwidth, high gain, high isolation for the design frequency. Comparing common base stage with common emitter stage (CE), common-base stage does not contain a feedback capacitance from collector to emitter to cause the Miller effect. As a consequence, the bandwidth of the common base stage is much higher than common emitter stage. For circuit design up to the frequency of 245GHz, common base stage could achieve higher gain for each stage. Comparing common base stage with cascode topology, with comparable gain and comparable power, the noise figure of the common base topology is smaller than cascode topology. Table 1 shows a summary of simulation comparison between the three different topologies with transistors of the same sized biased at the same collector current density at 245 GHz.

From table I, the common base topology has much better gain performance than common emitter topology per stage. Comparing common base of 2 stages with cascode topology, gain of common base topology is a little higher than cascode, and noise figure is 1dB less than that of cascode topology. Power of the two are comparable.

Figure 1 shows the schematic of the four-stage CB LNA . With resistor ladder R1 and R2, pad V_{cb} provides the base bias for the common base transistor. The transmission lines TL_{sh} not only provide the dc ground for the emitters of the transistors but as well work together with the TL_{ser} and Metal-Insulator-Metal (MIM) capacitors C1,C2,C3,C4,C5 to form the input, output, and inter-stage impedance matching network. Transmission lines TL_{load} are inductive loads for each common base stage. C_{byp} provides the ac ground for the base connection and the dc supply. Besides, resistors R_{byp} and C_{byp} at the

TABLE I. A COMPRISON OF THREE TOPOLOGIES

	Three Topologys			
	CE	***CB (1 stage)***	***CB(2stage)***	***cascode***
Gain	1.9dB	3.2dB	6.2dB	5.6dB
NFmin	8.5dB	7.9dB	9.8dB	12.1dB
NF	8.7dB	9.4dB	10.8dB	12.1dB
Power	7m*1.5V	7m*2.0V	14m*2.0V	7m*3.5V

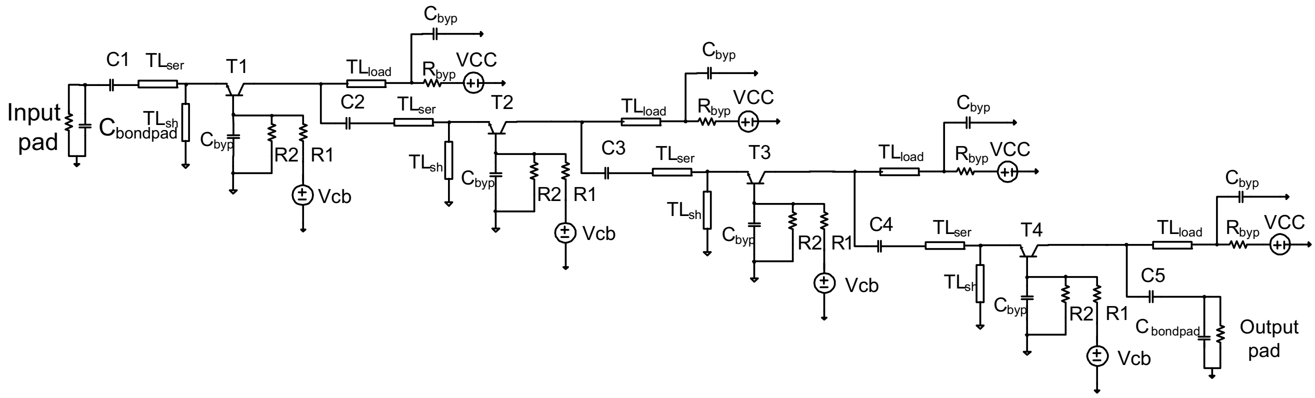

Figure 1. schematic of the 4 stage common base LNA

collector terminal form a low pass filter for the dc supply VCC, which helps to improve the isolation between CB stages. Bondpad capacitance $C_{bondpad}$ are also included in both the input and output matching networks.

The design was carried out using the transistor model of IHP for its experimental 0.25 um SG25 H1 BiCMOS (DotFive) technology. The technology has 5 metal layers. The 5 metal layers include 3 aluminum metal layers and 2 top-metal layers with 2um and 3um thickness respectively. Low-loss transmission lines could be designed with the two thick top-metal layers. The f_t and f_{max} of the experimental transistor are reported to be 300 GHz and 500 GHz respectively. [4]

All of the transmission lines were simulated with 2.5D planar EM-simulator (Momentum). The simulation results were fitted to transmission line model TLINP. And then TLINP is utilized in the design.

III. LAYOUT DESIGN

The chip photo of the LNA is shown in figure 4. The chip size is 0.42*0.46 mm^2, GSG input and output bondpads with 100um pitch length are utilized for on wafer measurement. Metal1 shielding is adopted for the pad design in order to prevent substrate loss and obtain high Q pad capacitance. On the left and right side are the input and output bondpads. On the top are the VCC and V_{cb} pads. Channel stop implant was blocked at critical places like input, output pad, transmission lines, long inter connects etc., in order to reduce the ohmic loss. Large areas of decoupling MIM capacitors are also included in the chip between the supply and the ground.

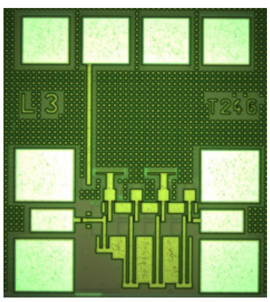

Figure 2. Chip photo

IV. SIMULATION AND MEASUREMENT RESULTS

For frequency as high as 245 GHz, frequency shift occurs for LNAs even if minor parasitics like pieces of short inter-connects, the terminal connections, parasitic bottom capacitor of the MIM capacitor etc. are introduced. Thus in order to give some frequency margin for measurement , two LNAs peaking at 245 GHz and at 265 GHz are designed. Figure 3 shows the S parameter simulation of the two LNAs. The two LNAs are both input and output matched to 50 Ohms. They can achieve 13 dB and 10 dB gain, 12 dB and 14 dB noise figure respectively at the designed frequency. Unconditional stability of the LNA is verified from dc to 300GHz.

Figure 4 shows the measurement result of the 265 GHz LNA. During the measurement with the original bias points in simulation, the LNA behaves unstable, and by reducing the bias voltage at the base terminal V_{cb} from 1.8 V to 1.55 V, the LNA becomes stable again. In order to give complete information, measurement results of two typical bias points are given. LNA with V_{cb} of 1.65V is not stable, with S22@212GHz above zero, it has power dissipation of 29mA*2V. LNA with V_{cb} of 1.55V is stable, it has a power dissipation of 14mA*2V. For the latter, the peak frequency shifts to 235 GHz. It has 12 dB gain at 245 GHz , and a 3 dB bandwidth of 26 GHz. Besides that, because the base is biased by resistor ladder, the LNA performance is sensitive to V_{cb}. Nevertheless this could be improved by more accurate transistor biasing circuits. Due to the limitation of the measurement equipment, the noise figure is not measured yet.

The difference between the simulation and measurement could be due to the parasitic inductance between base terminal and the ground. The inductance could come from the connection between base terminal and bypass capacitor (ac ground) or the unideal metal 1 ground plane and it is in the range of 1-5 pH. Nevertheless, at such high frequency 245 GHz , it affects the LNA performance a lot.

An analysis of the effect of the small parasitic inductance upon the common base is given below. In (1) ω_T is the cut off frequency of the transistor, g_m is the transconductance of the transistor and C_π is the base emitter capacitance. The impedance at the base terminal Z_B can be expressed by the parasitic inductance L_P as shown in (2). According to β-

transformation, from the emitter terminal, the impedance Z_E can be expressed by the base terminal impedance Z_B reflected back to the emitter as shown in (3); $\beta(j\omega)$ is the current gain of the transistor.[5] Inserting (2) into (3), (4) is obtained. From (4), the parasitic inductance at the base terminal introduces negative resistance at the emitter terminal.

$$\omega_T = \frac{g_m}{C_\pi} \tag{1}$$

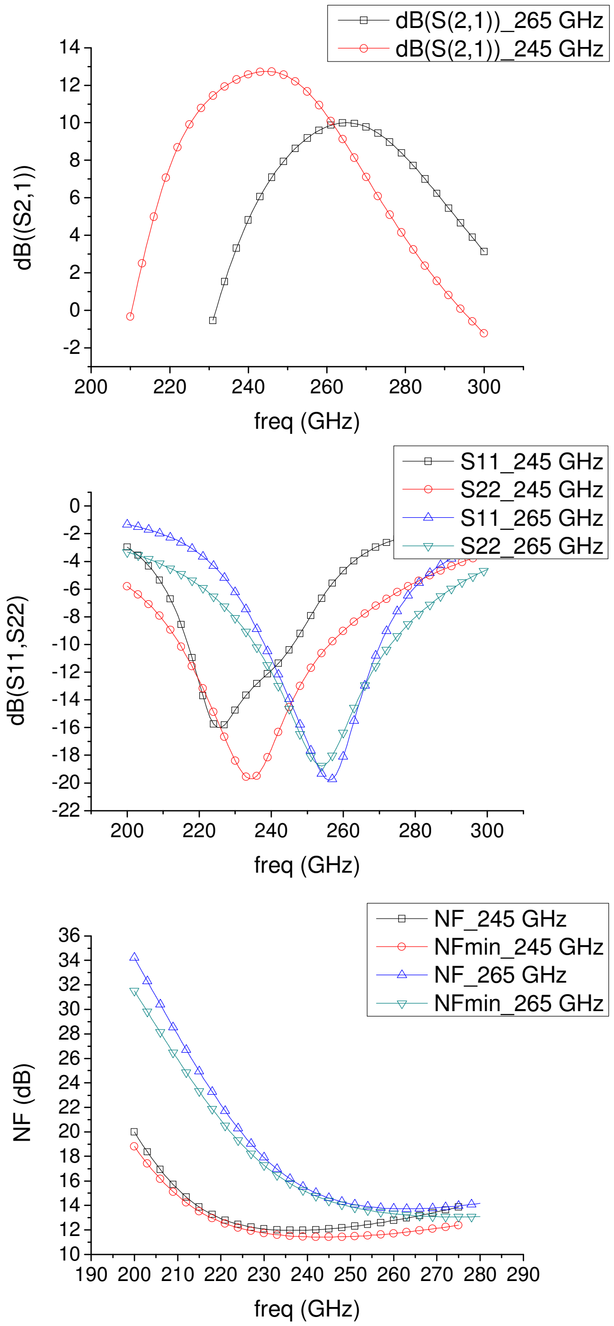

Figure 3. Simulation results of the 245 GHz and 265 GHz LNAs

$$Z_B = j\omega L_P \tag{2}$$

$$Z_E \approx \frac{Z_B}{\beta(j\omega)+1} \approx \frac{Z_B}{\left(\frac{\omega_T}{j\omega}+1\right)} \tag{3}$$

$$Z_E = \frac{(j\omega-\omega_T)L_P}{\left(\frac{\omega_T}{\omega}\right)^2+1} \tag{4}$$

The circuit is operating near f_T, $\omega \approx \omega_T$,

$$Z_E \approx \frac{(j\omega-\omega_T)L_P}{2} \tag{5}$$

From (5), the negative resistance is proportional to ω_T. ω_T is proportional to g_m, which is proportional to the collector current. The collector current is determined by the base emitter bias V_{be}. Thus by reducing base emitter bias voltage V_{be},

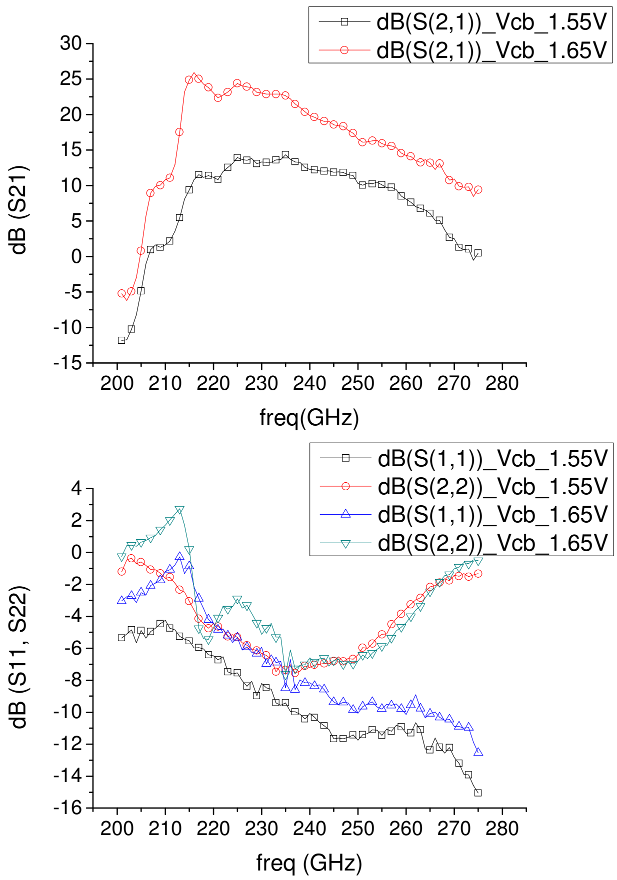

figure 4. Measured results of the 265 GHz LNA with different current density: 29mA*2V (V_{cb}: 1.65V) and 14mA*2V (V_{cb}: 1.55V)

collector current is reduced, ω_T is reduced and the negative resistance at the emitter can be reduced. In this way, the stability of the LNA is improved by decreasing the base terminal bias voltage.

In order to verify the explanation, an estimated parasitic inductance of 4pH is inserted between the base terminal and bypass capacitors (ac ground) for the 265 GHz LNA, and biased with the measured bias voltage value. S parameter simulation results of the LNA including the parasitic inductance is shown in figure 5. In comparison the measurement result is also plotted. The peak frequency is shifted to around 245 GHz due to the parasitic inductance, and the LNA could achieve higher gain even with lower collector current density. The simulation confirms the measurement result. Unconditional stability is verified across the 2 GHz to 300 GHz. Nevertheless, between dc and 2 GHz conditional stability is verified for specific frequency range. Furthermore, with reduced bias voltage value, taking advantage of the parasitic inductance, the LNA can have even smaller simulated noise figure, which is only 11 dB at 245 GHz. Table II shows a comparison of the simulation and measurement result of the LNA.

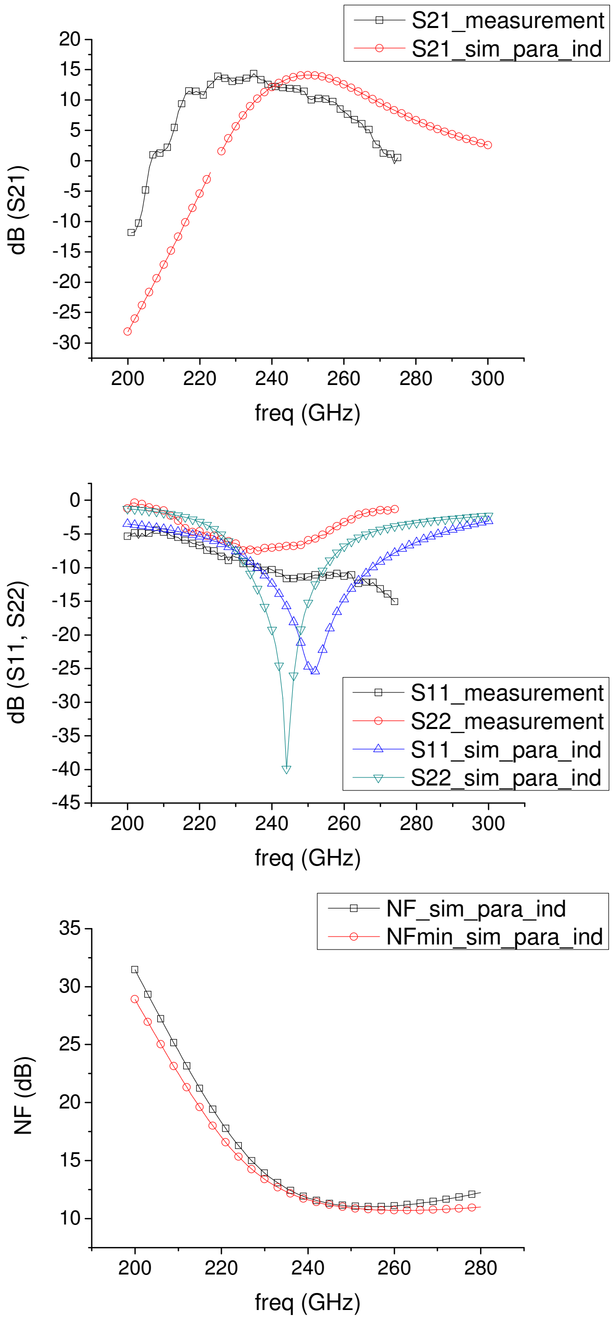

Figure 5. simulation results when the base inductance is included

TABLE II. A COMPRISON OF SIMULATION AND MEASUREMENT

	Simulation @265 GHz	*Simulation with parasitic inductance*	*Measurement*
S21	10 dB	14.1 dB	12 dB
Vcb	1.80 V	1.55 V	1.55 V
NF	13.7 dB	11.3 dB	-
NFmin	13.1 dB	11.2 dB	-
power	44mA*2V	16mA*2V	14mA*2V

V. CONCLUSION

A four stage common base 245 GHz LNA is designed and measured. A four stage common base 245 GHz LNA with 12 dB gain, 25 GHz 3-dB bandwidth, and a small power dissipation of 28 mW is demonstrated. The base bias voltage decreased to reduce current density compared with that in simulation. This phenomenon is explained and verified well by including a parasitic inductance between the base terminal and ground. Measurement results agree well with the simulation. This LNA will be used in a 245 GHz ISM band transceiver.

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