Virginia Polytechnic Institute and State University
Bradley Department of Electrical and Computer Engineering

ECE 5220: RFIC Design

CRN: 17491, MW 9:30 AM – 10:45 AM, RAND 121

Instructor: Dr. Kwang-Jin Koh

Office: 443 Whittemore Hall

Phone: (540) 231-7778

E-Mail: kkoh@vt.edu

Office Hours: Tentatively, Mondays 3:00 – 4:30 PM, Wednesdays 3:00 – 4:30 PM and by appointment (send e-mail)

Textbook: Behzad Razavi, *RF Microelectronics*, 2nd Ed., Prentice Hall, 2011

Thomas H. Lee, *Planar Microwave Engineering*, Cambridge University Press, 2004

References: P.R. Gray, P.J. Hurst, S.H. Lewis, and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th. ed., New York: Wiley, 2001.

A. Hastings, *The Art of Analog Layout*, Upper Saddle River, NJ : Prentice Hall, 2001.

H.L. Krauss, C.W. Bostian, and F.H. Raab, *Solid State Radio Engineering*, New York: Wiley, 1980.

L.E. Larson, ed., *RF and Microwave Circuit Design for Wireless Communications*, Boston: Artech House, 1997.

D.A. Johns and K. Martin, *Analog Integrated Circuit Design*, New York: Wiley, 1997.

D.M. Pozar, *Microwave Engineering*, 2nd. ed., New York: Wiley, 1998.

D.M. Pozar, *Microwave and RF Wireless Systems*, 2nd. ed., New York: Wiley, 2001.

B. Razavi, *Design of Analog CMOS Integrated Circuits*, Boston: McGraw-Hill, 2001.

These books will be on reserve at Newman Library.

Objective: The course focuses on Integrated circuit (IC) implementation of RF circuits for wireless communications applications. Topics include components for RFICs, RF amplifiers; noise, low noise amplifiers, mixers; power amplifiers, oscillators, and transceiver architectures. The course involves design of RF frontend components in a contemporary CMOS process using industry CAD tools.

Major Measurable Learning Objectives:

- Calculate noise (amplitude and phase), linearity, and dynamic range performance metrics for RF devices and circuits;
- Discuss transceiver architectures relevant to current wireless communications standards and their relative advantages and disadvantages;
- Discuss active and passive device technologies relevant to RFICs and their relative performance advantages and disadvantages;
- Design monolithic inductors for integrated amplifiers and oscillators;

- Design IC implementations of RF functional blocks (such as low-noise amplifiers, mixers and oscillators) based on foundry models and design rules to meet specifications for a wireless communications system;
- Discuss monolithic synthesizer architectures and their performance;
- Discuss issues in single-chip radio implementations; and
- Utilize RF/microwave CAD software in the design Describe the models for active devices in MOS and Bipolar IC technologies

Prerequisites: ECE 3204: (Analog Electronics II) and ECE 3614 (Intro. to Communication Systems) and either ECE 4605 (Radio Engineering) or ECE 4104 (Microwave and RF Engineering) -- The course builds on high-frequency circuit design as taught in ECE 4605 or ECE 4104, as well as fundamental background in analog circuits as taught in ECE 3204 and analog/digital communications as taught in ECE 3614.

Grading **(tentative)**:

Homework	20 %
Midterm	20 %
Final	30 %
Project	30 %

Total	100 %

Final course grades will be based on a number of factors, including absolute and relative performance. Letter grades will not be determined by a fixed curve or a fixed point range.

Grading policies: All homework is due by the **end** of the class on their due dates. **Late ones submitted by 4:30 PM on the same date are for 50 % of the penalty of the earned point. Any ones beyond that point will not be accepted**, unless approved by the instructor in advance.

If you feel that an error has been made in the grading of an assignment or an exam, you must present the work along with a **written** appeal to the instructor **within one week** after the graded work is returned to you. Verbal appeals will not be considered. Grades will not be changed after the one week period. Appeals should address specific grading errors -- negotiations over partial credit will not be considered.

Examination: There will be one midterm and one final during the semester, which may be closed or open book/notes. If it is closed book/notes, you will be allowed to bring in a few formula sheets.

No make-up exam will be given except for unforeseen, **officially documented** absences. If such a circumstance arises on a test date, you should contact the instructor as soon as possible. If you expect to be absent on a test date for **a legitimate reason** (such as a conference attendance and a job interview), you should contact the instructor **at least one week in advance**. So that a proper arrangement can be made.

Homework: Homework assignments may include conventional calculations, derivations, and/or simple design problems. All homework will be graded, with the grade based on effort for all problems and possibly the correctness of one or more selected problems.

Homework may be hand written. However, all information that is turned in for grading should be **neat, clearly organized, and legible**. Work that cannot be easily read (in the opinion of the instructor) will receive no credit. **The solutions with a cover page should appear in the order of the problems**, and the cover page should have necessary information such as homework assignment number, your name, and the Hokie Passport number. **Be sure to staple your pages together**. Submissions held together with folded corners, paper clips, or other such shaky manner will be penalized.

Design Project: The project, which is team work of a few students, involves the design, simulation, and full-custom layout of RF frontend functional blocks. **The project assignment will require a detailed final report.** The project assignment may also require a presentation, in which case, everyone is required to attend the presentations of the entire class and will evaluate other teams' works.

Presentation Day: TBD (be announced later)

CAD Tools: We will use Cadence CAD tools for the class project. Tutorials and help sessions, if necessary, for those tools will be provided, but use of CAD tools will not be covered in class.

Cadence tools are available on workstations in the ECE CAD and Visualization Laboratory (CVL, http://computing.ece.vt.edu). Every graduate student is eligible for an account.

Honor Code: Honesty in your academic work develops into professional integrity. As such, the Honor Code will be strictly enforced in this course. All aspects of your course work are covered by the Honor System. The examination and homework should be **your own work** unless otherwise noted.

Students may discuss general approaches to solving homework problems among themselves. Discussions and cooperative learning on general topics and CAD tools is also encouraged. **However, using another person's solution, design, implementation, or computer program or files are prohibited and will be considered as an Honor Code violation**. For more details on the relevant honor codes, consult the websites listed below:

- Undergraduate Honor System - http://www.honorsystem.vt.edu/
- Graduate Honor System - http://ghs.grads.vt.edu/

Special Needs: Any student who feels that he or she may need an accommodation because of a disability should see the instructor. Reasonable accommodations are available for a student who has a documentation of a disability from a qualified professional. Students should work through Services for Students with Disabilities (SSD) in 152 Henderson Hall. Any student with accommodations through the SSD Office should contact the instructor during the first two weeks of the semester.

Students requesting accommodations due to potential conflicts with the observance of specific religious or ethnic holidays or time periods should also contact the instructor in the first two weeks of the semester.

Lectures: Attendance will not be taken, but you are expected to attend lectures. If you must miss class, you are responsible for obtaining the notes from a classmate. Cell phones must be turned off during class. The lecture note for a class meeting will be posted on the Scholar website.

General: You are expected to show courtesy to the other students and the instructor by **not talking nor creating other disturbances** during class. Your cooperation is strongly requested and would be appreciated..

Tentative Course Schedule

This schedule is tentative and subject to change throughout the semester.

Week	Date	Topics	Readings
1	Jan. 16 – Jan. 18	Introduction, Impedance Matching (1)	Razavi: Ch.1-2 Lee: Ch.1-7
2	Jan. 23 – Jan. 25	Impedance Matching (2)	Razavi: Ch.1-2 Lee: Ch.1-7
3	Jan. 30 – Feb. 1	Noise Analysis (2)	Razavi: Ch.1-2 Lee: Ch.1-7
4	Feb. 6 – Feb. 8	Noise Analysis (1), Linearity Analysis (1)	Razavi: Ch.1-2 Lee: Ch.1-7
5	Feb. 13 – Feb. 15	Linearity Analysis (2)	Razavi: Ch.1-2 Lee: Ch.1-7
6	Feb. 20 – Feb. 22	No class (ISSCC forum presentation, make-up class will be scheduled later.)	
7	Mar. 3 – Mar. 7	No class (spring break, 03/03-03/11)	
8	Mar. 12 – Mar. 14	LNA design (2)	Razavi: Ch. 5 Lee: Ch. 12-14
9	Mar. 19 – Mar. 21	Midterm Exam Week	
10	Mar. 26 – Mar. 28	LNA Design (1), Mixer Design (1)	Razavi: Ch.5,6 Lee: Ch. 10,12-14
11	Apr. 2– Apr. 4	Mixer Design (2)	Razavi: Ch.6 Lee: Ch. 10
12	Apr. 9 – Apr. 11	VCO Design (2)	Razavi: Ch.8 Lee: Ch.15
13	Apr. 16 – Apr. 18	VCO Design (1), Power Amp. Design (1)	Razavi: Ch.8, 12 Lee: Ch.15, 20
14	Apr. 23 – Apr. 25	Power Amp. Design (2)	Razavi: Ch.12 Lee: Ch.20
15	Apr. 30 – May. 2	RX and TX Architectures (2)	Razavi: Ch.3,4,13
16	May. 7 – May. 9	Final Exam Week	

Hope you work hard, learn a lot, and enjoy the course.