VirginiaTech
Invent the Future

ECE 5220 RFIC Technology & Design (Introduction)

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Course Format

- Course name: ECE 5220 RFIC Technology & Design (CRN: 17491)
- Course time: 9:30 – 10:45 AM, Mon/Wed
- Lecture room: RAND 121
- Course instructor: Kwang-Jin Koh, kkoh@vt.edu, 540-231-7778
- Office hours: 3:00 – 4:30 PM, Mon/Wed, Room #: 4443 Whittemore
- Course website: Should be available soon in the ECE class website (VT scholar web).
- Text books:

✓ *Razavi* "RF Microelectronics", 2nd ed, Prentice Hall
(We will use this book as a "supplementary" textbook, in the sense that you can use it to reinforce the concepts from class.)

✓ *Thomas Lee* "Planar Microwave Engineering", Cambridge University Press
(This book contains comprehensive materials on RF and microwave ICs and systems as well. Good book for intuitive understanding of complex systems.)

Course Format (cont…)

- Course philosophy: We will focus on fundamental concepts of RF system, and specific RF circuit designs in the course.
- Prerequisite
  - Strong background in analog circuit analysis and design
  - Strong background in device physics of diode, BJT and MOSFET
    (*will not cover details of device physics, but simple small-signal and noise models for hand analysis and reading assignments*)
  - Good understanding of S-parameters
    (*will not cover details of S-parameter, but reading assignments*)
  - Basic understanding of communication theory
  - Basic understanding of microwave circuits

- Grading (tentative)
  - Mid term (15%), Final (25%), HW (30%), Design project (30%)
  - Details of design project will be announced later.

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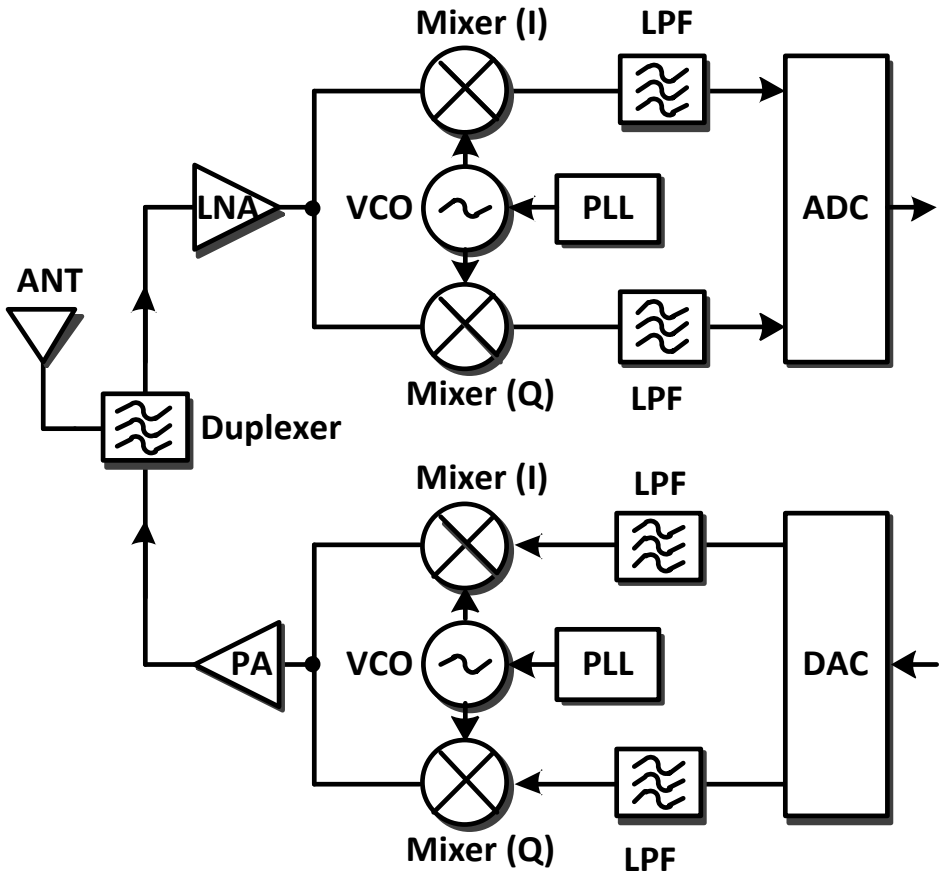
Course Schedule (#23-25 Lectures, Tentative)

Week	Date	Topics	Readings	HWs
1	01/18	Introduction, Impedance Matching (1)	R: Ch1-2, L: Ch1-7	
2	01/23, 01/25	Impedance Matching (2)	R: Ch1-2, L: Ch1-7	Hw-1
3	01/30, 02/01	Noise Analysis (2)	R: Ch1-2, L: Ch1-7	
4	02/06, 02/08	Noise Analysis (1), Linearity Analysis (1)	R: Ch1-2, L: Ch1-7	Hw-2
5	02/13, 02/15	Linearity Analysis (2)	R: Ch1-2, L: Ch1-7	Hw-3
6	02/20, 02/22	No Class (ISSCC forum presentation)	Make-up class be announced later	
7	03/03, 03/07	Spring Break (03/03 ~ 03/11)		
8	03/12, 03/14	LNA Design (2)	R: Ch 5, L: Ch12-14	Hw-4
9	03/19, 03/21	Midterm Exam Week		
10	03/26, 03/28	LNA Design (1), Mixer Design (1)	R: Ch 5,6, L: Ch12-14	Hw-5
11	04/02, 04/04	Mixer Design (2)	R: Ch 6, L: Ch10	
12	04/09, 04/11	VCO Design (2)	R: Ch 8, L: Ch15	Hw-6
13	04/16, 04/18	VCO Design (1), Power Amp. Design (1)	R: Ch 8, 12, L: Ch 15, 20	
14	04/23, 04/25	Power Amp. Design (2)	R: Ch 12, L: Ch 20	Hw-7
15	04/30, 05/02	Transceiver Architecture (2)	R: Ch 3,4, 13	
16	05/7, 05/09	Final Exam Week		

Course Overview

These are typical function blocks for a direct conversion radio.



What's direct conversion? (we will discuss this later in mixer design and transceiver architecture lectures.)

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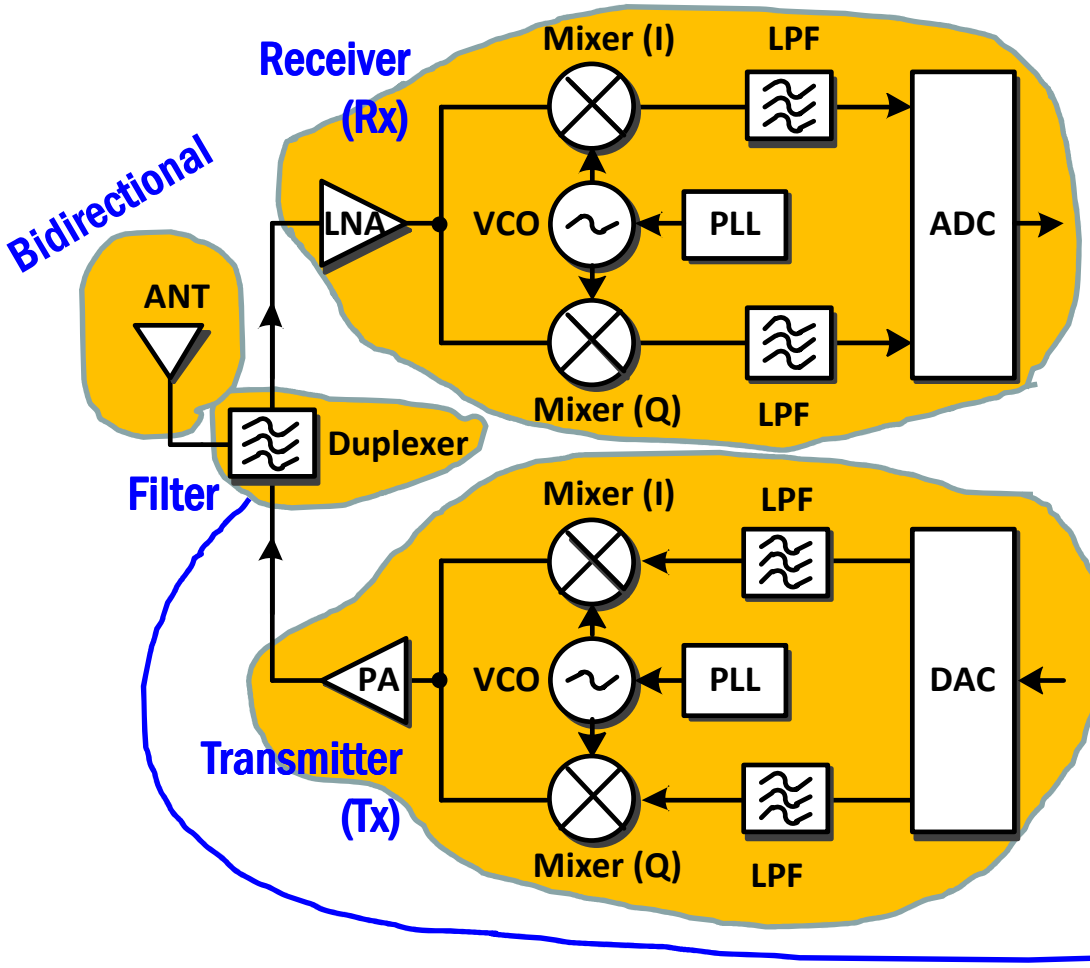
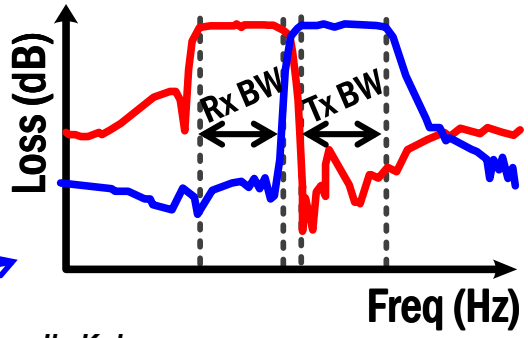


Antenna is bidirectional. It can send or receive RF signal.

After antenna, basically we have two paths; one is receiving RF signal from antenna (receiver or Rx), and the other is transmitting RF signal to antenna (transmitter or Tx).

Duplexer is a filter separating Rx and Tx signals.



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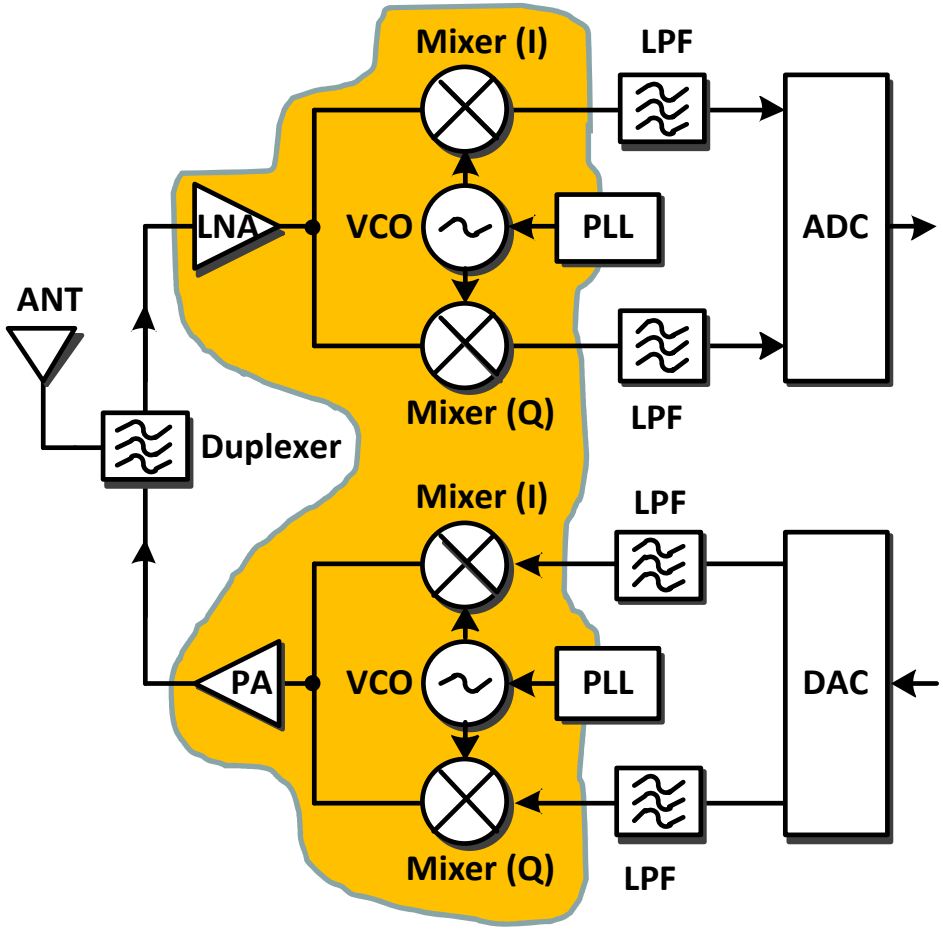

Usually when we say RFICs , they are mainly LNA, mixer, VCO, and power amplifier in this diagram, which operates at RF frequencies (several 100's MHz to several 10's GHz range).

PLL is mostly mixed-mode circuit, but it includes some function blocks being operated at RF frequencies, such as high frequency divider following VCO.

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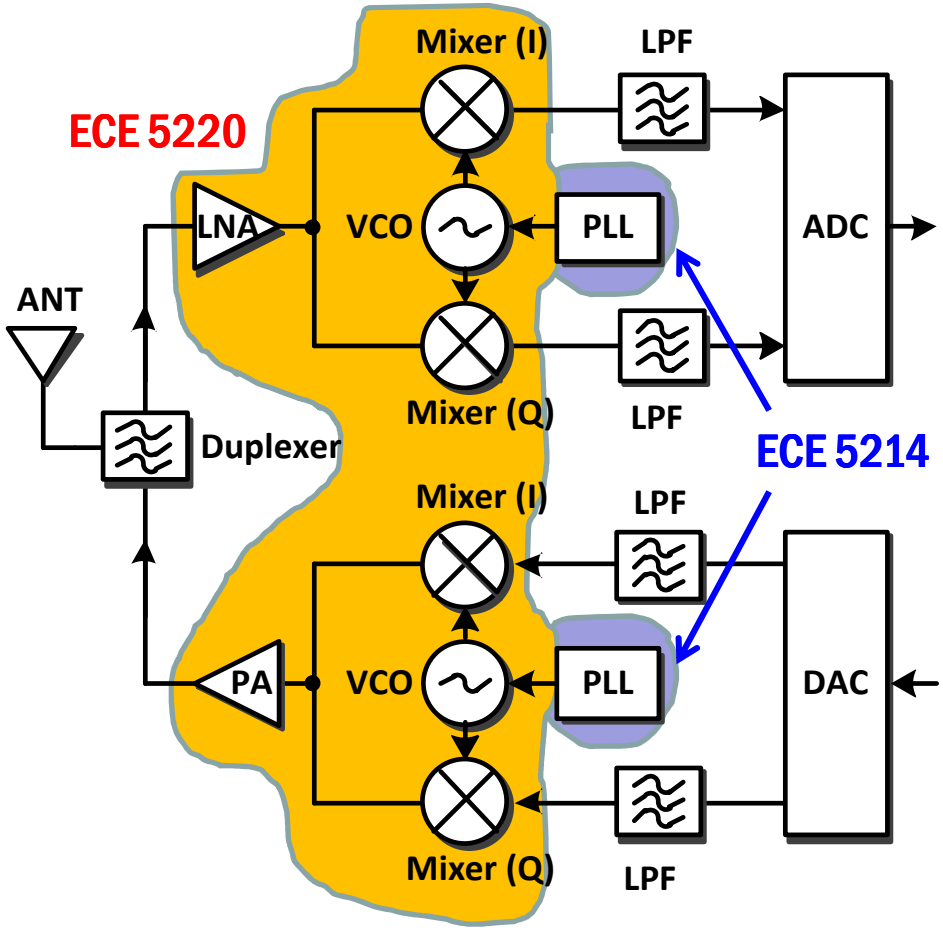

In this course, we will focus on mostly LNA, mixer, VCO and power amplifier designs.

PLL design is covered in "ECE 5214 Phased-Locked Loops: Theory and Practice" in current ECE curriculum.

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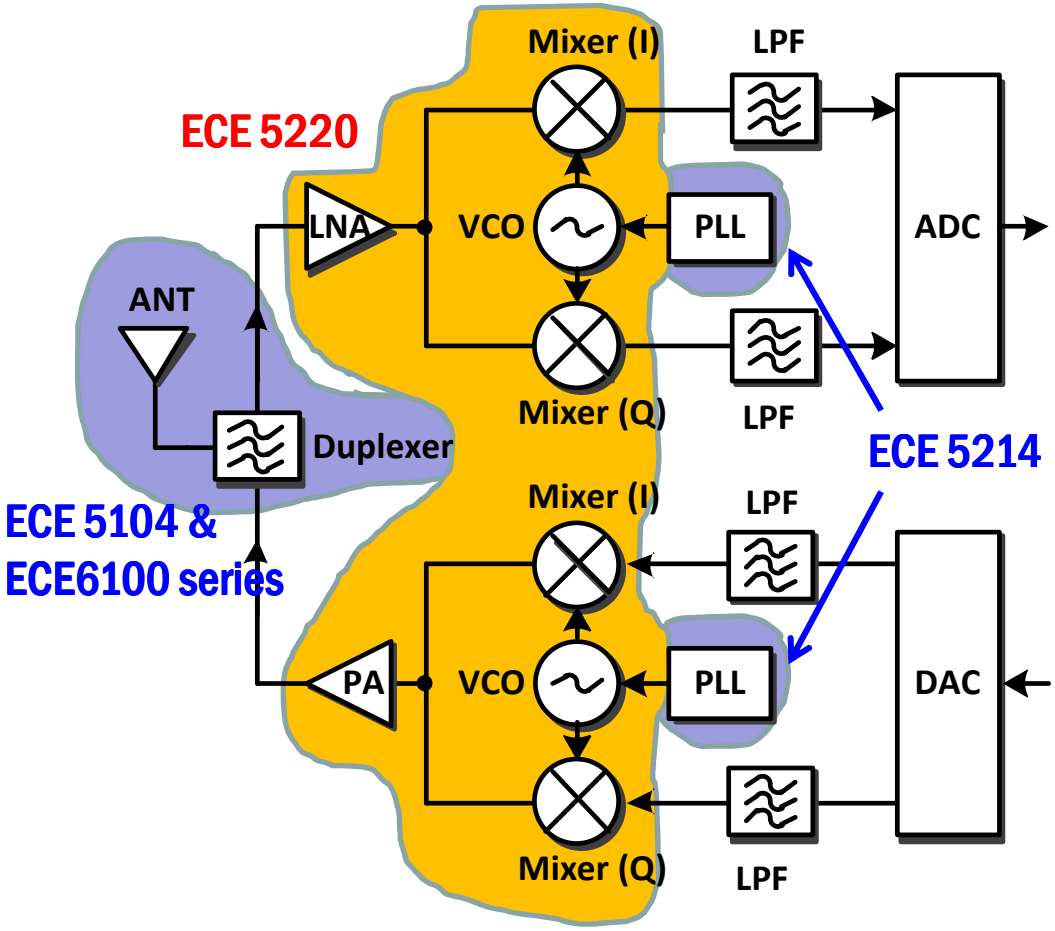

In this course, we will focus on mostly LNA, mixer, VCO and power amplifier designs.

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There are couple of courses handling antenna and duplexer filter designs (ECE 5104 & ECE6100 series).

Course Overview

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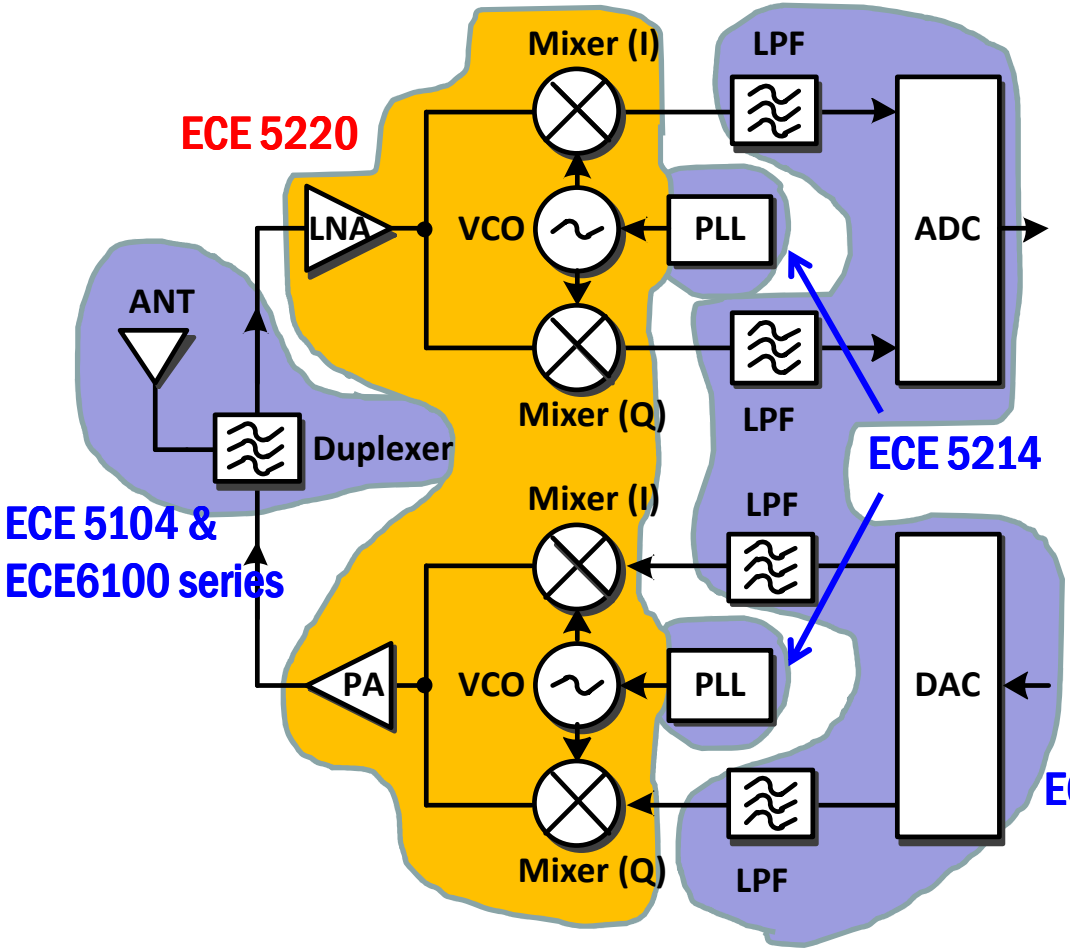
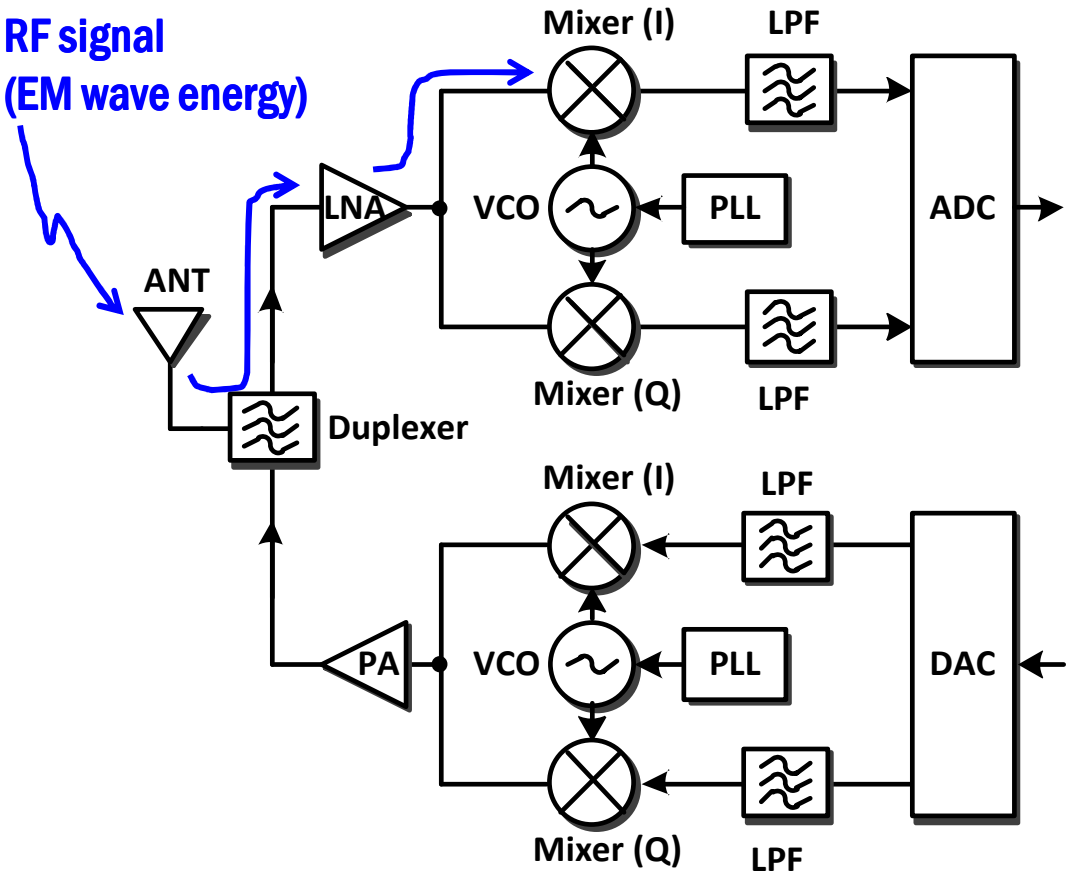


In this course, we will focus on mostly LNA, mixer, VCO and power amplifier designs.

The missing parts are baseband analog and mixed mode circuit designs. Some subjects in this area will be covered in "ECE4220 Analog Integrated Circuit Design" in fall semester.

Challenge in RF IC Designs

Where is difficulty in RF IC designs ?



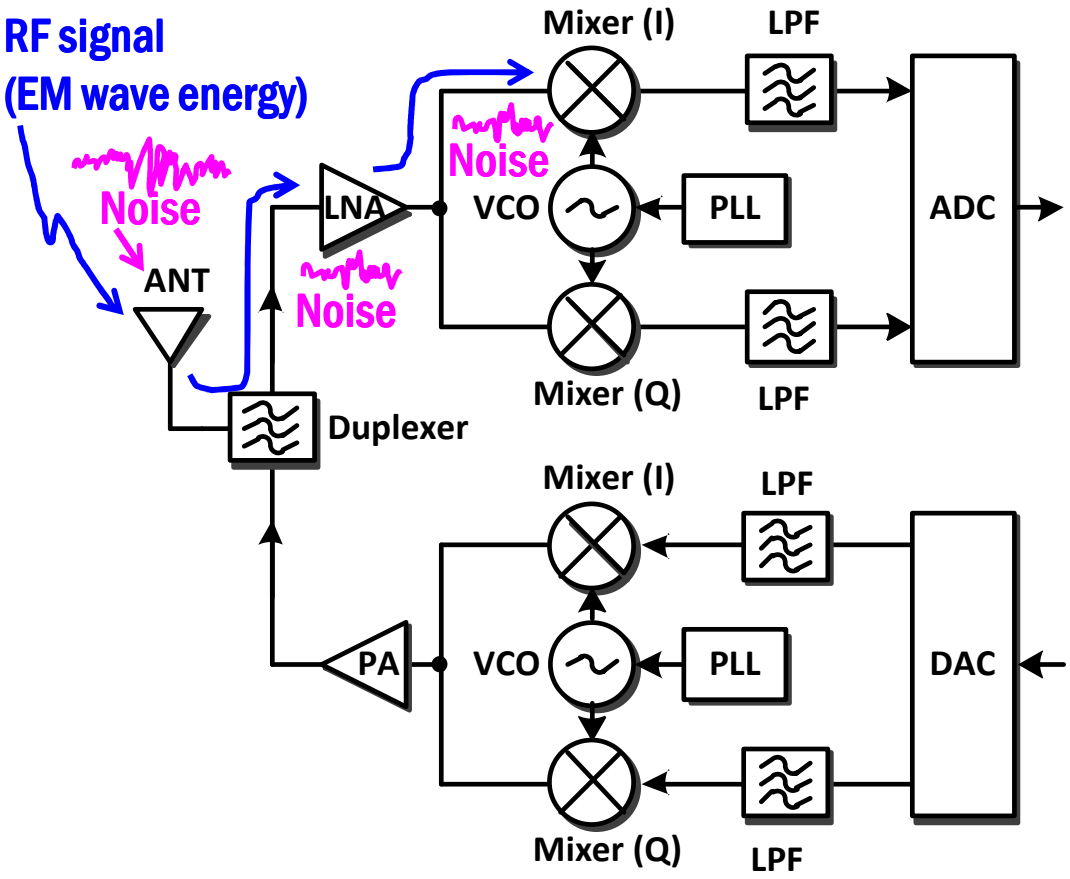
Well, let's think about in the Rx path first.

The role of antennal is to capture RF signal in the form of EM wave energy in the air medium. Usually its power level is very small (~pW level), and we want to maximize the captured power (or energy) in the antenna.

This is the issue related to "Impedance Matching".

Challenge in RF IC Designs

Where is difficulty in RF IC designs ?



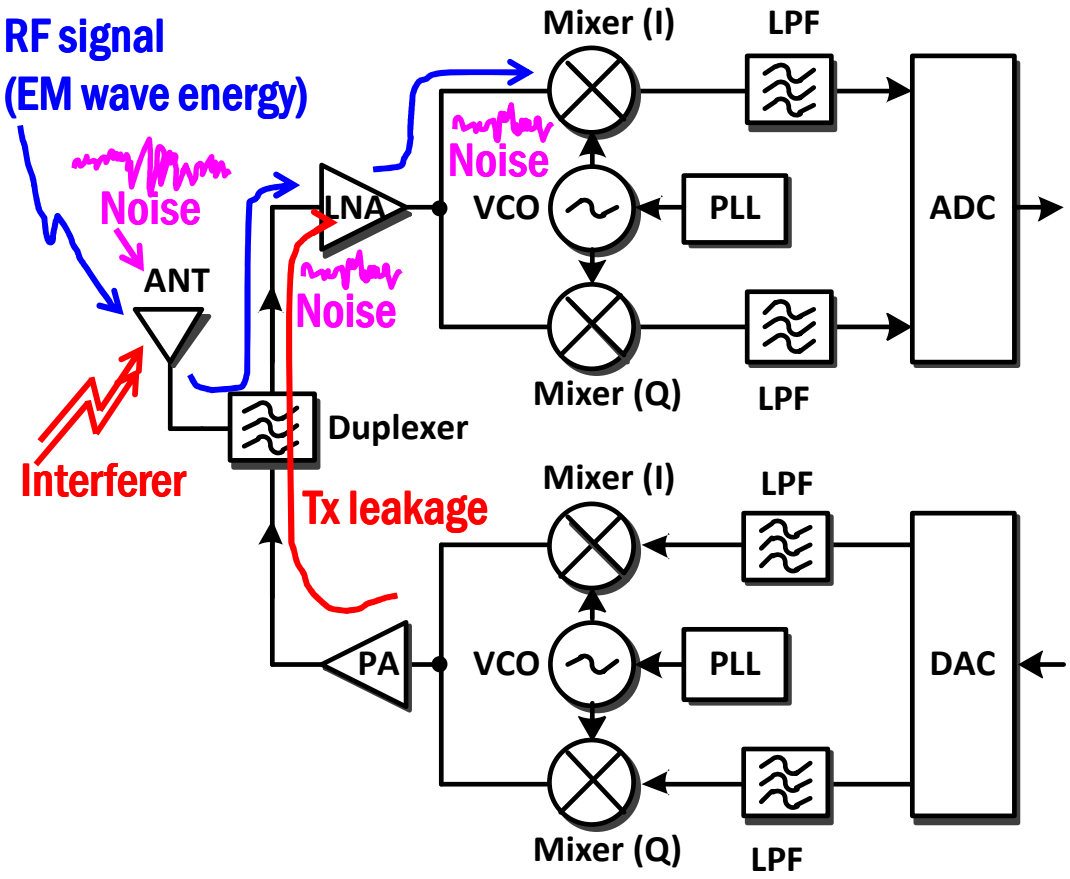
Well, let's think about in the Rx path first.

Not only signal but also noise will be coming through antenna. Inside chip, every electronics (LNA, mixer, ...) generates noise. If signal energy is smaller than noise energy, we can not get the signal (no communication).

This is the issue related to "Noise Analysis".

Challenge in RF IC Designs

Where is difficulty in RF IC designs ?



Well, let's think about in the Rx path first.

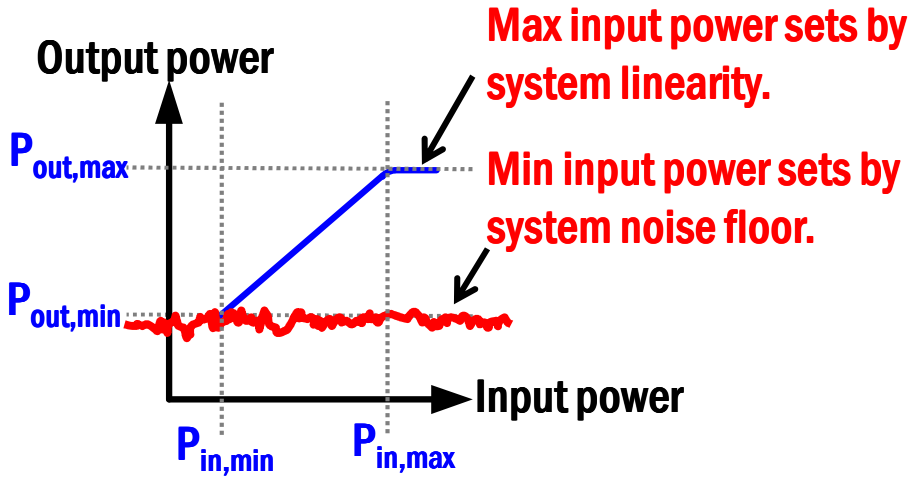
On top of noise, there will also be a strong interference from other base stations and cell phones. Strong Tx signal (~1W) will also be leaked to Rx path. These strong interference and leakage will distort (minor) or intermodulate (worst) wanted signal.

This is the issue related to "Linearity Analysis".

Challenge in RF IC Designs

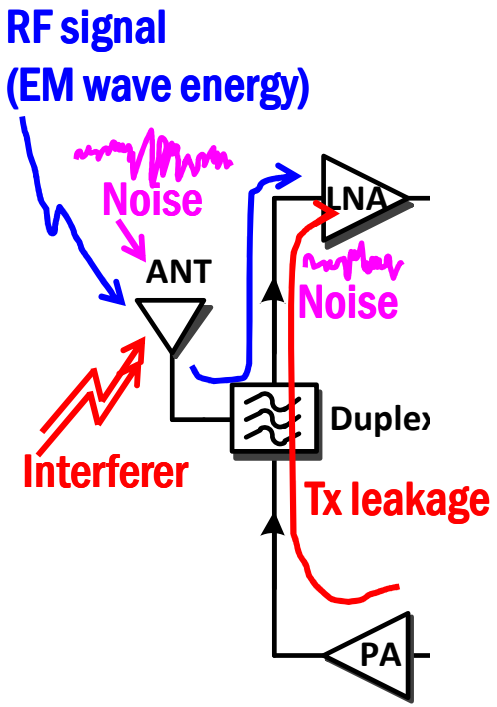
In summary,

- ❑ Most of wireless transceivers needs a impedance matching to maximize power transfer in the front-ends.
- ❑ Most of wireless transceivers have limited input power range, set by noise and linearity of the system (We call this range as input dynamic range, $P_{in,max}$-$P_{in,min}$).



We will study "impedance matching", "noise analysis" and "linearity analysis" first, before specific IC designs.

Challenge in RF IC Designs

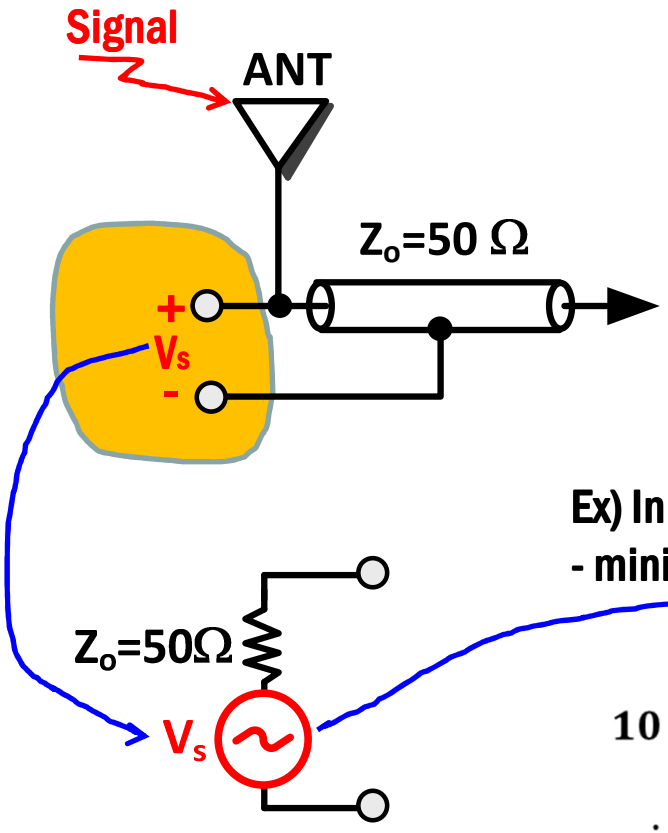


This is called "football field" metaphor, proposed by Paul Davis at Bell Labs.

Example) GSM system

- Because of noise, desired minimum received input power level needs to be larger than -102 dBm ($10^{-13.2}$ W, 1.8 uV_{rms}).
- But the largest interferer received by the antenna has a level of 0 dBm (10^{-3} W, 225 mV_{rms}).
- If you imagine the desired minimum input power to be normalized to the head of a pin (~ 1mm in diameter), then the largest interferer is roughly the size of two football fields, 100 m x 100 m.
- Receiving a GSM signal is analogous to the problem of finding the head of a pin in a football field without being able to actually going onto the field to look for it. In addition, this has to be accomplished in less than 100 ms, which is typically the time for the cellular handset to receive a call.

Quantifying Power Level at Antenna



Power levels in RF system are often quantified in terms of dBm. Power level in dBm is the relative power of the signal with respect to 1mW in dB:

$$P_{signal}(dBm) = 10 \times log\left(\frac{P_{signal}}{1mW}\right)$$

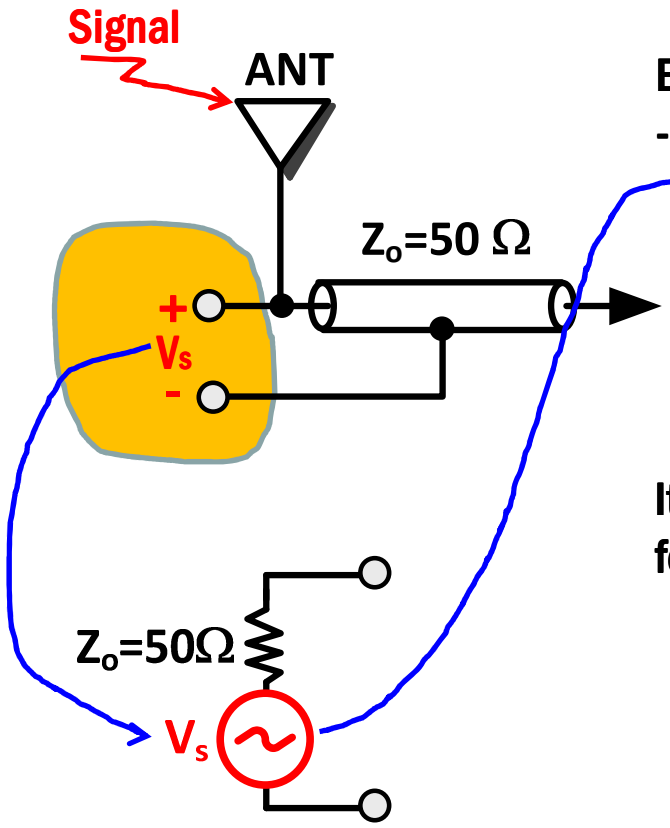
Ex) In RF systems, typical range of
- minimum input power level: -120 ~-100 dBm

Note: power is defined by 50Ω

$$10 \times log\left(\frac{\frac{V_s^2}{50\Omega}}{1mW}\right) = -120 \sim -100\ \text{dBm}$$

$$\therefore V_s = 0.225 \sim 2.25\ \mu V_{rms}\ \text{(in 50Ω system)}$$

Quantifying Power Level at Antenna



Ex) Similarly in RF systems, typical range of
- maximum input power level: -25 ~-20 dBm

Note: power is defined by 50Ω

$$10 \times log\left(\frac{\frac{V_s^2}{50\Omega}}{1mW}\right) = -25 \sim -20\ \text{dBm}$$

$$\therefore V_s = 12.8 \sim 22.5\ mV_{rms}\ (\text{in } 50\Omega \text{ system})$$

It will be a good engineering sense to have this feeling of number for RF system engineers.

$10\ mV_{rms}$ $(-27\ \text{dBm})$: *Very storng signal*
$1\ mV_{rms}$ $(-47\ \text{dBm})$: *Storng signal*
$10\ \mu V_{rms}$ $(-87\ \text{dBm})$: *Weak signal*
$1\ \mu V_{rms}$ $(-107\ \text{dBm})$: *Very weak signal*