VirginiaTech
Invent the Future

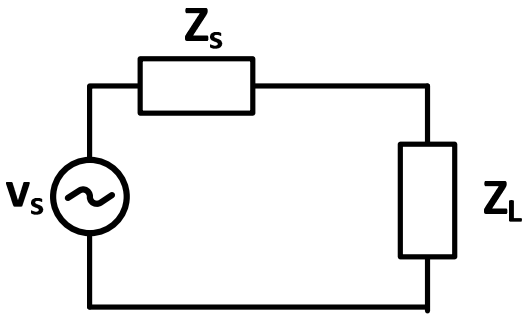
ECE 5220 RFIC HW -1

(Due: 02/06/2012, Hand in by the end of class time, 10:45AM)

Homework will still be acceptable by 4:30PM (office hour) 02/06/2012 after class with 20% degradation of the point you would earn otherwise.

Problem-1: Power penalty for mismatch

- When load impedance is not perfectly matched to source impedance, calculate power reduction factor (P_L/P_{max}) for the mismatch.



$$Z_s = R_s + jX_s$$

$$Z_L = R_L - jX_L$$

$$R_L = R_s + \Delta R_s$$

$$X_L = X_s + \Delta X_s$$

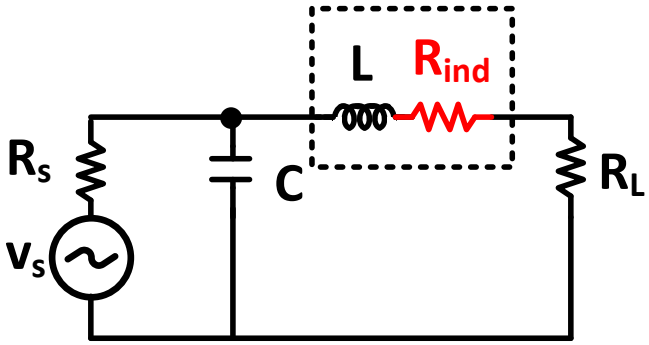
1) Derive output power (P_L) delivered to load resistance R_L under the mismatched condition.
2) Derive a power reduction factor, which is a ratio of P_L/P_{max} , where is P_{max} is the maximum power deliverable to load under perfect matched condition.
3) Based on the result in 2), fill in empty column in table below.

$\Delta X_s/X_s$	P_L/P_{max} (%)
5%	
10%	
20%	
50%	
Assume ΔR_s=0	

$\Delta R_s/R_s$	P_L/P_{max} (%)
5%	
10%	
20%	
50%	
Assume ΔX_s=0	

Problem-2: Power penalty for inductor loss

- Assume that inductor in the matching circuit shown below has finite resistance, R_{ind}.



1) Derive output power (P_L) delivered to load resistance R_L under the finite Q_{ind} of inductor.
2) Derive power (P_{ind}) delivered to R_{ind}.
3) Derive efficiency defined by $\eta = \frac{P_L}{P_L + P_{ind}}$.
4) Express η in terms of Q_T and Q_{ind}.

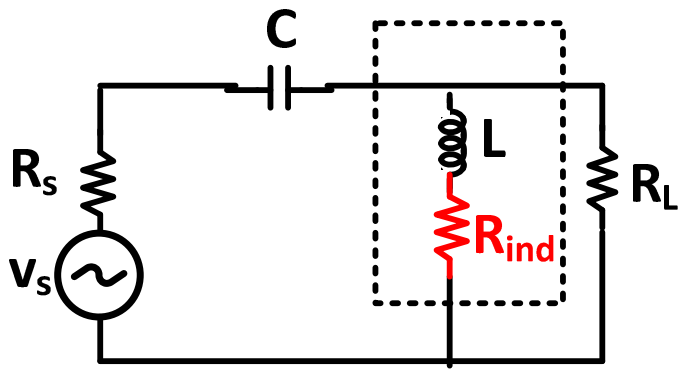
Definition:

$$Q_T = \frac{\omega_o L}{R_L} = \frac{1}{\omega_o C R_L} = \sqrt{\frac{R_s}{R_L} - 1}$$

$$Q_{ind} = \frac{\omega_o L}{R_{ind}}$$

Problem-3: Power penalty for inductor loss

- Repeat the same problems in Problem-2 for the case of impedance down conversion shown below figure.



1) Derive output power (P_L) delivered to load resistance R_L under the finite Q_{ind} of inductor.
2) Derive power (P_{ind}) delivered to R_{ind}.
3) Derive efficiency defined by $\eta = \frac{P_L}{P_L + P_{ind}}$.
4) Express η in terms of Q_T and Q_{ind}.

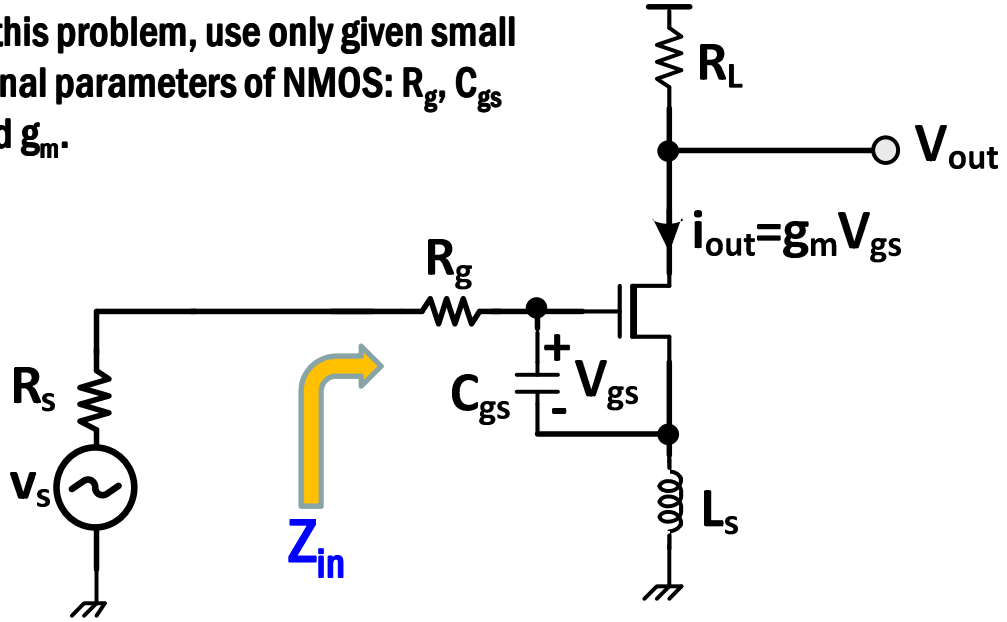
Definition:

$$Q_T = \frac{R_L}{\omega_o L} = \omega_o C R_L = \sqrt{\frac{R_L}{R_s} - 1}$$

$$Q_{ind} = \frac{\omega_o L}{R_{ind}}$$

Problem-4: LNA input matching

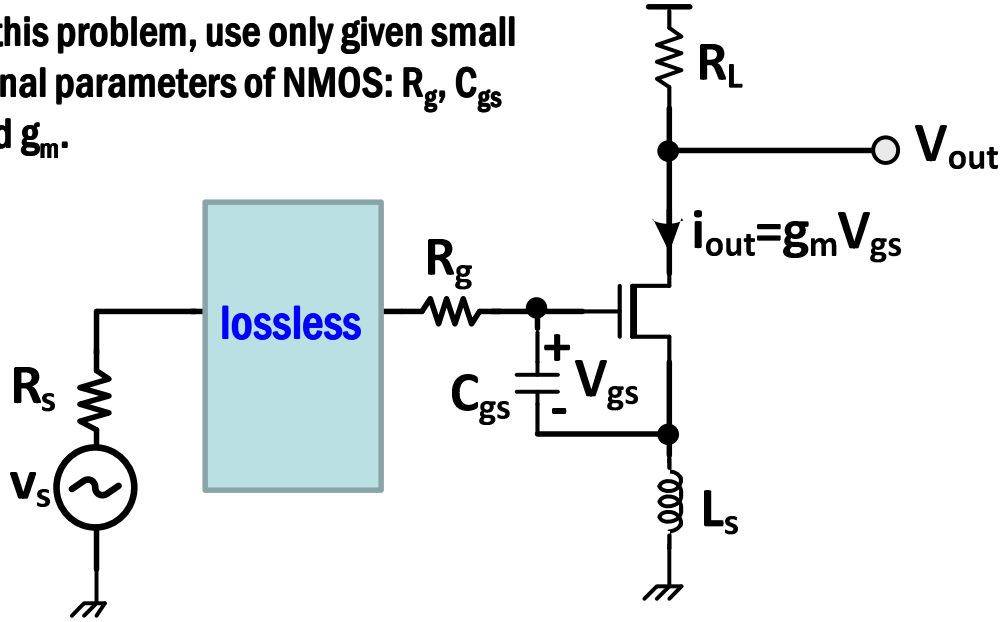
In this problem, use only given small signal parameters of NMOS: R_g, C_{gs} and g_m.



1) Derive input impedance Z_{in}.
2) Under directly being driven by source, calculate V_{gs} and output current i_{out}.
3) Calculate voltage gain $\mathbf{Av} = \frac{\mathbf{V_{out}}}{\mathbf{V_s}}$.

Problem-4: LNA input matching

In this problem, use only given small signal parameters of NMOS: R_g, C_{gs} and g_m.



4) Assume that real part of Z_{in} in 1) is equal to R_s. Design lossless matching network for maximum power transfer (assume $\omega_o L < 1/(\omega_o C_{gs})$, where ω_o is target frequency for matching).

5) Under matched conditions, calculate V_{gs} and output current i_{out}.

6) Calculate voltage gain $Av = \frac{V_{out}}{V_s}$, and compare the result with that of 3).

7) Explain the role of source inductor L_s in view of impedance matching.