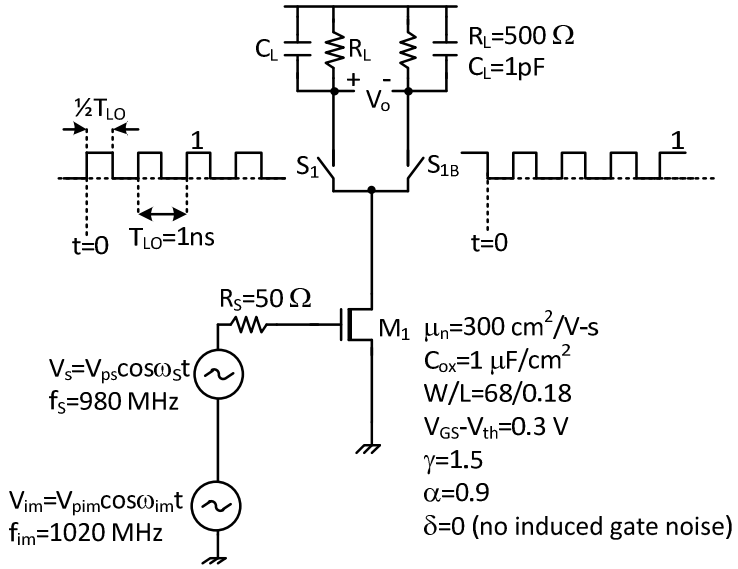
ECE5220 RFIC Final Exam, Due: 4PM, 05/10/2012 (Thursday) Name: Grade:

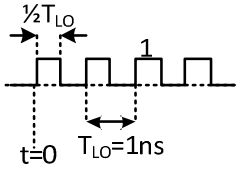
1. In the mixer shown below, DC characteristic of the NMOS, M1, is set by square-law characteristic, i.e.

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2.$$

Assume that Rs << 1/ωCgs and NMOS has only drain thermal noise current, i.e., no gate induced noise and parasitic gate resistance. The drain thermal noise coefficient is γ. S_1 and S_{1B} are ideal differential switches driven by ideal rectangular pulse trains whose duty cycle is 50%. **R_L is noisy load resistor**.



*You may need this series expression for question #1.

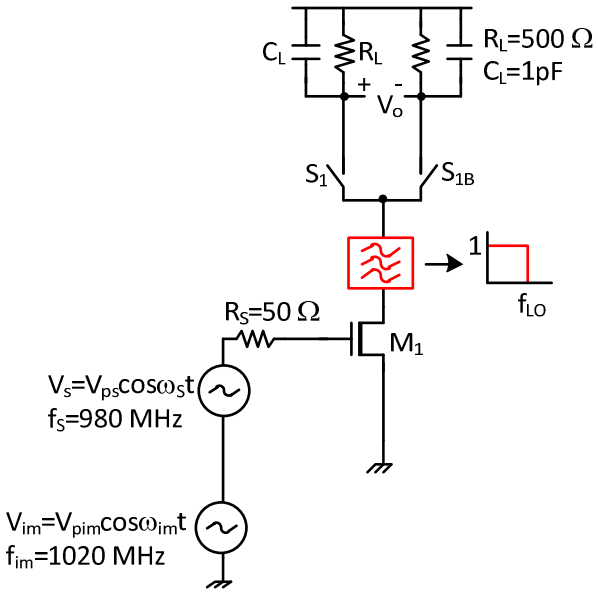


$$\mathrm{rect}(t) = \frac{1}{2} + \sum_{n=1}^{n=\infty}\left(\frac{2}{(2n-1)\pi}sin(2n-1)\omega_{LO}t\right)$$

1) Assume no image signal (V_{pim}=0) and V_{ps}=1mV_{peak}. Calculate ***rms*** output signal power (S_o) and output noise power ($N_o/\Delta f$) density and noise factor F (15 pt).
(Note: K=1.38x10^{-23} J/K, T=300 K)

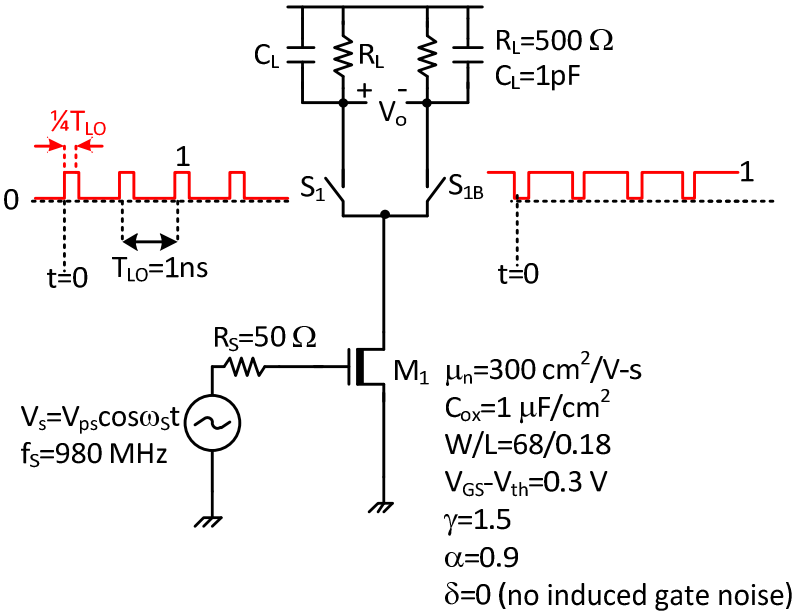
2) Repeat 1) when W/L increased twice while maintaining same bias current (10 pt).

3) What's output signal power if the image tone has same magnitude as signal, i.e., V_{pim}=V_{ps}=1mV_{peak} (5 pt) ?



4) Now, in order to remove the image tone, let's apply ideal brick-wall type low pass filter (LPF) as shown above. Calculate output noise power and noise factor. Assume that the LPF is noiseless (5 pt).

(Note: the image rejection filer will also reject noise and help to improve SNR. In general, the M1 can be regarded as LNA and the switches (S1 and S1B) as mixer, respectively. You could understand the role of a filter between LNA and mixer through this example.)

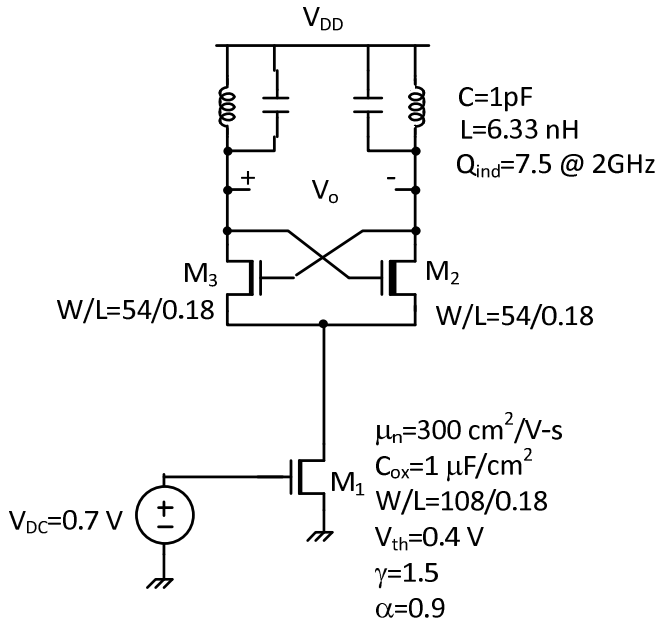


5) Now let's change the LO clock duty cycle from 50% to 25% as shown above, and all the other conditions are same as 1) and no image signal. Calculate ***rms*** output signal power (S_o) and output noise power (N_o) and noise factor F (15 pt).
(Note: non-50% duty cycle also generates RF leakage to IF output node due to DC component of LO waveforms.)

2. In the VCO shown below, DC characteristic of the NMOS, M1-3, is set by square-law characteristic,

$$\mathrm{I}_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2.$$

Assume that Cgs of M2-3 is negligible compared with C in the LC-tank. For simplicity, let's further assume that dominant noise sources are M1 and parasitic resistance from LC-tank, and noises from M2-3 are negligible. M1 has only drain thermal noise current, i.e., no gate induced noise and parasitic gate resistance.



1) Calculate the possible maximum output signal swing in peak-to-peak value and set minimum supply voltage VDD that allows the maximum output swing (5 pt).
(Note: Each NMOS needs at least minimum $V_{ds,sat}$ during full output swing excursion to sustain oscillation.)

2) Under the bias condition determined in 1), calculate phase noise contributions from parasitic resistance from inductor at 10 MHz offset frequency (10 pt).

3) Under the bias condition determined in 1), calculate phase noise contributions from M1 at 10 MHz offset frequency (10 pt)
(Note: You don't need to calculate phase noise contribution due to flicker noise of M1, since at 10MHz offset dominant noise source will be thermal noise of M1.)

4) Under the bias condition determined in 1), calculate total phase noise at 10 MHz offset frequency (5 pt).

5) Now, let's use ideal filter which will reject noise at $2xf_{osc}$ from M1 completely (f_{osc} is output oscillation frequency). Assume the filter is noiseless. Calculate phase noise contribution from M1 at 10MHz offset. How much improvement will it achieve compared with 3) through filtering the second harmonic noise? (20 pt).