DC Stability (2)

①

- Common-mode DC feedback ⇒ common-mode feedback load
- What could be an issue in this common-mode feedback load?

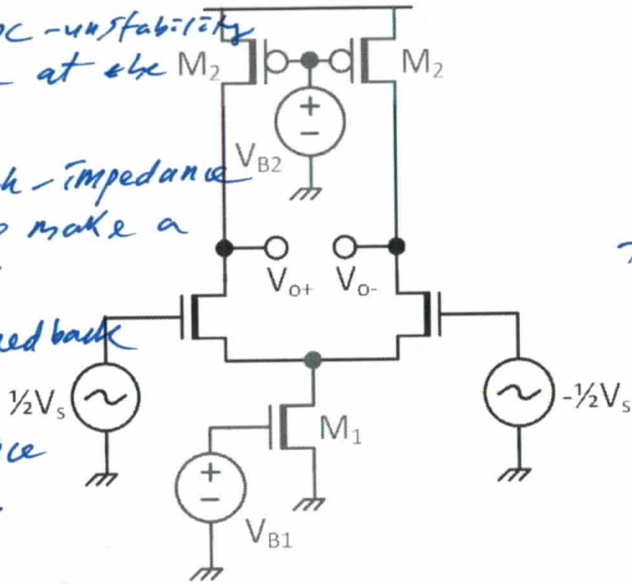
DC-feedback-loop

(*) The source of DC-unstability
→ high impedance at the output node

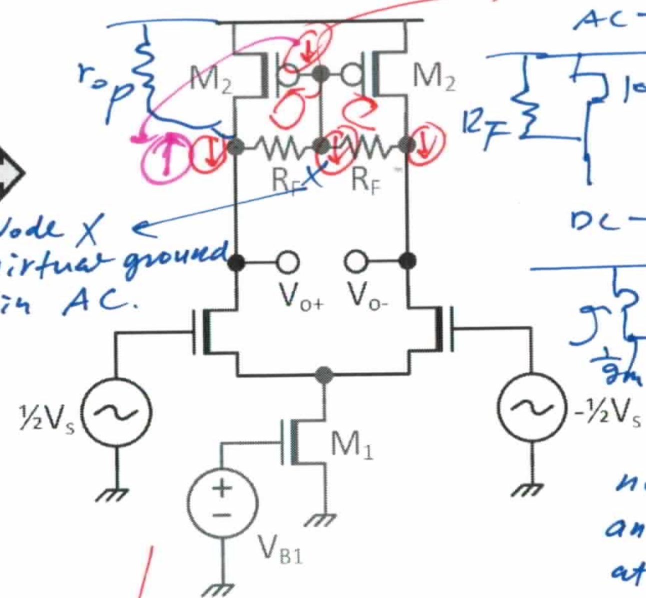
→ We need high-impedance at A-C to make a large gain

→ Apply DC-feedback to lower output impedance at DC only.

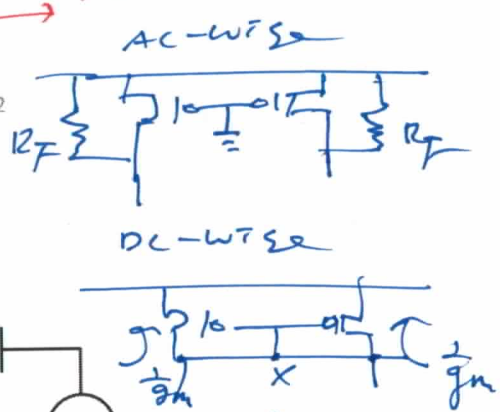
→ "common-mode DC feedback"



⇨



Node X ← → virtual ground in AC.



node X will sense any DC variation at output node

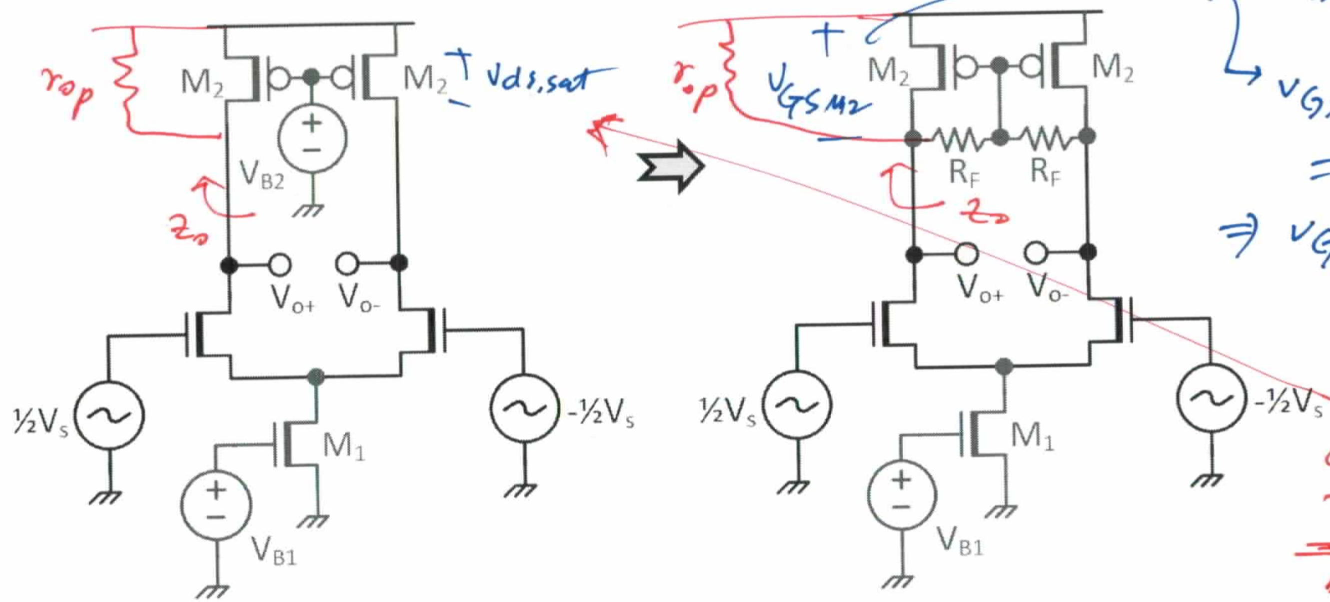
→ This DC variation will be suppressed by PMOS.

Issue
① $Z_o = r_{op} // R_F \ll r_{op}$
② Voltage head room

See next page.

DC Stability (2)

- Common-mode DC feedback ⇒ common-mode feedback load
- What could be an issue in this common-mode feedback load?



$V_{GS,M2} - V_{th} = V_{DS,sat}$

$\Rightarrow V_{GS,M2} = V_{DS,sat} + V_{th}$

$z_o = r_{op}$

$z_o = r_{op} \parallel R_F$

output impedance becomes smaller in common-mode feedback load than standard case.

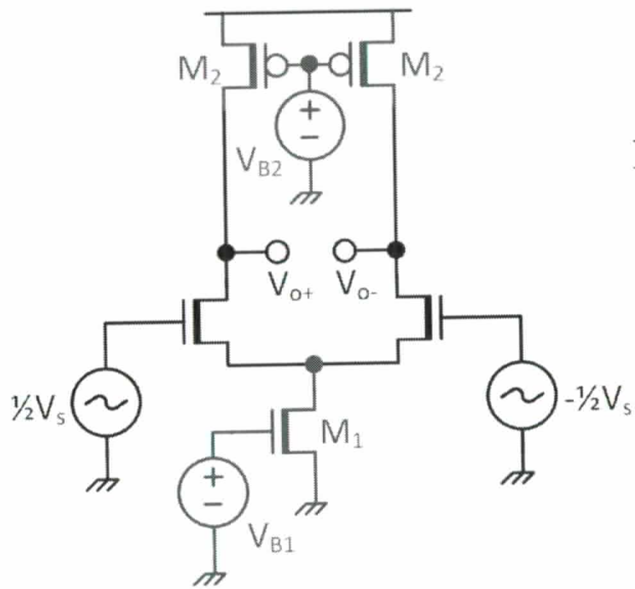
common-mode feedback load will sacrifice voltage headroom by one V_{th}.

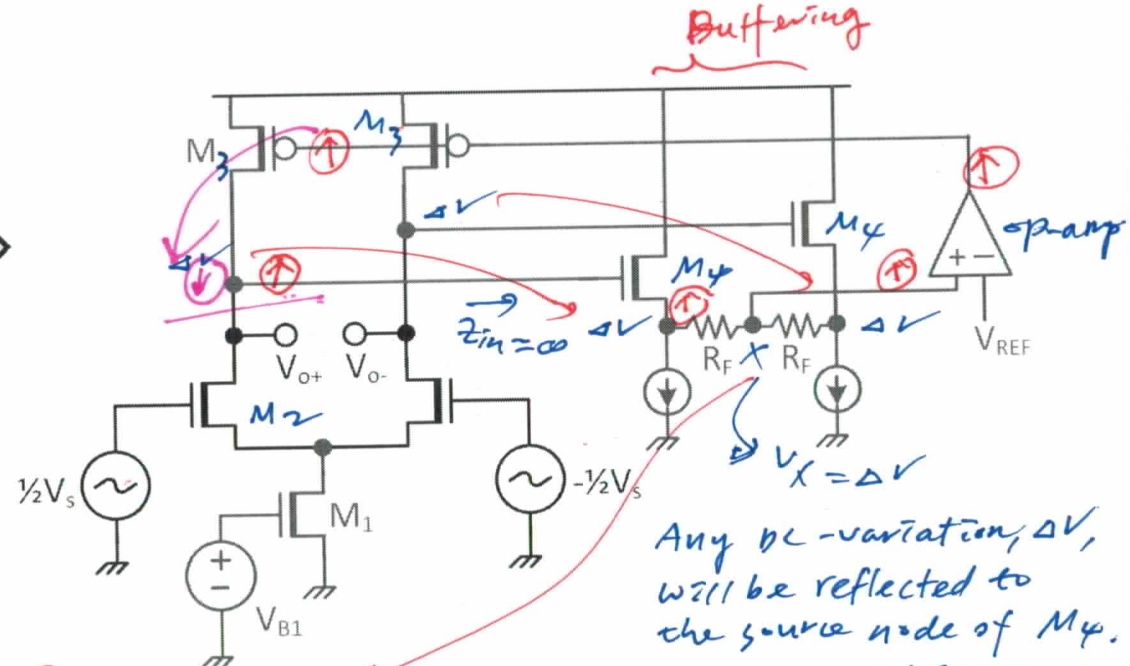
How to fix these issues?
Ans) Apply buffering.

DC Stability (3)

(3)

- Apply buffering first, then common-mode DC feedback (why?)





- No voltage headroom sacrifice
- No output impedance degradation

AC-wise node X is virtual ground.

Any DC-variation, ΔV, will be reflected to the source node of M4.

→ node X will sense ΔV,

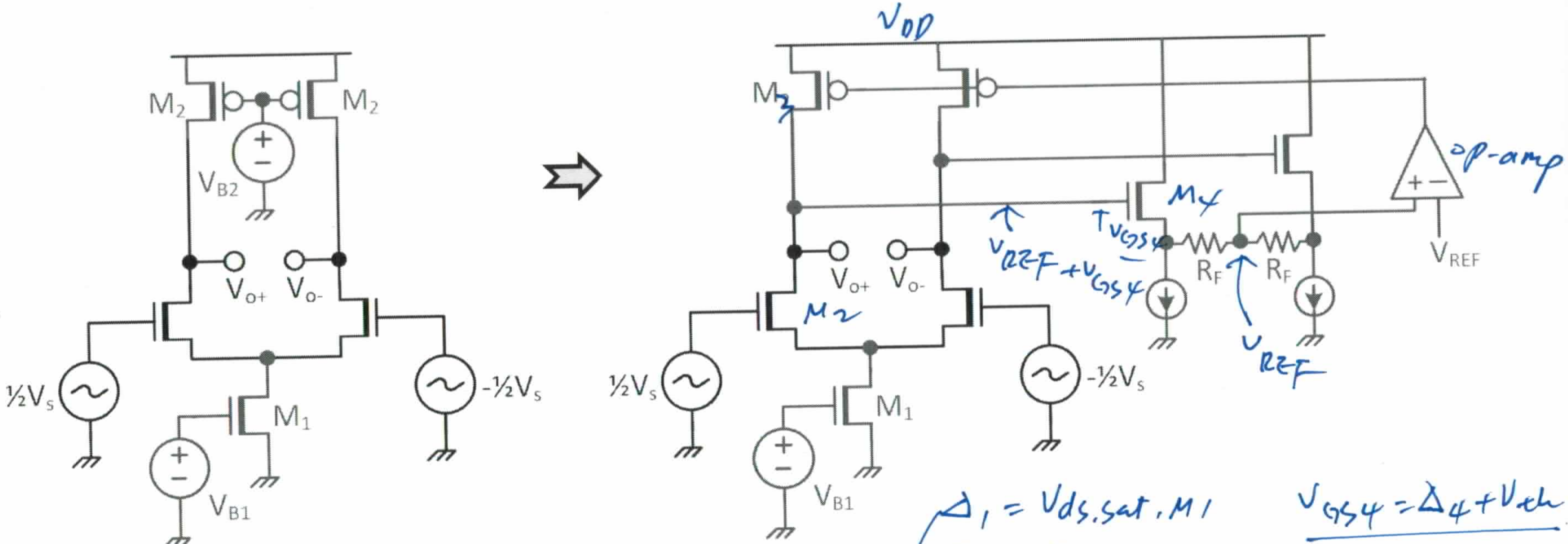
→ op-amp generates a control voltage for PMOS

→ PMOS will suppress the DC variation, ΔV, in negative direction

→ DC negative feedback

DC Stability (3)

- Apply buffering first, then common-mode DC feedback (why?)



$\Delta_1 = V_{ds,sat,M1}$
$\Delta_2 = V_{ds,sat,M2}$
$\Delta_3 = V_{ds,sat,M3}$
$\Delta_4 = V_{ds,sat,M4}$

$V_{GS4} = \Delta_4 + V_{th}$

Q) what's the range of V_{REF} so that all transistors operates in saturation mode?

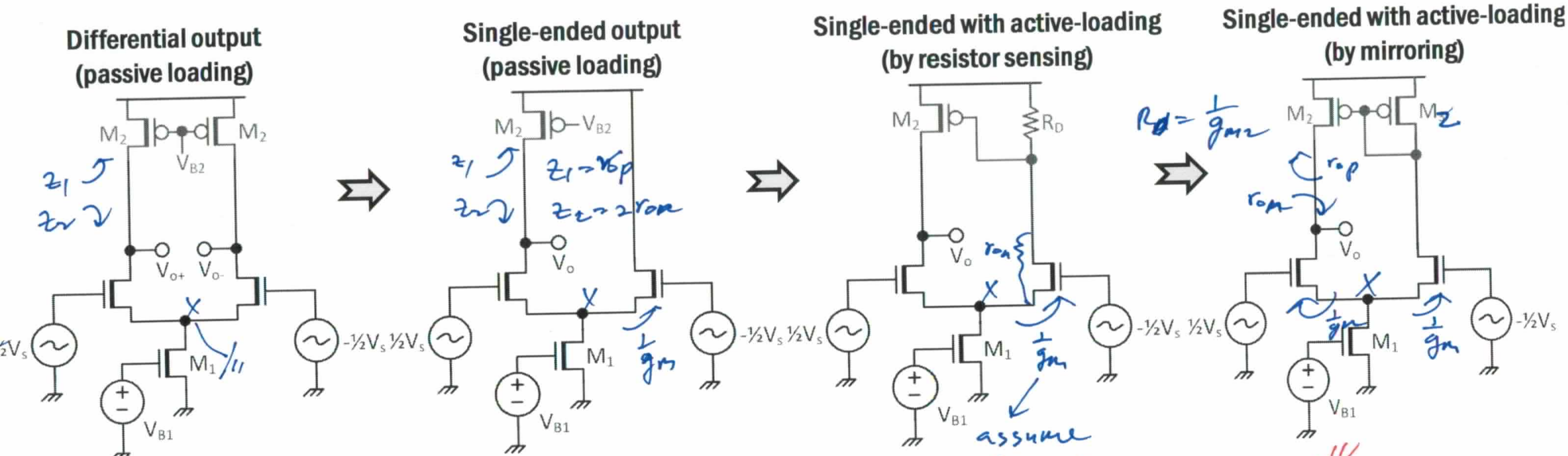
$$\Delta_1 + \Delta_2 \leq V_{REF} + V_{GS4} = V_{REF} + V_{th} + \Delta_4 \leq V_{DD} - \Delta_3$$

$$\Delta_1 + \Delta_2 - \Delta_4 - V_{th} \leq V_{REF} \leq V_{DD} - \Delta_3 - \Delta_4 - V_{th}$$

Note: V_{REF} needs to satisfy all DC conditions inside op-amp as well.

Active Loading

- These topologies are for single-ended output.



perfect symmetry
→ X ⇒ virtual ground node
→ $z_1 = r_{op}$, $z_2 = r_{on}$
→ $A_v = g_m(r_{on} || r_{op})$

assume $R_D << r_{on}$

Not symmetry
→ X ⇒ Not virtual ground

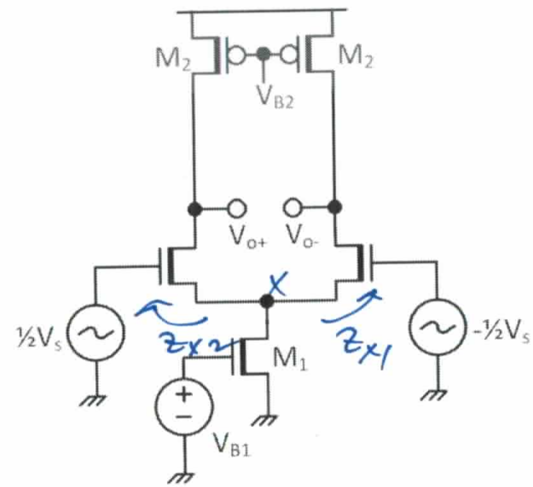
$R_D = \frac{1}{g_{m2}}$

can be regarded as symmetry circuit
→ X ⇒ virtual ground
→ $A_v = g_m(r_{on} || r_{op})$

same
(see next slides for more details)

Some Comments On Applying Virtual Grounding

- When can we apply virtual grounding in differential topologies (and when can't)?



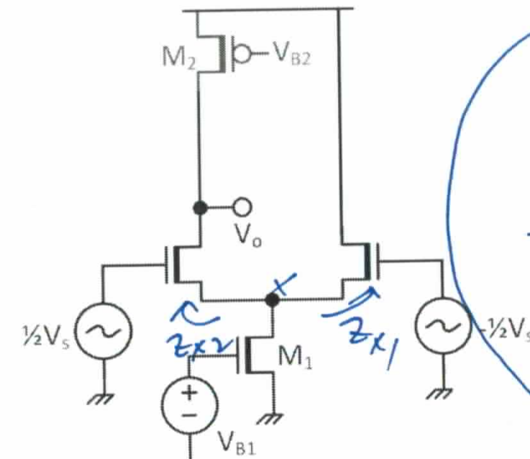
$Z_{X1} = Z_{X2} = Z_X$

V_X by $\frac{1}{2}V_s$ only $\rightarrow V_{X1} = \frac{g_m Z_X}{1+g_m Z_X}\left(\frac{1}{2}V_s\right)$

V_X by $\left(-\frac{1}{2}V_s\right)$ only $\rightarrow V_{X2} = \frac{g_m Z_X}{1+g_m Z_X}\left(-\frac{1}{2}V_s\right)$

$V_X = V_{X1} + V_{X2} = 0$

$Z_{X1} = Z_{X2} \rightarrow$ can apply virtual ground at node-X.



$Z_{X1} \neq Z_{X2}$

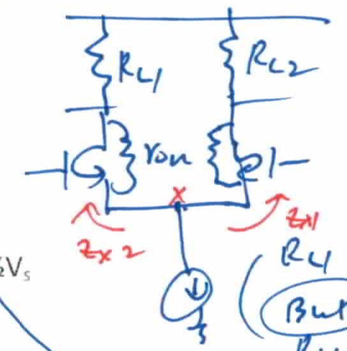
$V_{X1} = \frac{g_m Z_{X1}}{1+g_m Z_{X1}}\left(\frac{1}{2}V_s\right)$

$V_{X2} = \frac{g_m Z_{X2}}{1+g_m Z_{X2}}\left(-\frac{1}{2}V_s\right)$

$V_X = V_{X1} + V_{X2} \neq 0$

$\rightarrow$ can't apply virtual ground at node-X

How about this one?



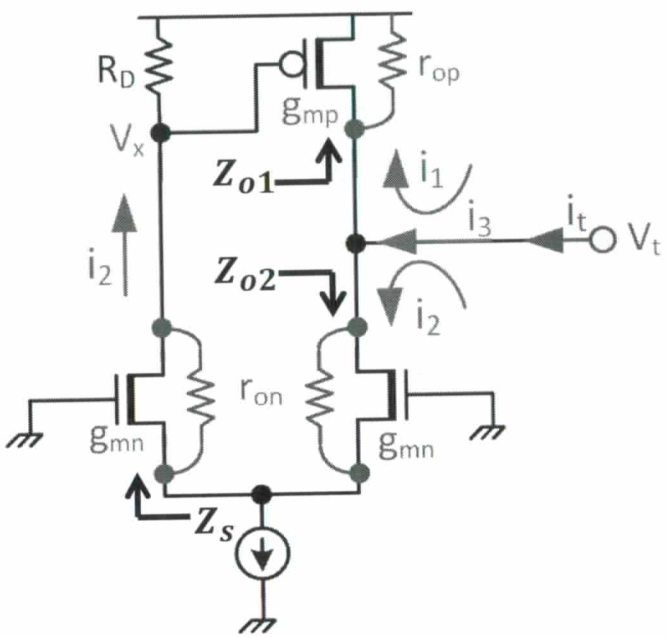
$R_{L1} \neq R_{L2}$

(But $R_{L1} \ll r_{on}$, $R_{L2} \ll r_{on}$)

$Z_{X1} \approx Z_{X2} \approx \frac{1}{g_m}$

$\Rightarrow$ can apply virtual ground at node-X

Active-Load Output Impedance Calculation (1)



- ❑ Assume that $R_D \ll r_{on} \Rightarrow z_s = \frac{1}{g_{mn}} \Rightarrow z_{o2} = \frac{v_t}{i_2} = 2r_{on}$
- ❑ $z_{o1} = \frac{v_t}{i_1} = r_{op}$
- ❑ There is another current component in the output due to active loading: PMOS will sense V_x and create i_3.

$$i_3 = g_{mp} v_x = i_2 \times g_{mp} R_D$$

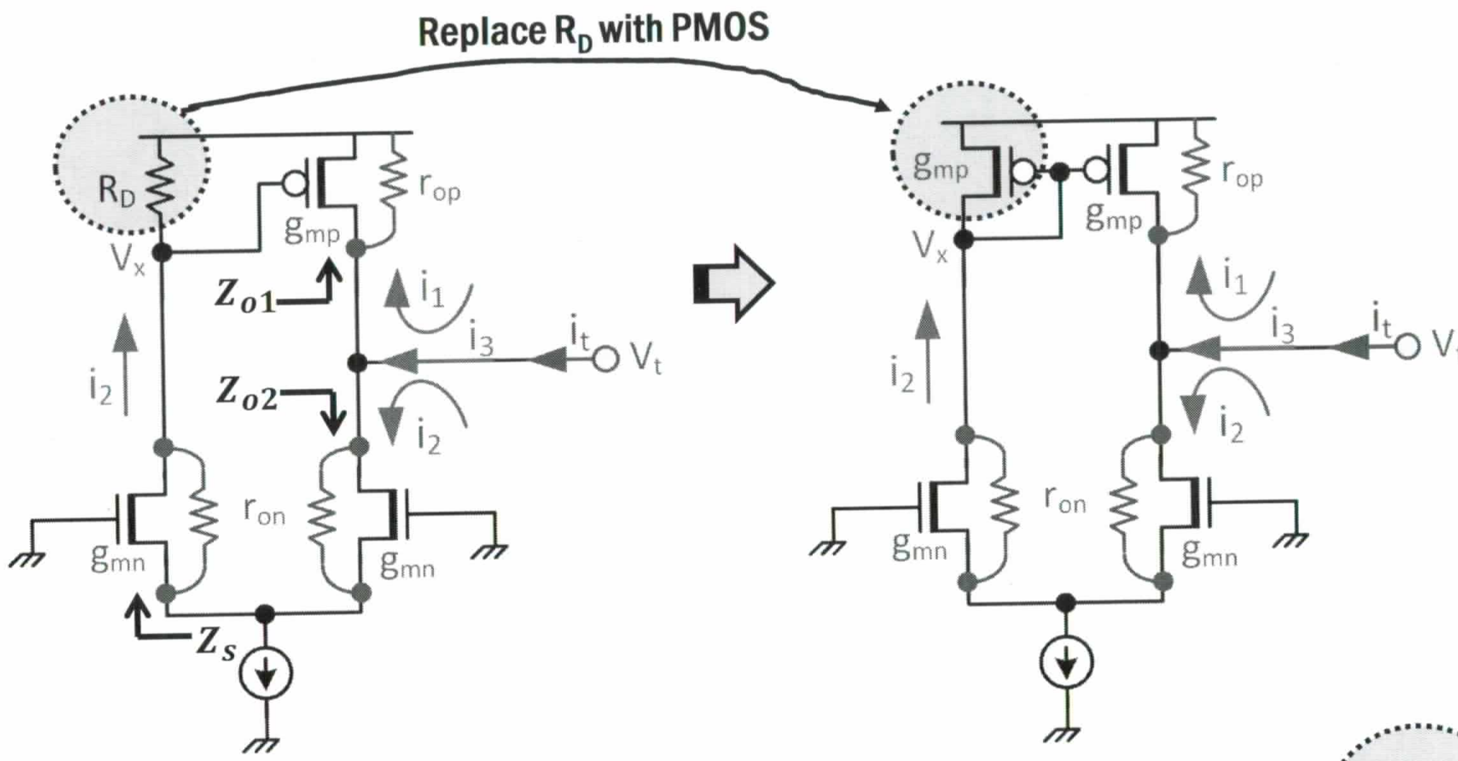
$$\therefore \textit{total current } i_t = i_1 + i_2 + i_3 = i_1 + i_2(1 + g_{mp}R_D)$$

$$\Rightarrow Y_{out} = \frac{i_t}{v_t} = \frac{i_1 + i_2(1 + g_{mp}R_D)}{v_t} = \frac{1}{z_{o1}} + \frac{1}{z_{o2}}(1 + g_{mp}R_D)$$

$$\Rightarrow Z_{out} = \frac{1}{Y_{out}} = Z_{o1} \parallel \frac{Z_{o2}}{(1 + g_{mp}R_D)} = r_{op} \parallel \frac{2r_{on}}{(1 + g_{mp}R_D)}$$

Note: z_{o2} is divided by $(1 + g_{mp}R_D)$ due to active loading effect.

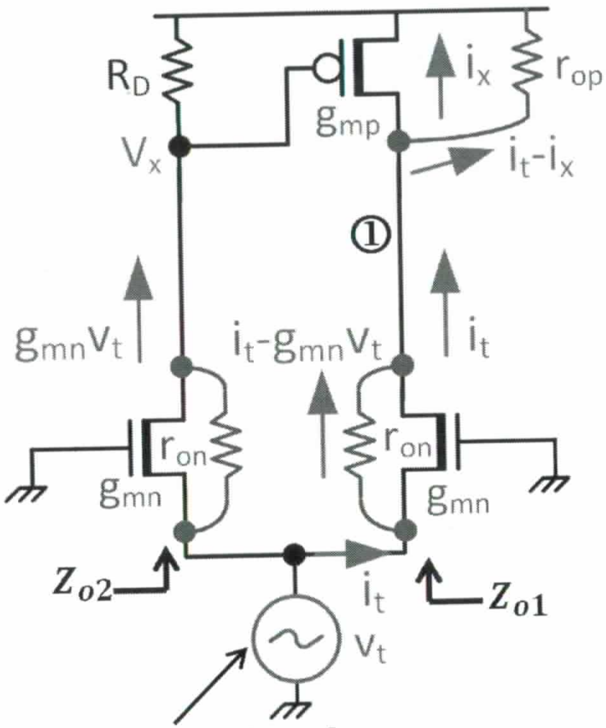
Active-Load Output Impedance Calculation (2)



$$Z_{out} = Z_{o1} \parallel \frac{Z_{o2}}{(1 + g_{mp}R_D)} = r_{op} \parallel \frac{2r_{on}}{(1 + g_{mp}R_D)}$$

$$Z_{out} = r_{op} \parallel \frac{2r_{on}}{\left(1 + g_{mp}\frac{1}{g_{mp}}\right)} = r_{op} \parallel r_{on}$$

Active-Load Source-side Impedance Calculation (1)



❑ Assume that $R_D \ll r_{on} \Rightarrow z_{o2} = \dfrac{1}{g_{mn}}$

$$i_x = g_{mp}v_x = g_{mn}g_{mp}R_Dv_t$$

$$\Rightarrow v_{①} = (i_t - i_x)r_{op} = i_t(1 - g_{mn}g_{mp}R_Dv_t)r_{op}$$

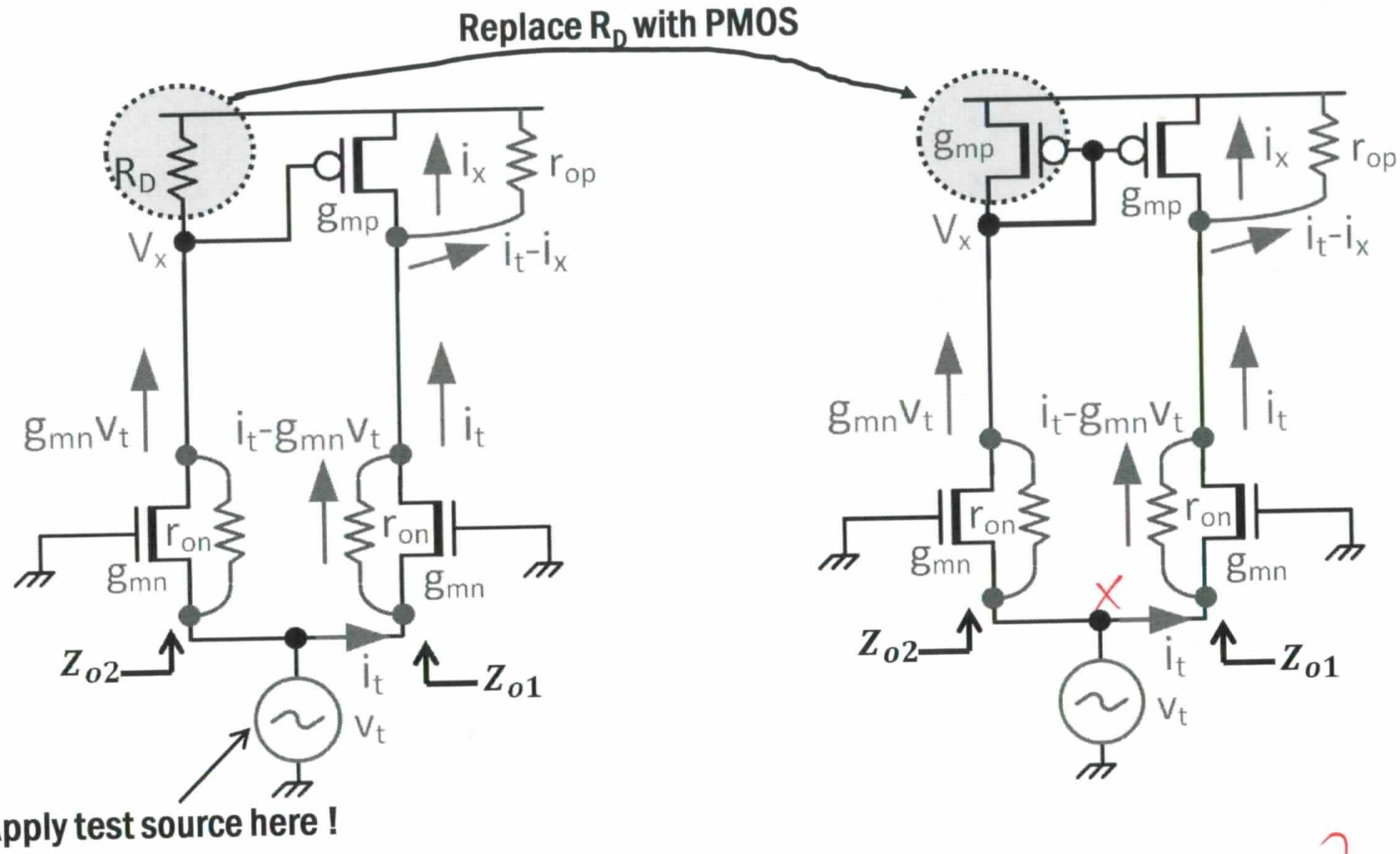
$$\Rightarrow v_t = v_{①} + (i_t - g_{mn}v_t)r_{on} = i_t(r_{on} + r_{op}) - (g_{mn}g_{mp}R_Dr_{op} + g_{mn}r_{on})v_t$$

$$\Rightarrow Z_{o1} = \frac{v_t}{i_t} = \frac{r_{on} + r_{op}}{1 + (g_{mn}g_{mp}R_Dr_{op} + g_{mn}r_{on})}$$

$$\approx \frac{1}{g_{mn}}\frac{r_{on}+r_{op}}{r_{on}+g_{mp}R_Dr_{op}}$$

This is a little bit involved expression. But most cases of active-loading, they use PMOS rather than R_D, which will simplify the expression (see next page).

Active-Load Source-side Impedance Calculation (2)



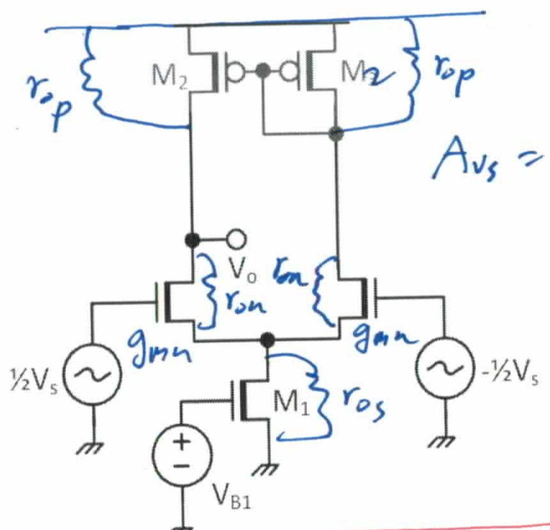
- $Z_{o1} = \frac{v_t}{i_t} \approx \frac{1}{g_{mn}} \frac{r_{on}+r_{op}}{r_{on}+g_{mp}R_D r_{op}}$
- $Z_{o2} = \frac{1}{g_{mn}}$

- $Z_{o1} = \frac{v_t}{i_t} \approx \frac{1}{g_{mn}}$
- $Z_{o2} = \frac{1}{g_{mn}}$

} can apply virtual ground at node X

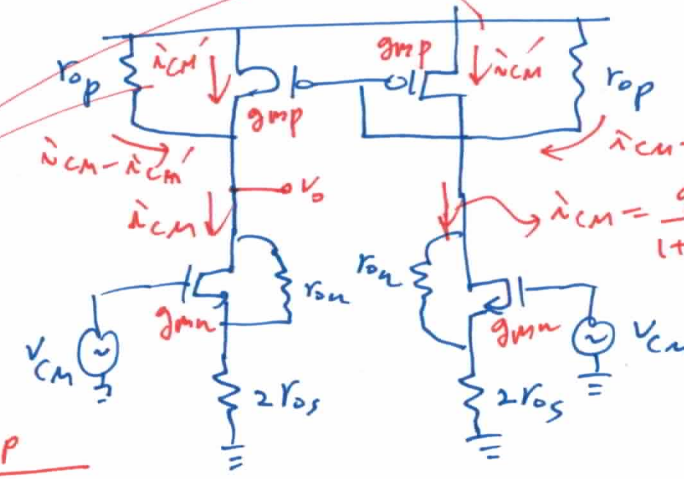
Common-Mode Rejection Ratio (CMRR)

Differential-mode



$A_{vs} = \frac{v_o}{v_s} = g_{mn}(r_{on} \| r_{op})$

Common-mode



$i_{cm} = \frac{g_{mn}}{1+2g_{mn}r_{os}} v_{cm}$

$$CMRR = \frac{A_{vs}}{A_{v,cm}} = g_{mn}(r_{on} \| r_{op})(2g_{mp}r_{os})$$

$$i_{cm}' = i_{cm} \cdot \frac{r_{op}}{\frac{1}{g_{mp}} + r_{op}} = i_{cm} \frac{g_{mp}r_{op}}{1+g_{mp}r_{op}}$$

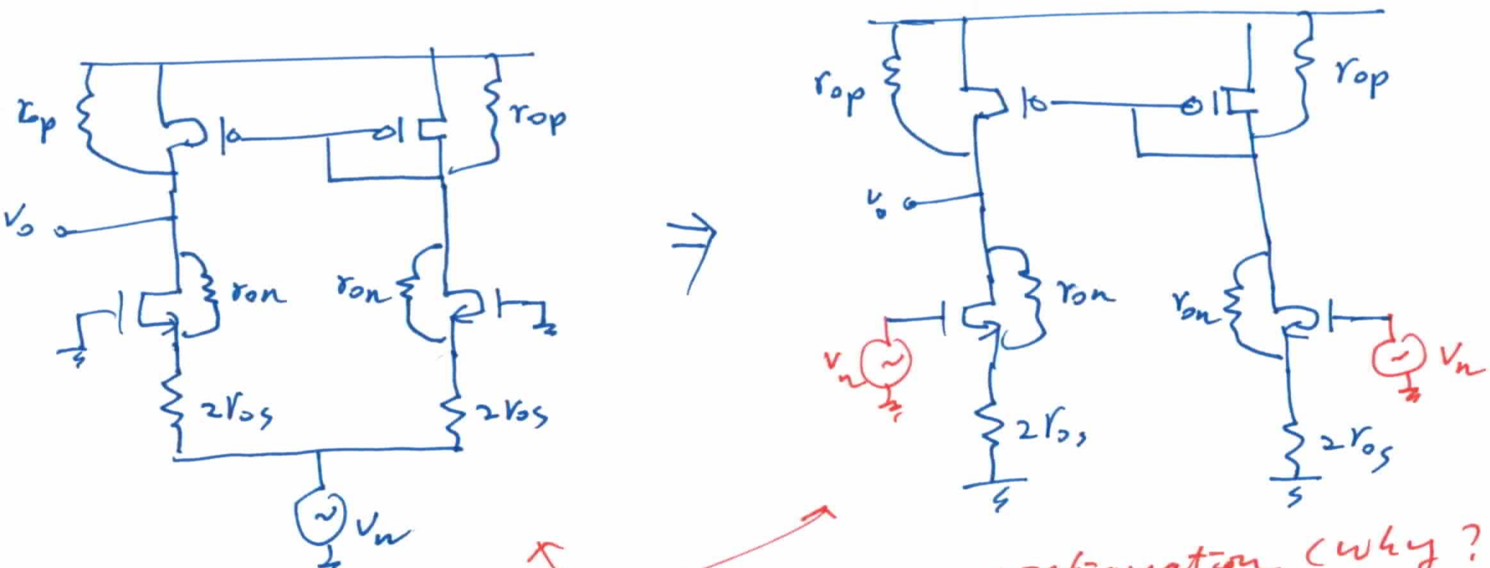
$$\therefore i_L = i_{cm} - i_{cm}' = i_{cm}\left(1 - \frac{g_{mp}r_{op}}{1+g_{mp}r_{op}}\right) = \frac{i_{cm}}{1+g_{mp}r_{op}}$$

$$v_{o,cm} = i_L \times r_{op} = \frac{r_{op}}{1+g_{mp}r_{op}} \cdot i_{cm} = \frac{r_{op}}{1+g_{mp}r_{op}} \frac{g_{mn}}{1+2g_{mn}r_{os}} v_{cm}$$

$$\Rightarrow A_{v,cm} = \frac{v_{o,cm}}{v_{cm}} = \frac{g_{mn}r_{op}}{(1+g_{mp}r_{op})(1+2g_{mn}r_{os})} \simeq \frac{1}{2g_{mp}r_{os}}$$

Power Supply Rejection Ratio (PSRR)

Ground supply rejection ratio (GSRR) = PSRR−



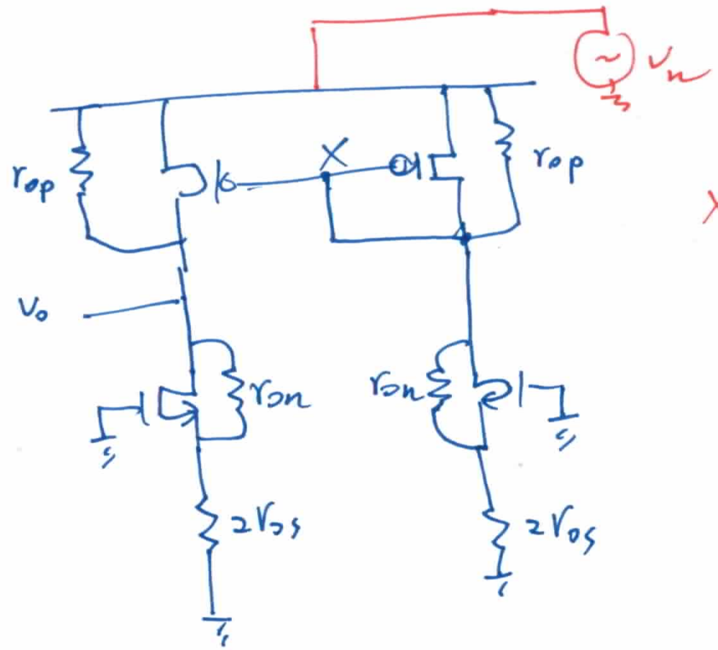
They are same configuration (why?)

∴ GSRR (PSRR−) = CMRR

Power Supply Rejection Ratio (PSRR)

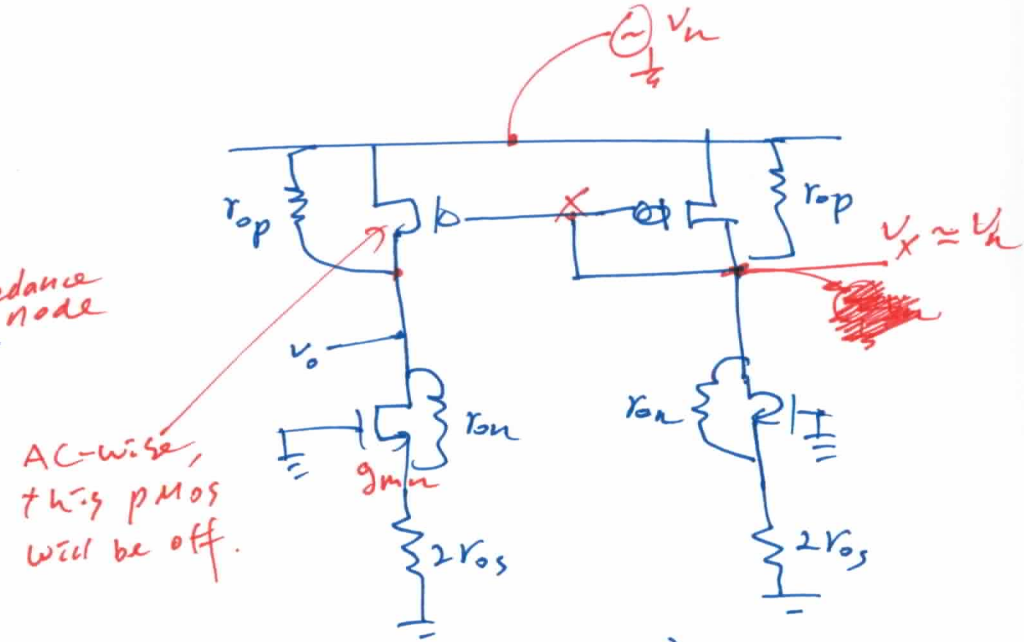
(13)

power supply rejection Ratio (PSRR +)



X ⇒ low impedance node

⟹



$$\therefore \frac{v_o}{v_n} = \frac{r_{on}(1+g_{mn}\cdot 2r_{os})}{r_{op} + r_{on}(1+g_{mn}\cdot 2r_{os})} \approx 1$$

$$PSRR+ = \frac{\text{differential-mode signal gain}}{\left(\frac{v_o}{v_n}\right)} = \frac{A_{vs}}{\left(\frac{v_o}{v_n}\right)} = A_{vs} = g_{mn}(r_{on} \| r_{op})$$

→ larger gain, better suppression of supply noise