# ECE4220 Class Project #3

Due Date: Dec. 4th (by class time)

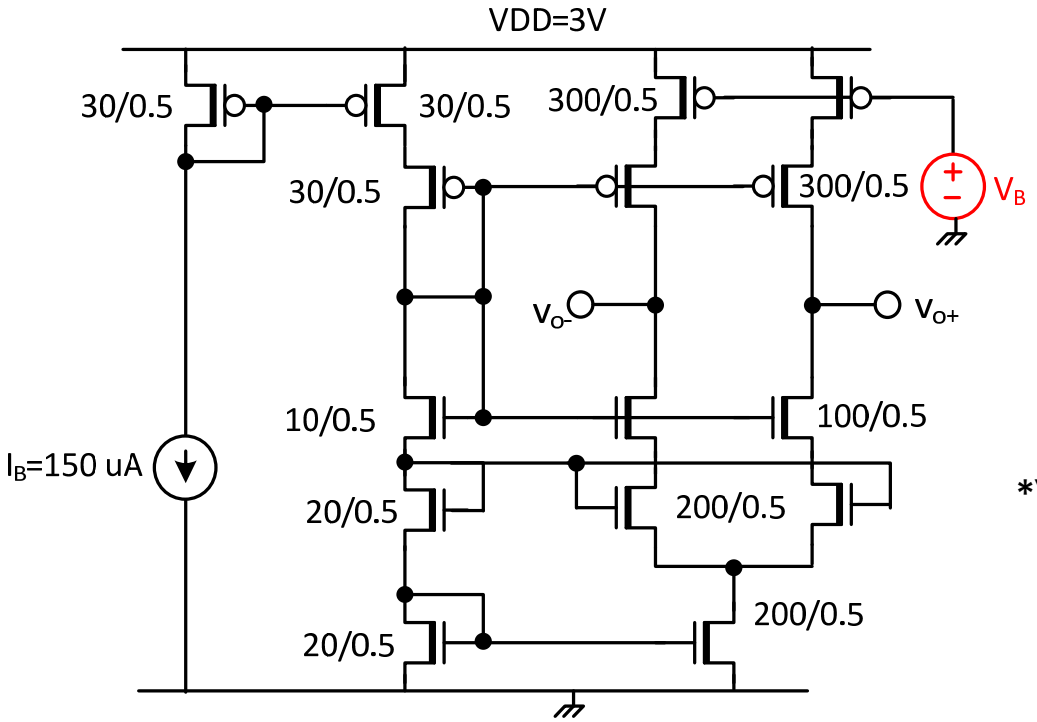
Full Credit: 100-pt

Instructor: Dr. Kwang-Jin Koh

ECE Dept. Virginia Tech

Email: kkoh@vt.edu

# Common-Mode Feedback Design (1)

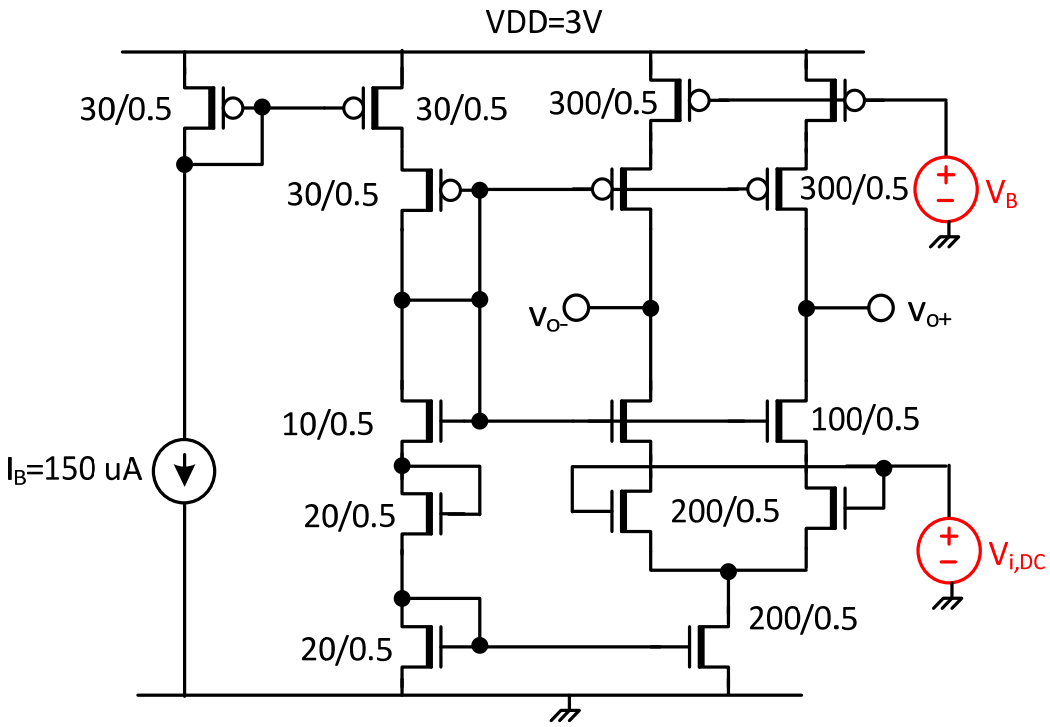



Configure a cascode differential amplifier schematic as shown. Use ideal current source for $I_B$ (note: in real design , $I_B$ will be generated by a bandgap reference typically).

- Q-1) Sweep $V_B$ and find the range of $V_B$ where all the transistors can operate in saturation mode (5 pt).

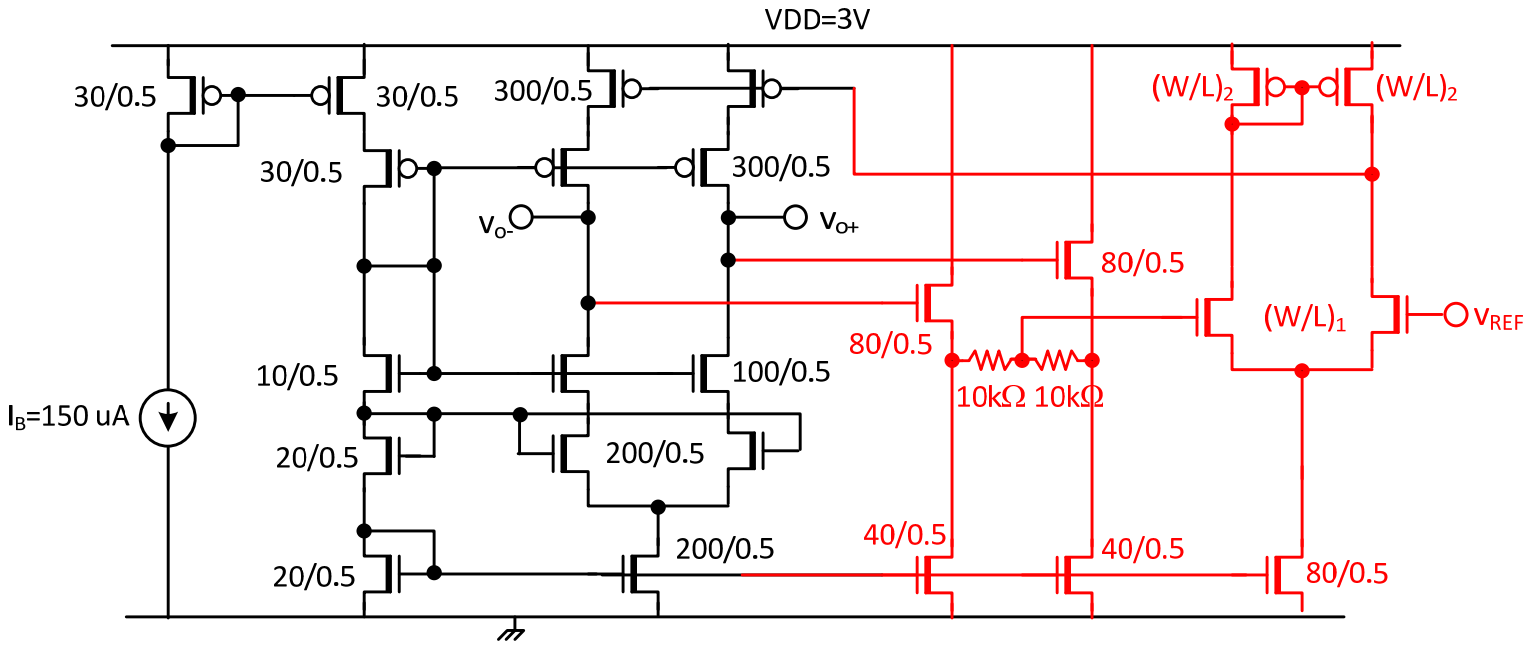
*You should observe how sensitive of node bias points to $V_B$.

# Common-Mode Feedback Design (2)



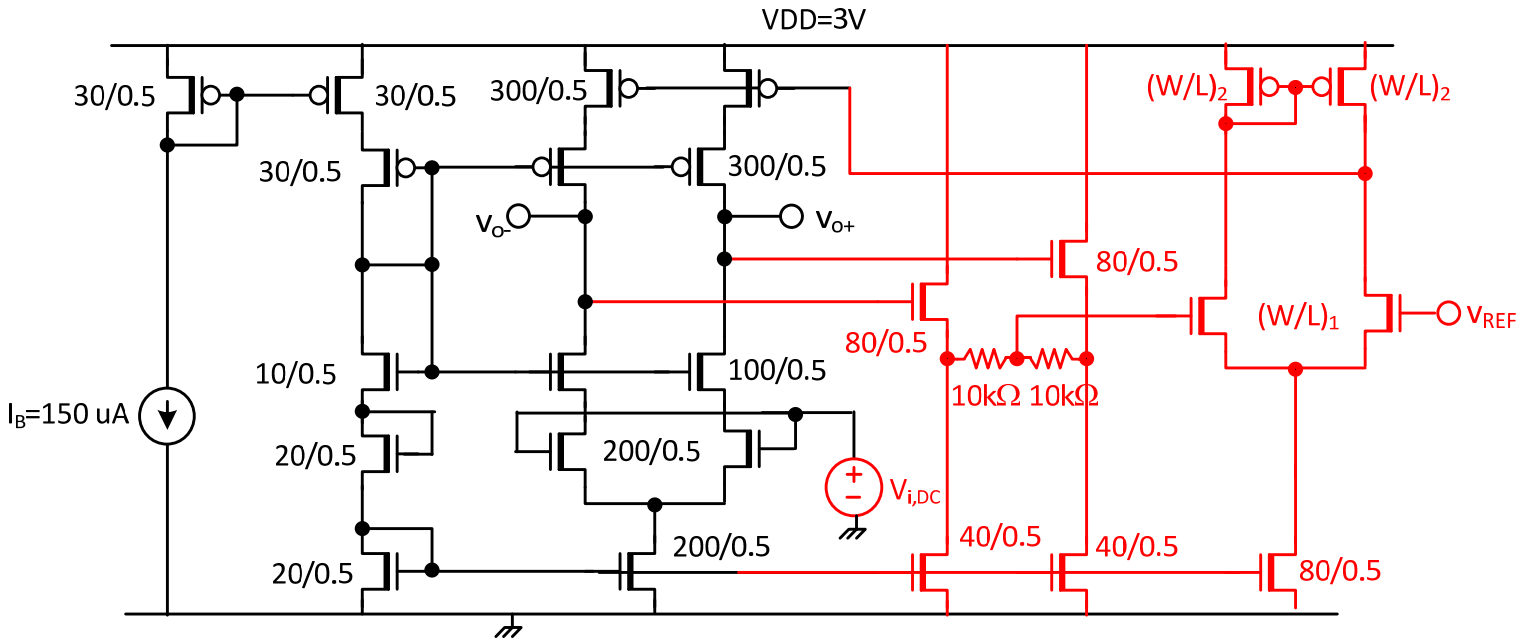

- Q-2) Set $V_B$ to a specific value within the range you determine in Q-1. Then apply common-mode input DC, $V_{i,DC}$, and sweep it. What's the common-mode input DC range where all the transistors can operate in saturation mode (5pt).

# Common-Mode Feedback Design (3)



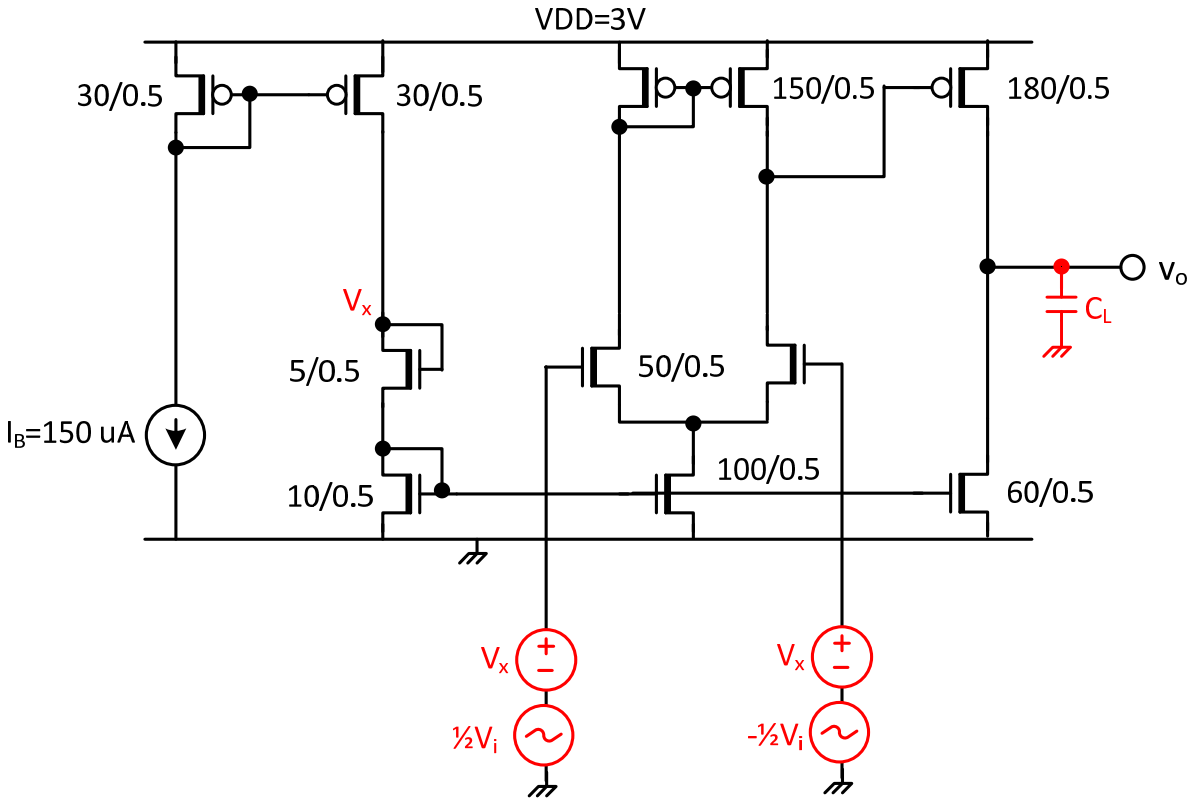

- Q-3) Now, let's design common-mode DC feedback circuits. Set the size of $(W/L)_1$ and $(W/L)_2$ and determine range of $V_{REF}$ so that all transistors can operate in saturation mode (10 pt).

# Common-Mode Feedback Design (4)




- Q-4) let's set $V_{REF}$ to a specific value which is within the range you determined in Q-3. Sweep $V_{i,DC}$ a nd determine input common-mode range and output common-mode range. Do you observe any di fferent result from that of Q-2? If yes, why? (10 pt).

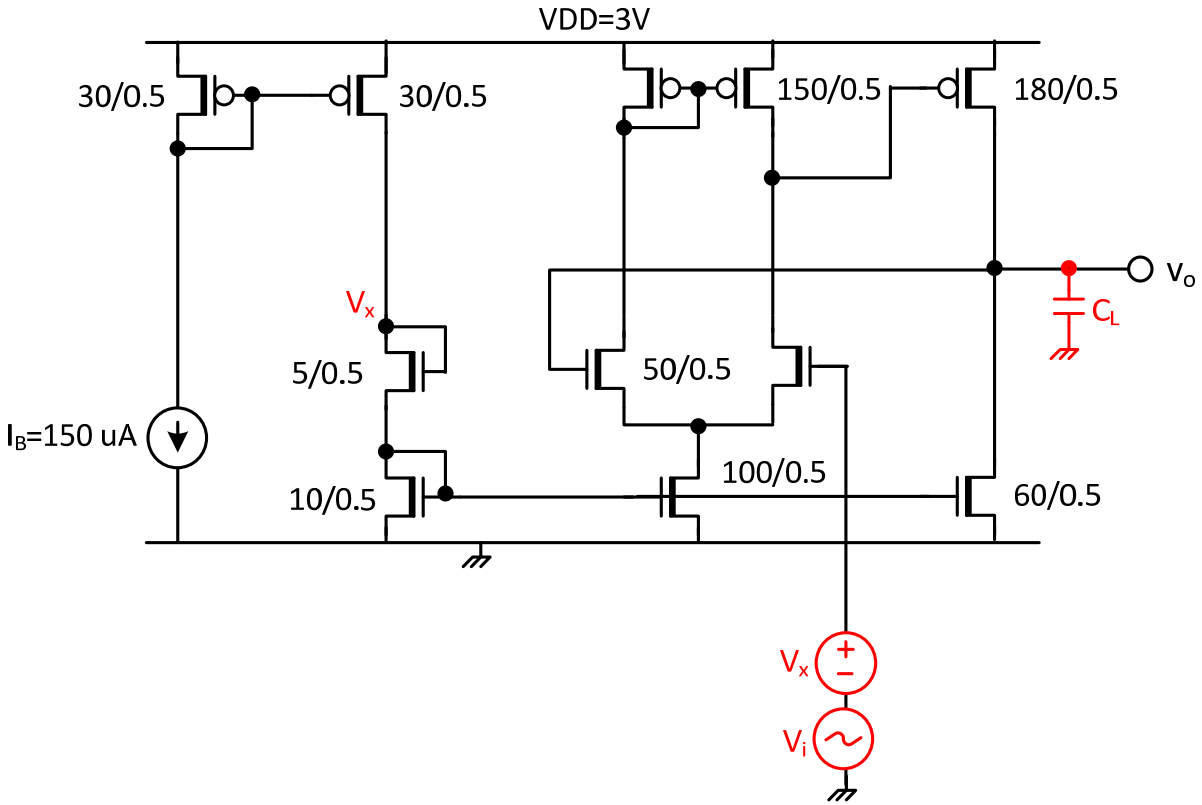
# Uncompensated 2-stage OP-Amp (1)




- Q-5) Let's design 2-stage op-amp, and set $C_L$=1 pF. Calculate and simulate voltage gain ($A_v = \frac{V_o}{V_i}$) (5 pt).

- Q-6) Calculate dominant pole frequency ( $\omega_{p1}$), second pole frequency ($\omega_{p2}$) and do minant positive zero frequency ($\omega_z$). Compa re your calculations with simulations (5 pt).

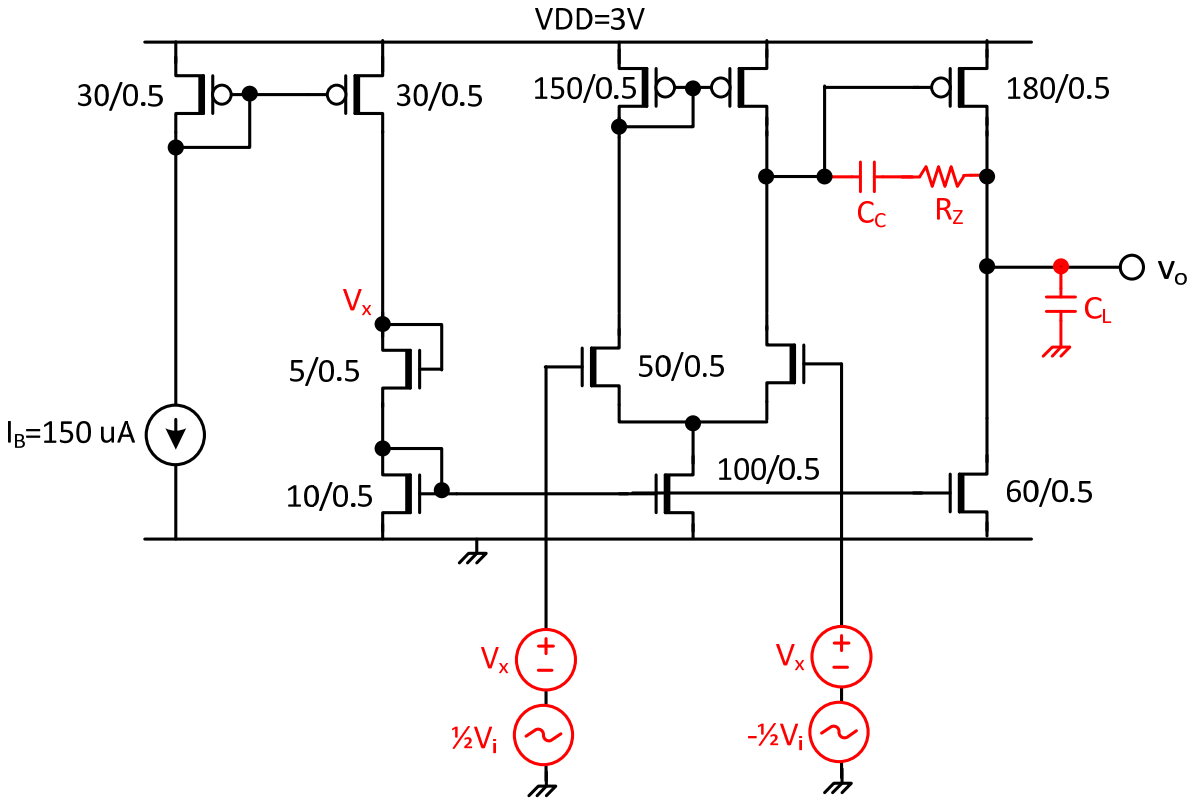
# Uncompensated 2-stage OP-Amp (2)




Now, let's assume that you are applying unity feedback as shown in the figure. Note that unity feedback is the worst case feedback when you consider stability. And you should design stability (i.e., compensate op-amp) to guarantee > 60-deg of phase margin in this worst case feedback.

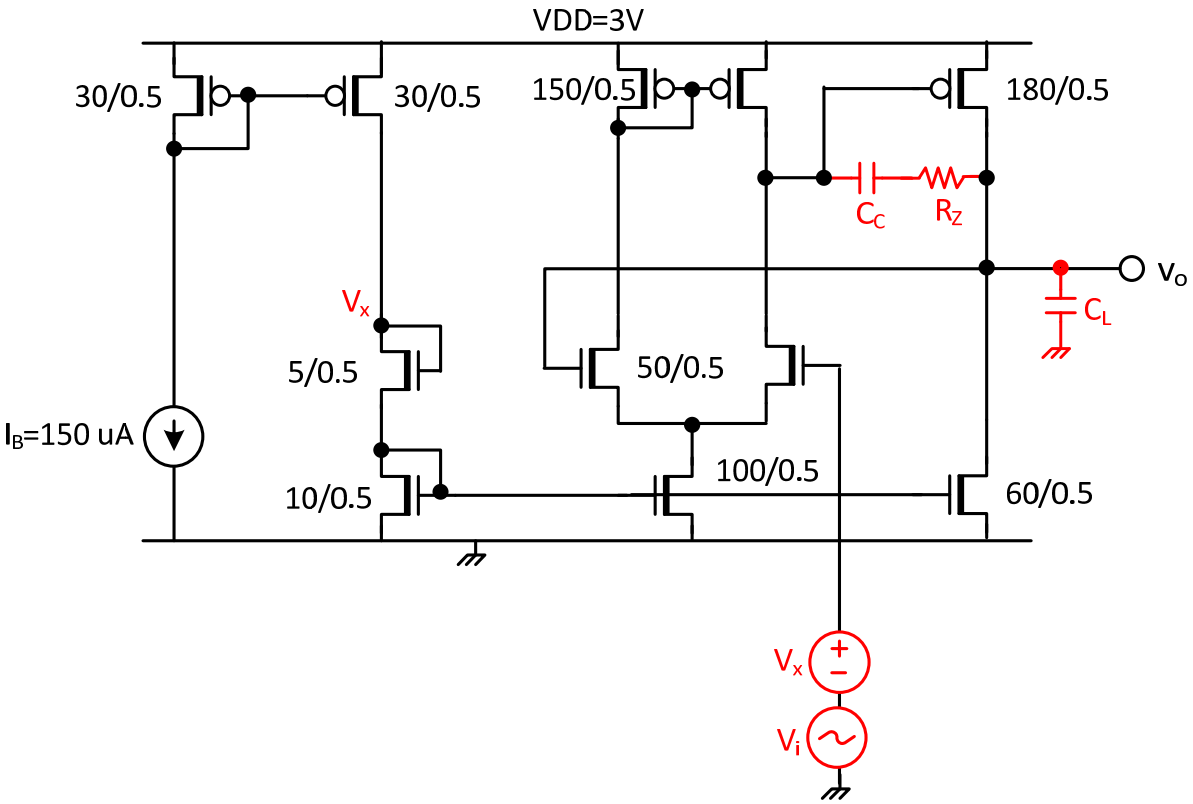
- Q-7) Simulate voltage gain ($A_v = \frac{V_o}{V_i}$).
  Do you observe any peaking in the $A_v$? If yes, why ? Simulate loop-gain (T) and phase margin ($\emptyset_M$) (10 pt).

# OP-Amp Frequency Compensation (1)



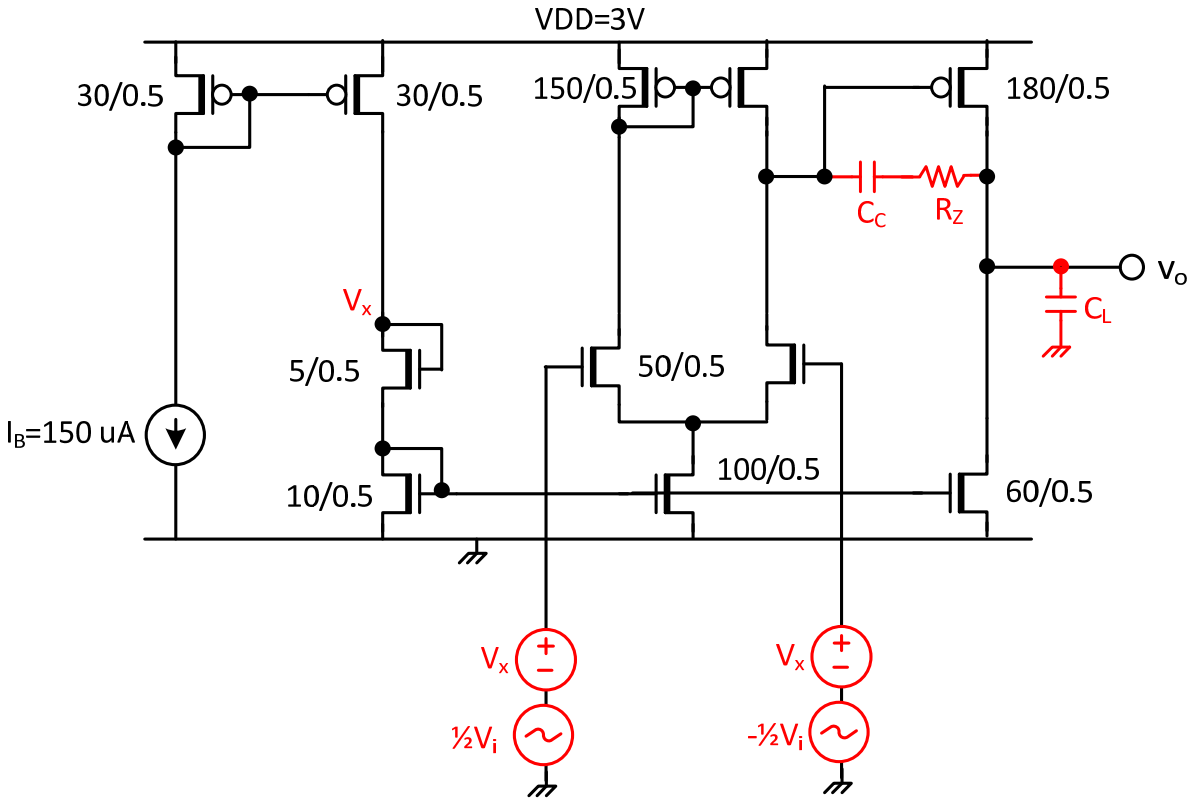

- Q-8) Determine (Calculate) $C_C$ and $R_Z$ so that $\emptyset_M$~45 deg. Calculate dominant pole ($\omega_{p1}$), second pole ($\omega_{p2}$) and dominant zero ($\omega_z$). What's the unity gain frequency ($\omega_u$)? Verify your calculation through simulation (20 pt).

# OP-Amp Frequency Compensation (2)



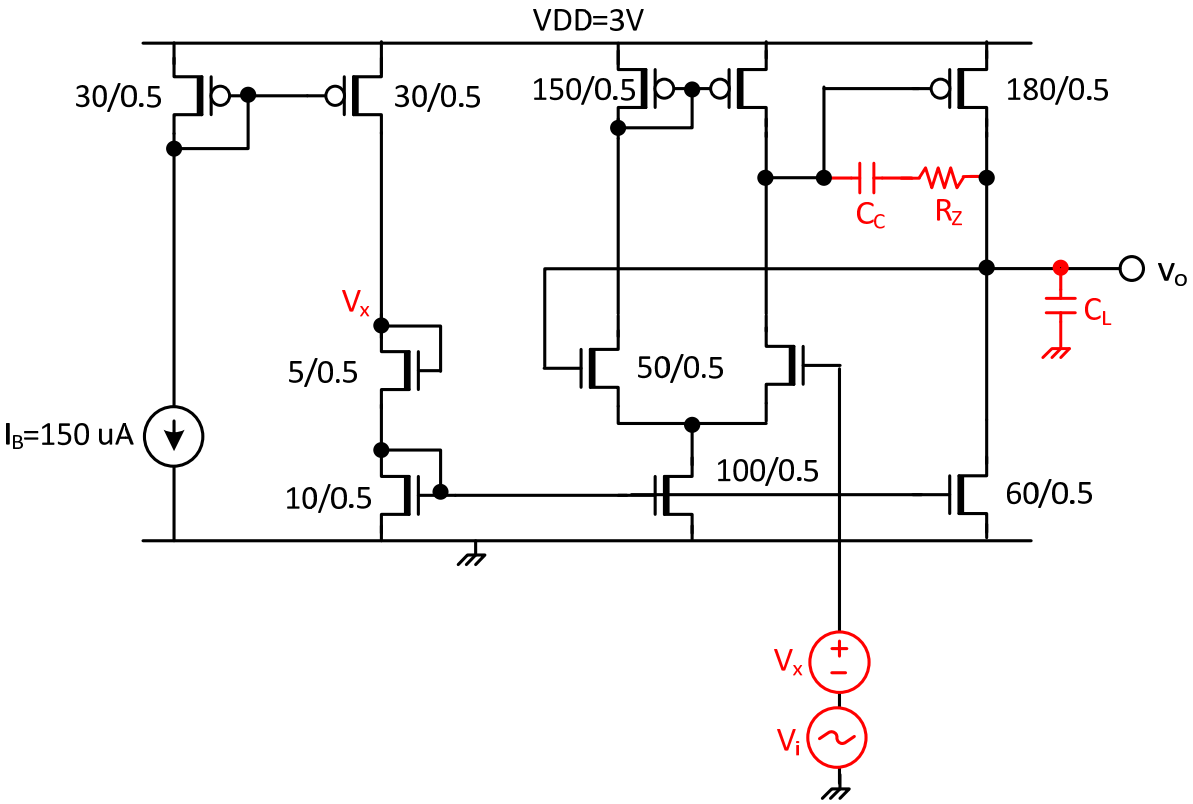

- Q-9) Set $C_C$ and $R_Z$ as in Q-7, and then apply unity feedback. Simulate voltage gain ( $A_v = \frac{V_o}{V_i}$). Do you observe any peaking in the $A_v$? (5 pt).

# OP-Amp Frequency Compensation (3)




- Q-10) Determine (Calculate) $C_C$ and $R_Z$ so that $\emptyset_M$~80 deg. Calculate dominant pole ($\omega_{p1}$), second pole ($\omega_{p2}$) and dominant zero ($\omega_z$). What's the unity gain frequency ($\omega_u$)? Verify your calculation through simulation (10 pt).

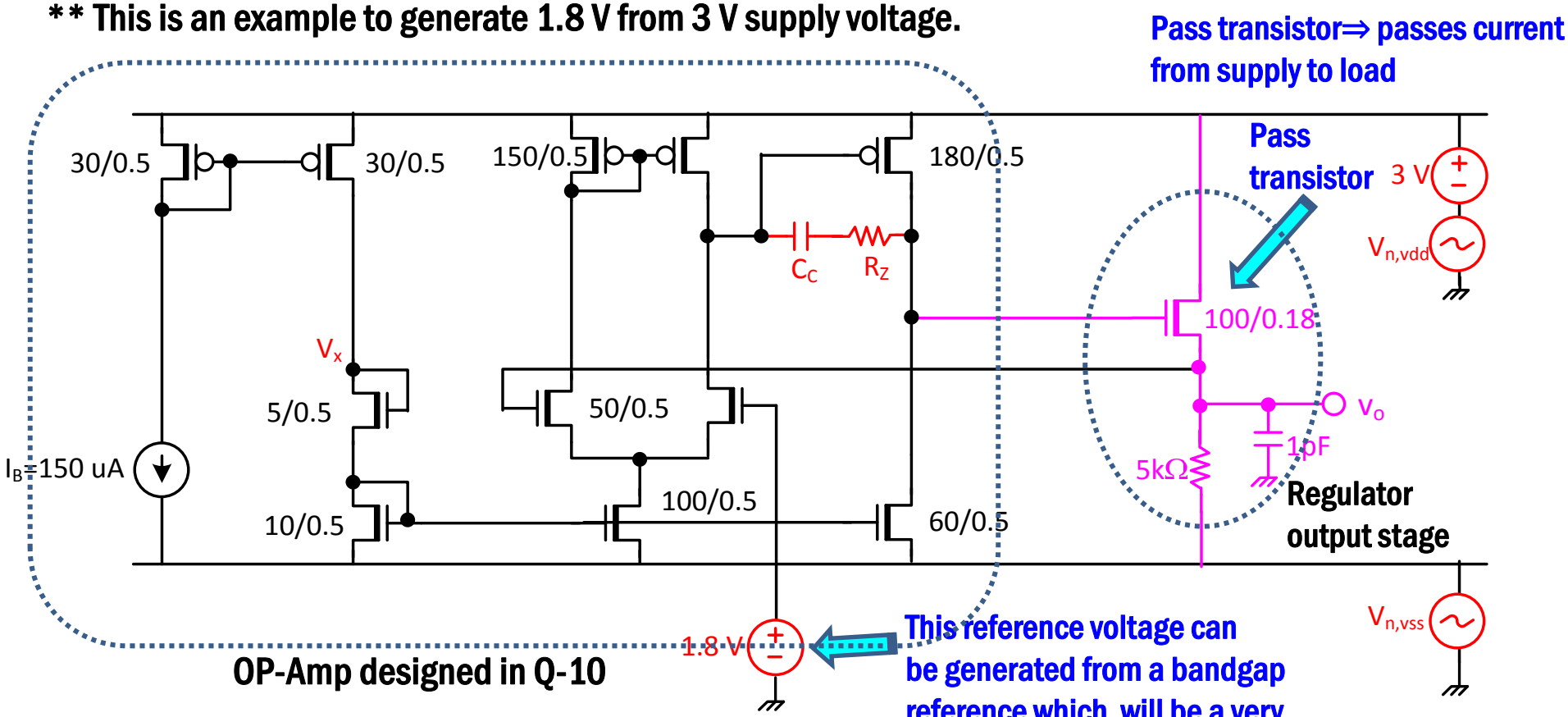
# OP-Amp Frequency Compensation (4)




- Q-11) Set $C_C$ and $R_Z$ as in Q-8, and then appl y unity feedback. Simulate voltage gain ( $A_v = \frac{V_o}{V_i}$). Do you observe any peaking in the $A_v$? (5 pt).

# OP-Amp Application: Linear Regulator (1)

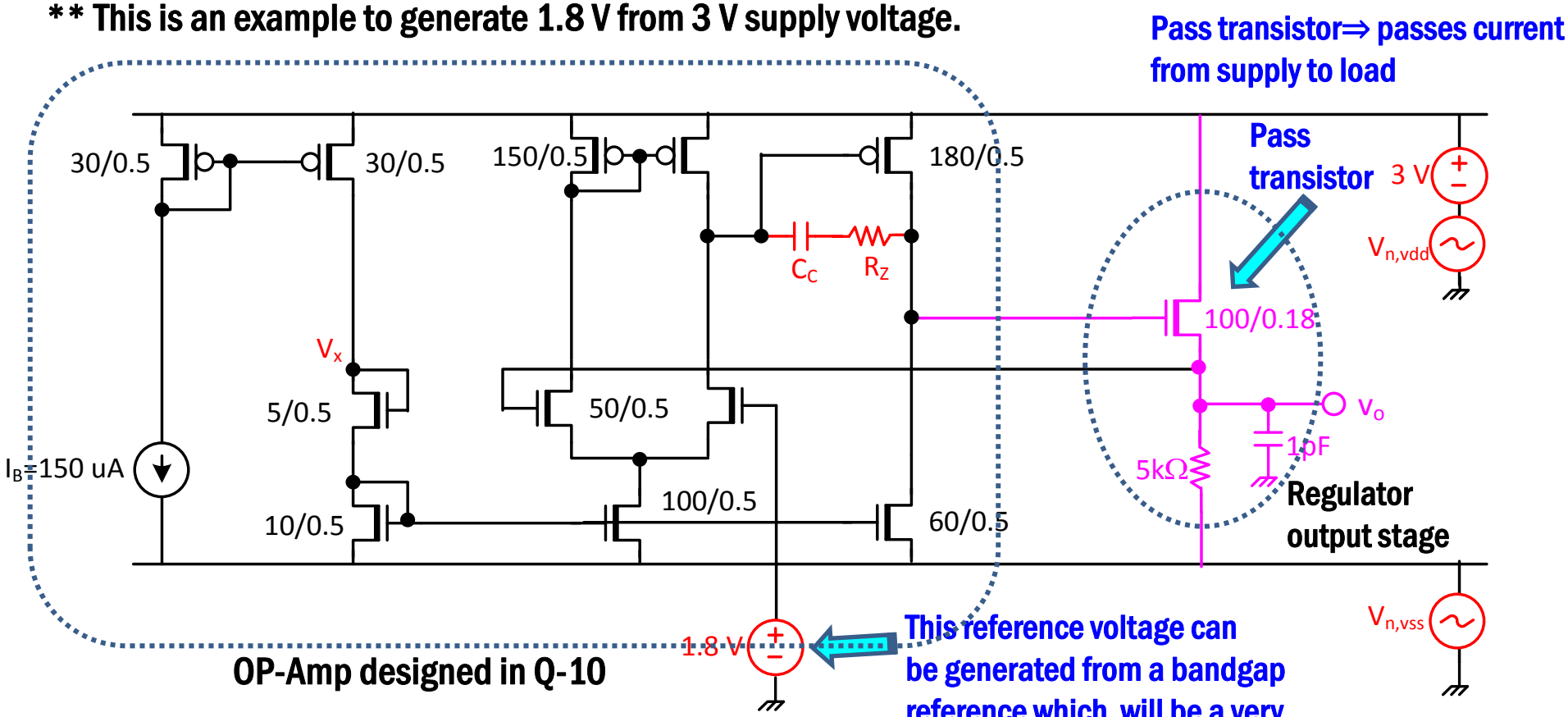
** This is an example to generate 1.8 V from 3 V supply voltage.




Note: $V_{n,vdd}$ and $V_{n,vss}$ could represent a low-frequency supply noise and ground noise, respectively. You should observe that these low-frequency noise will be suppressed by the feedback loop-gain in the simulation. ⇒ Alternatively speaking, VDD and GND will be **regulated** by the feedback loop.

# OP-Amp Application: Linear Regulator (2)

** This is an example to generate 1.8 V from 3 V supply voltage.




- Q-12) Set $V_{n,vss}$=0 and simulate voltage gain, $A_{v,nvdd} = \frac{V_o}{V_{n,vdd}}$ (Note: $1/A_{v,nvdd}$ is PSRR+ ) (5 pt).
- Q-13) Set $V_{n,vdd}$=0 and simulate voltage gain, $A_{v,nvss} = \frac{V_o}{V_{n,vss}}$ (Note: $1/A_{v,nvss}$ is PSRR- ) (5 pt).