ECE4220 Class Project #2

Due Date: Nov. 8th (by class time)

Full Credit: 100-pt

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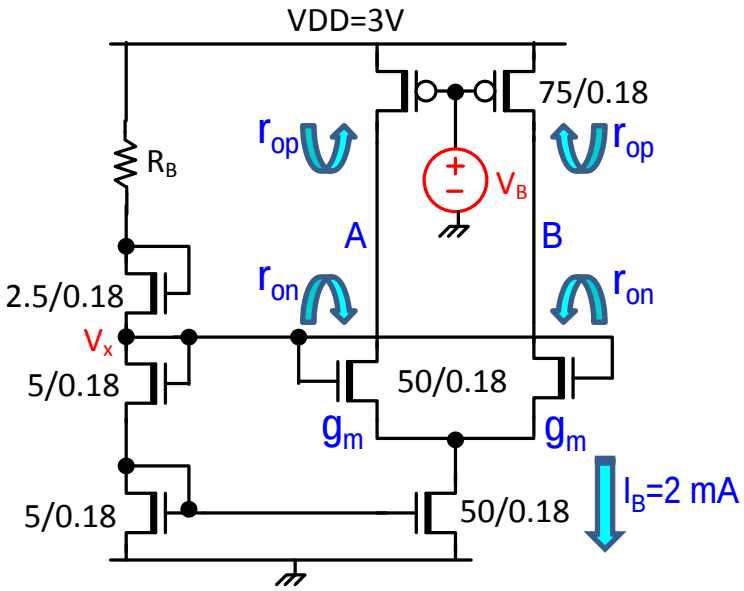
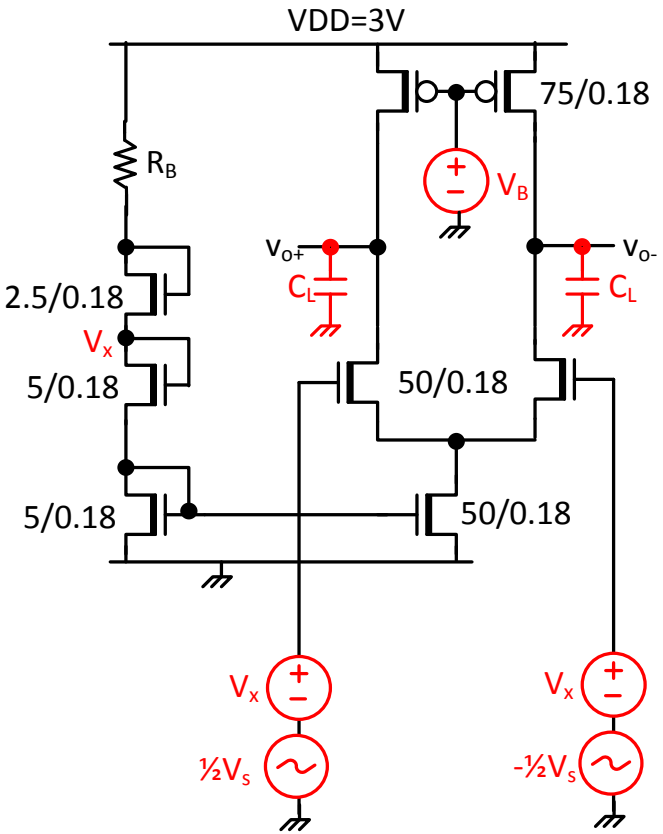
Differential Amplifier Design (1)



Use Jazz 0.18-μm CMOS devices, model "nfet" and "pfet" for active transistors. For all passive components, you can use ideal model in "analoglib". Set NMOS and PMOS sizes as shown in the figure.

- Q-1) Through DC simulation, set R_B and V_B so that total bias current in the differential paths is 2 mA (1mA per each path) and all the transistors can operate in saturation mode (10 pt).
- Q-2) Once you set an appropriate V_B, you can check all small signal parameters out (basically the simulator will display the small signal parameters). What are the output impedance of NMOS (r_{on}) and PMOS (r_{op})? What is g_m of NMOS? (5 pt)
- Q-3) From Q-1 you can notice that DC voltage of drain nodes of NMOS and PMOS (node-A and mode-B) will be very sensitive to V_B. Explain the reason why (5 pt).

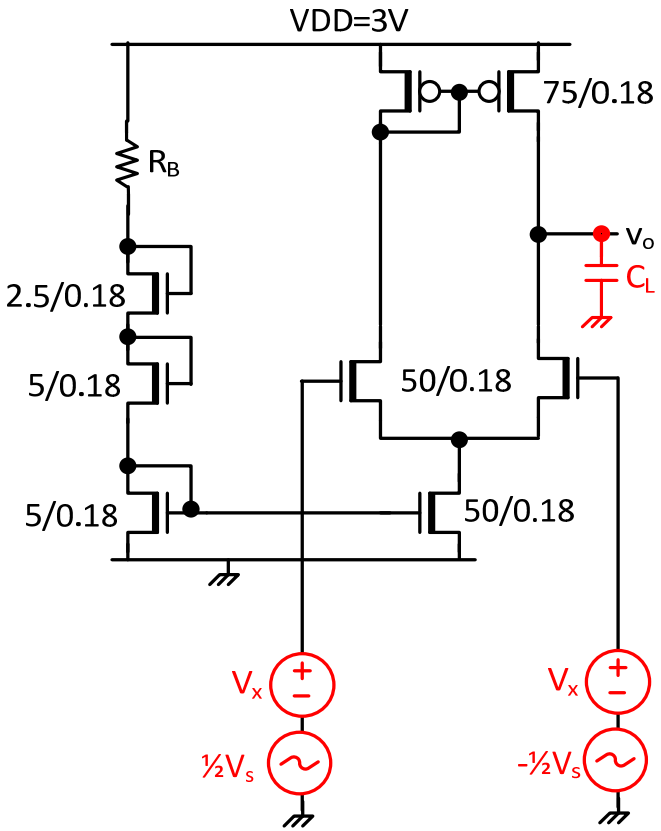
Differential Amplifier Design (2)



Use bias voltages you set in the previous step (Step-(1)), and apply DC bias voltages to NMOS and PMOS as shown in the figure below (V_x and V_B to NMOS and PMOS, respectively). Set C_L as C_L=10 pF (note: C_L could represent a loading capacitance from next stage).

- Q-4) Apply input signal ($\pm\frac{1}{2}V_s$) using "vsin" source, and plot output differential gain ($A_v = \frac{V_{o+}-V_{o-}}{V_s}$) versus frequency in dB-scale (5 pt).
- Q-5) Estimate the differential gain based on small signal parameters (r_{on}, r_{op} and g_m) you find in the DC simulation in Step-(1) , and compare the simulation result in Q-4 with your estimation (5 pt).
- Q-6) From the result in Q-4, you can confirm that the differential amplifier is one-pole system. Calculate the pole frequency (3-dB BW) based on small signal parameters and compare your calculation with the simulation result (5 pt).
  Note: After DC simulation in Step-(1), you can identify all the small signal parameters including parasitic capacitances (C_{gs} and C_{gd}).

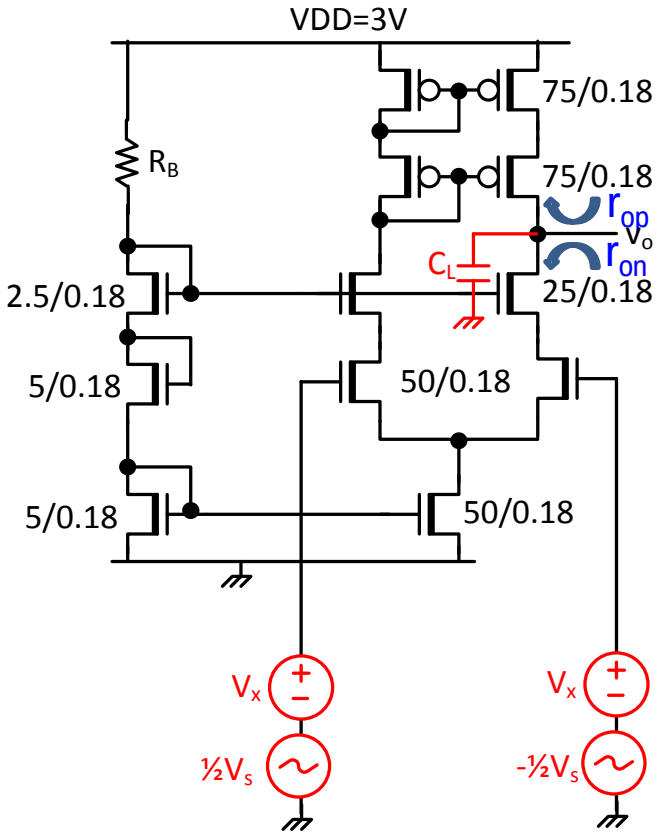
Differential Amplifier Design (3)



Now, let's change the topology as shown below. Set C_L as C_L=10 pF (note: C_L could represent a loading capacitance from next stage).

- Q-7) Apply input signal ($\pm\frac{1}{2}V_s$) using "vsin" source, and plot output gain ($A_v = \frac{V_o}{V_s}$) versus frequency in dB-scale . While single-ended output, gain should be about the same as in Q-4, and explain why? (5 pt).
- Q-8) From the result in Q-7, you should observe that this amplifier is second-order system (2-poles and 1-zero). Calculate the dominant , non-dominant poles and zero frequencies. Compare your calculations with the simulation results (20 pt).
  Hint: You can approximate that each node contribute a pole ("one-pole one-node" approximation).

Differential Amplifier Design (4)

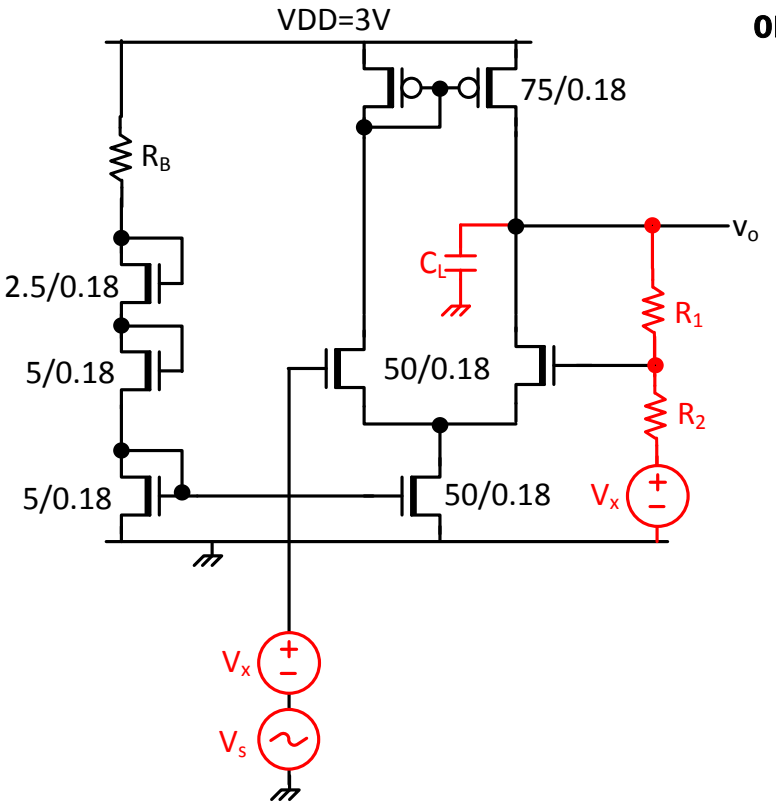


Let's cascoding NMOS and PMOS. You might need to tweak R_B slightly from previous value so that the differential amplifier has the same bias current of 2 mA total. Set C_L as C_L=10 pF (note: C_L could represent a loading capacitance from next stage).

- Q-9) Apply input signal ($\pm\frac{1}{2}V_s$) using "vsin" source, and plot output gain ($A_v = \frac{V_o}{V_s}$) versus frequency in dB-scale (5 pt).

- Q-10) Calculate r_{on}, r_{op} and output resistance $r_{on} \parallel r_{op}$. Calculate output gain and compare your calculation with the simulated result (15 pt).

Differential Amplifier Design (5)



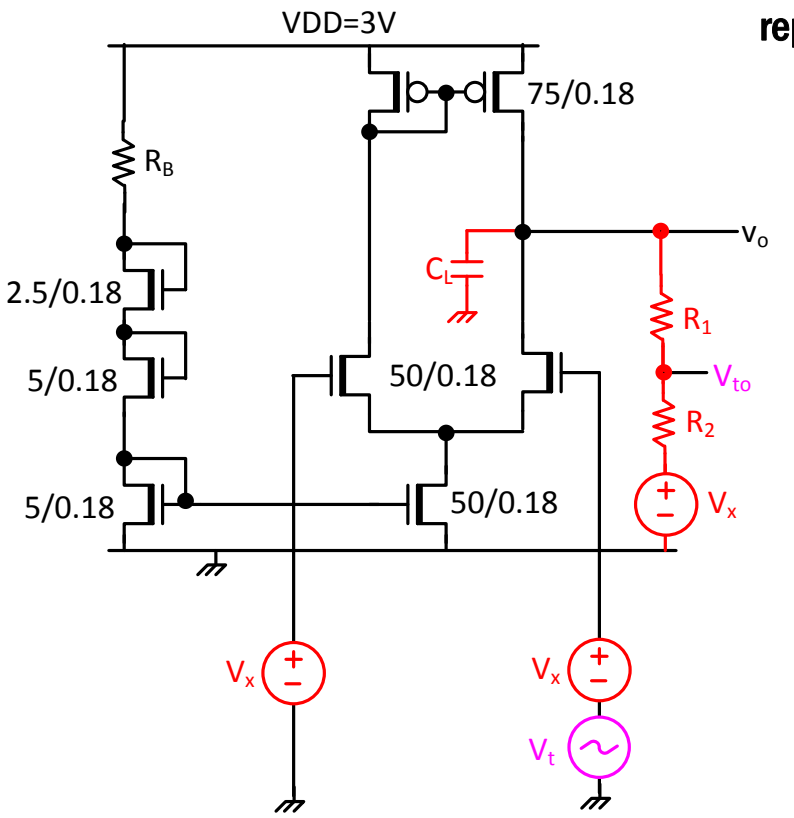
Use the same DC conditions as in Step-(3), and apply feedback resistors, R_1 and R_2. Set C_L as C_L=10 pF (note: C_L could represent a loading capacitance fr om next stage).

- Q-11) Use virtual grounding concept and calculate R_1 and R_2 so that the gain ($A_v = \frac{V_o}{V_s} = \frac{1}{f}$) can be 6 dB (5 pt).

- Q-12) Simulate your design and plot gain curve versus frequency (5 p t).

Note: your simulated gain might be smaller than the target 6dB (why?)

Differential Amplifier Design (6)



Use the same DC conditions as in Step-(3), and set feedback resistors, R_1 an d R_2, as you designed in the previous step. Set C_L as C_L=10 pF (note: C_L could represent a loading capacitance from next stage).

- Q-13) Calculate and simulate feedback loop gain ($T = \frac{V_{to}}{V_t}$) (10 pt).

Note: Your loop gain (T) might not be large enough in this design, and there could be some error in the overall closed-loop gain $(= \frac{1}{f})$ which is calculated based on virtual grounding technique. To get an exact gain, you can multiply a correction factor $(= \frac{T}{1+T})$, to the gain based on virtual grounding technique. To improve loop gain, cascoding desig n is preferable.