CAD Simulation Project-1: Basic DC characterizations

(Due: Oct. 16th by the end of Class time)

1. In this DC simulation, you can identify Vth, gm and process the parameter of nCox product. Configure schematic as shown below, which will guarantee that the NMOS will be operated always in saturation mode if VGS > Vth.



1. Set W/L=100 m/0.18 m, and sweep VGS from 0 to 4 V. Plot IDS vs. VGS curve.
2. Plot vs. VGS (you can use built-in mathematical calculation function in CADENCE SPECTRE).
3. Plot vs. VGS, and estimate Vth and nCox.
4. Plot vs. VGS (you can check out subthreshold current).
5. Repeat (1)-(4) for the following PMOS (W/L=100/0.18).



1. (body effect) Set VGS=0.6 V (W/L=100/0.18) in the schematic shown below. Sweep VBS from -1 V to +1 V, and plot IDS vs. VBS curve. And Plot vs. VBS (you can use built-in mathematical calculation function in CADENCE SPECTRE).



1. In this simulation, you will identify operation modes of the transistor, and DC current, gm, gds (and ro) depending on the operation modes. In the following set-up, set W/L=100/0.18.



1. Set VDS=0.3 V. Sweep VGS from 0 to 4 V. Plot IDS vs. VGS curve.
2. Plot vs. VGS (you can use built-in mathematical calculation function in CADENCE SPECTRE).
3. Plot vs. VGS (you can check out subthreshold current).
4. Set VGS=0.6 V. Sweep VDS from 0 to 5 V. Plot IDS vs. VDS curve.
5. Plot and vs. VDS (you can use built-in mathematical calculation function in CADENCE SPECTRE).
6. Set VGS=0.7 V and repeat (4) and (5).
7. Set VGS=0.8 V and repeat (4) and (5)

(By comparing (5), (6) and (7), you can confirm that output resistance will decrease when increasing IDS).