# A CMOS Focal-Plane Array for Terahertz Imaging

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***Abstract*— A terahertz focal-plane array (FPA) for video-rate imaging applications has been fabricated in a commercially available CMOS process technology. The 3×5 pixel array uses conventional low-cost quarter-micron NMOS transistors for incoherent power detection. Each pixel has a size of 150×150 $\mu$m$^2$ and consists of an on-chip antenna, an incoherent power detection circuit, and a 43-dB amplifier with a 1.6-MHz bandwidth. At 0.6 THz a pixel achieves a responsivity of 50 kV/W with a minimum NEP of 400 pW/$\sqrt{\text{Hz}}$. Images at 0.6 THz are presented which demonstrate the feasibility of the applied method and show the potential of silicon integrate terahertz FPAs for future low-cost terahertz camera systems.**

## I. Introduction

Great achievements have been made in terahertz science and technologies. However, detectors are often comprised of discrete components which are bulky and exhibit a low level of integration at high cost. Most terahertz images today are build up one pixel at a time, through raster scanning with single-point detectors or phased arrays. Therefore, a fully integrated CMOS FPA is one of the key building blocks that will enable low-cost video-rate terahertz cameras in the future. It presents a crucial step towards the commercialization of terahertz imaging technologies.

Direct detectors have been around for many years and are based on the physical principle of energy/power absorption (calorimeters/bolometers [1], [2]), pneumatic detectors (Golay cells [3]), and square-law detectors (Schottky Barrier Diodes (SBDs) or npn/FET non-linearities). Most of them are, however, incompatible with conventional microelectronics and require additional processing steps to be incorporated into today's semiconductor process technologies.

It is expected that future low-cost portable terahertz cameras will require sophisticated signal processing capabilities, paired with low power consumption and high sensitivity at room temperature. This fuels the growing interest in silicon integrated terahertz detectors. Promising low-cost alternatives include all electronic approaches, such as silicon SBD circuits with cut-off frequencies beyond 1 THz [4], SiGe hetero-junction bipolar transistors (HBTs) with cut-off frequencies as high as $f_{max}/f_T = 350/300$ GHz [5], and CMOS circuits reported at frequencies higher than 400 GHz [6].

In this paper, results of an incoherent 0.6-THz (direct) power detection array fabricated in a conventional low-cost quarter-micron CMOS technology are presented for the first time. The detection principle works, although the radiation frequency is well above the 35-GHz cut-off frequency ($f_T$) of the available NMOS transistors. It is based on: (i) non-quasi-static transport phenomena in NMOS transistors, and (ii), applied self-mixing boundary conditions known from resistive FET mixers.

The detection principle is described in Sec. II and the FPA implementation is given in Sec. III. Measured and simulation results including THz images of postal envelopes measured in transmission mode are presented in Sec. IV. The conclusion follows in Sec. V.

## II. Detection Principle

The terahertz detection is facilitated by the following FET operation principles: (i) the non-quasi-static transport mechanism in NMOS transistors, and (ii), the boundary conditions for self-mixing in resistive FET mixers. The first phenomenon is similar to the theory of transmission lines, which has been a focus of considerable research in the past and is considered being a classical topic of electrical engineering. The mathematical models of transmission lines consist of partial differential equations describing the current and voltage dynamics along interconnects together with the boundary conditions imposed by externally connected loads or components. Similarly, the transport mechanism along the channel of a FET transistor is distributed and can be understood as a bias dependent RC transmission line. Such transistor models are known as Non-Quasi-Static (NQS) models in the literature [7] and include the finite time for the channel charge to build-up. The boundary conditions are usually manifold and make the mathematical treatment of such effects very difficult.

The second phenomenon used to facilitate terahertz detection relates to self-mixing boundary conditions in FET resistive mixers. Self-mixing can be understood from the operation principle of a resistive mixer [8]. In a resistive mixer, the RF and LO signals are usually applied separately to the gate and the drain of an unbiased (cold) FET, while the IF mixing products are observed as part of an extracted $I_{ds}$ current. For self-mixing, though, the RF signal is simultaneously applied to the gate and the drain, and hence, cause a dc current that is proportional to the square of the RF ac voltage. This self-mixing is usually unwanted in FET resistive mixers, but can be utilized in incoherent (direct) power detection circuits. For example in 10-500 MHz power detectors published in 1987 based on JFETs [9], or later, in 0.1-3 GHz GaAs MESFET detectors [10].

The combination of self-mixing boundary conditions with non-quasi-static NMOS device models, therefore, facilitate the detection of radiation from low frequencies up into the terahertz frequency range. At low frequencies the response is primarily resistive self-mixing of the transistor used as a discrete component, while at higher frequencies, the distributed nature of the bias dependent RC transmission line causes distributed self-mixing along the FET channel. To the first

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order, the response is only limited by the parasitic RC time constant and is expected to roll-off with $-20$ dB per decade.

It should be noted, that unlike plasma wave oscillations reported in [11], the distributed self-mixing along the FET channel does not require a propagating plasma wave inside the channel and can be understood from a bias dependent RC transmission line only. The optimum response to terahertz radiation, though, is achieved in combination with external self-mixing boundary conditions.

The NQS self-mixing is being considered by available BSIM device models [7] and can be simulated from strong inversion to the sub-threshold region of a FET resistive mixer. For simplicity, however, it is analytically derived here only for a single device (no NQS effects) in strong inversion ($V_{gs} > V_{th}$) and for a time-harmonic excitation. If an excitation voltage $v_{ds}(t)$ is applied over the drain source junction with zero $V_{ds}$ bias (triode region), the drain current can be calculated as

$$i_{ds}(t) = v_{ds}(t) g_{ds}(t) = v_{ds}(t) \frac{W}{L} \mu Q_{ch}(t), \qquad (1)$$

where $Q_{ch}(t) = C_{ox}(v_{gs}(t) - V_{th} - v_{ds}(t)/2)$ is the time varying channel charge density and where $W$, $L$, and $\mu$ have their usual meaning. The self-mixing boundary condition is $v_{gs}(t) = V_g + v_{ds}(t)$ and was set with an external capacitor $C_{gd}$ connected between the gate and the drain of the transistor as illustrated in Fig. 1 a). For the drain current follows

$$i_{ds}(t) = \frac{W}{L} \mu C_{ox}(v_{ds}^2(t)/2 + v_{ds}(t)(V_g - V_{th})). \qquad (2)$$

The dc-component of the drain current can be calculated for a time harmonic excitation of the form $v_{ds}(t) = V_{RF} \sin(\omega t)$ as

$$I_{ds} = \frac{W}{L} \mu C_{ox}(V_{RF}^2/4)). \qquad (3)$$

This leads to the detected dc output voltage

$$V_{ds} = \frac{I_{ds}}{G_{ds}} = \frac{V_{RF}^2}{4(V_g - V_{th})} \qquad (4)$$

and the expected responsivity is

$$R_v = \frac{V_{ds}}{P_{in}} = \frac{\frac{V_{RF}^2}{4(V_g - V_{th})}}{V_{RF}^2 / R_{in}} = \frac{R_{in}}{4(V_g - V_{th})}. \qquad (5)$$

The noise equivalent power (NEP) is only limited by the thermal noise of the channel conductance $G_{ds}$. Since the channel of the NMOS detector is not dc-current biased, the noise spectral power density at the drain output terminal is $N_0 = 4k_B T / G_{ds}$ and the NEP follows as

$$\mathrm{NEP} = \frac{\sqrt{N_0}}{R_v} = \sqrt{\frac{4^3 k_B T}{R_{in}^2 \frac{W}{L} \mu C_{ox}} (V_g - V_{th})}. \qquad (6)$$

In order to simulate the distributed nature of the transistor, the gate-channel transmission line has to be considered at frequencies in vicinity or above the $f_T$ cut-off frequency. The NQS transport mechanism may be simulated by dividing the FET into segments of smaller FETs as shown in Fig. 1 b). The capacitors $C'$ represent the combined gate-source $C_{gs}$ and gate-drain $C_{gd}$ capacitances of adjacent transistor segments. It appears as a distributed $C_{gd}$ gate-drain capacitance that contributes as a distributed resistive self-mixing at very high frequencies to the overall incoherent power detection.

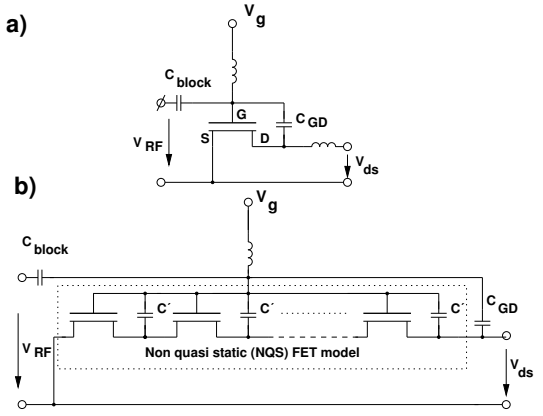


Fig. 1. a) Low frequency incoherent (direct) power detection based on resistive self-mixing with external coupling capacitor $C_{gd}$, and b), the high-frequency NQS representation showing the distributed capacitance between the gate and the channel.

## III. Monolithic Detector Design

A chip micrograph of the implemented 3×5 FPA is shown in Fig. 2. The FPA was manufactured in a 0.25 $\mu$m CMOS process provided by IHP-Microelectronics GmbH, Frankfurt-(Oder), Germany. The available NMOS transistors have a cut-off frequency of $f_T$ = 35 GHz. Each pixel includes an

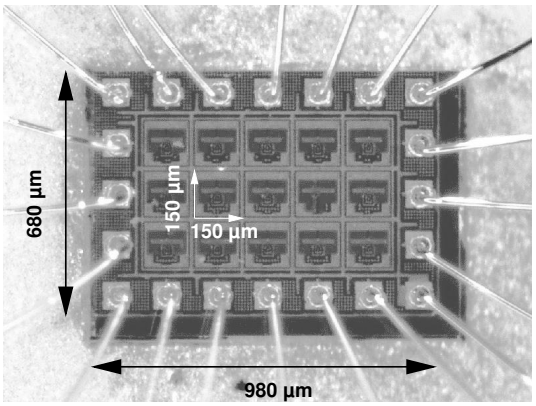


Fig. 2. Chip micrograph. The 3×5 FPA has a pixel size of 150×150 $\mu$m$^2$ and an overall size of 680×980 $\mu$m$^2$ including bondpads.

on-chip, half-wavelength long, 650 GHz tuned folded dipole antenna without a backside ground-plane. The dipole antennas are sensitive to either front-side or back-side illumination depending on the used packaging scheme. Alternative array configurations with narrow-band patch antennas have also been fabricated and include integrated ground planes to prevent backside radiation and coupling to substrate modes. Each pixel detects the signal by a differential NMOS FET pair based on the principle described in Sec. II. To facilitate further on- or off-chip processing of the detected signal, each pixel includes a 43-dB voltage amplifier with a 1.6-MHz bandwidth. Further circuit details can be found in [12].

## IV. Measured Results

The measurement setup used to capture THz images of postal envelopes in transmission mode is shown in Fig. 3 [13]. A similar measurement setup was used to measure the pixel responsivity and noise equivalent power.

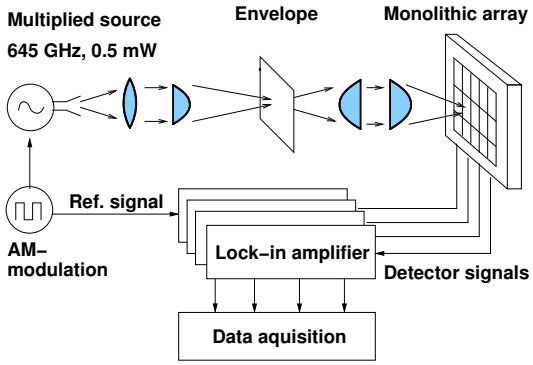


Fig. 3. Measurement setup used to capture 0.6-THz images of postal envelopes in transmission mode at the University of Frankfurt's site [13].

A 645 GHz diode multiplier chain with 0.5 mW output power was used to illuminate a spot on the object through a system of collimating and focusing lenses. A similar lens system was used to project the image back onto the FPA. The multiplier chain was driven by an AM-modulated CW tone in order to facilitate processing of the detected signal with a lock-in technique. As a proof of principle, the array functionality was demonstrated through the simultaneous parallel readout of four pixels from one detector row, while the image was scanned at the image plane. The number of channels was limited by the available lock-in-amplifiers and the associated data acquisition system. The reconstructed image from a four-pixel parallel readout is shown in Fig. 4 with an integration time constant of 1 ms per pixel.

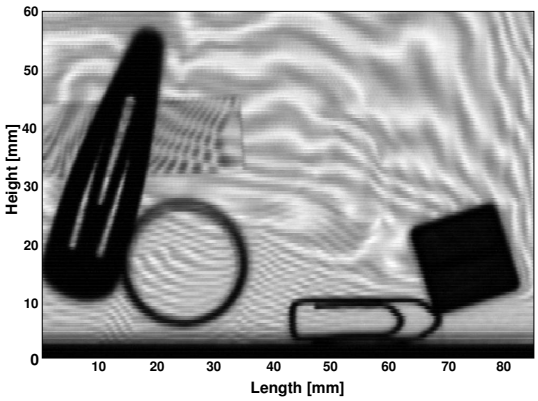


Fig. 4. Captured 0.6-THz image of a postal envelope, revealing its hidden office supplies, such as paper clips, tape and candy bars. The image was reconstructed from a four-pixel parallel readout of the FPA.

Fig. 5 shows the measured and simulated responsivity ($R_v$) of a single pixel. The results were obtained with an illumination power density of 18.3 $\mu$W/mm$^2$. The measured room temperature 606-GHz responsivity is 50 kV/W with a NEP of 400 pW/$\sqrt{\text{Hz}}$ at a 16-kHz modulation, which compares with Golay cells (200-400 pW/$\sqrt{\text{Hz}}$, 45-10 kV/W @10-70 Hz [3]). Simulations indicate that the minimum NEP without amplifier drops to about 60 pW/$\sqrt{\text{Hz}}$ (NMOS channel is not dc-current biased).

## V. Conclusion

A 0.6-THz direct detection 3×5 focal-plane array (FPA) has been implemented in a commercially available 0.25 $\mu$m CMOS process technology. The FPA is not thermal-time-constant limited and has a large 1.6-MHz modulation bandwidth. As such, it will enable video-rate imaging applications at 0.6 THz in a low-cost CMOS process technology and leads to the construction of terahertz cameras, practical for a wide range of high profile applications.

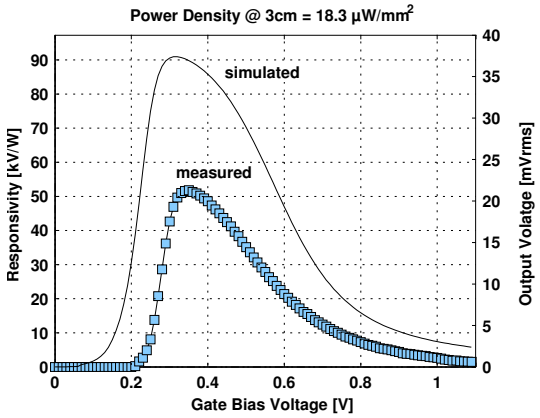


Fig. 5. Measured and simulated pixel responsivity versus $V_{gs}$-bias.

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