15.1 A 1kPixel CMOS Camera Chip for 25fps Real-Time Terahertz Imaging Applications

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Future imaging applications in the submillimeter-Wave range (300GHz to 3THz) require RF systems that can achieve high sensitivity and portability at low power consumption levels. In particular, CMOS process technologies are attractive due to their low price tag for industrial, surveillance, scientific, and medical applications. Recently, CMOS-based detectors have shown good sensitivity up to 1THz with NEPs on the order of 66pW/√(Hz) at 1THz [1]. However, CMOS terahertz imagers developed thus far have only operated single detectors based on lock-in measurement techniques to acquire raster-scanned images with frame rates on the order of minutes [2]. To address these impediments, we present a low-power 1kpixel terahertz camera chip fully compliant with an industrial 65nm f_t/f_{max}=160GHz/200GHz CMOS process technology. The active-pixel circuit topology is designed to accommodate the optics for wide bandwidth (0.6 to 1THz) in stand-off detection with a 40dBi Si-lens. It includes row/col select and integrate-and-dump circuitry capable of capturing terahertz images with video frame rates up to 25fps at a power consumption of 2.5µW/pixel.

The imager follows a global shutter readout scheme as indicated in Fig. 15.1.1. The core of a pixel consists of a ring-antenna and a cold (non-biased) differential NMOS distributed resistive mixer. The RF signal is coupled to the source of the mixer and is directly downconverted to DC within the transistor itself, in order to enable the operation above the transistor's f_{max} according to [3].

Conventional CMOS image sensors for the visual spectrum typically utilize a photodiode detector and require a separate reset transistor in order to clear all integrated charges on a floating diffusion. Unlike this, the readout circuit scheme here uses the NMOS detector transistor itself to reset the accumulated charges on the integration capacitor, reducing the number of required circuit elements. The detector transistor may be seen as a current source in parallel with the channel resistance of M1 and an 8pF integration capacitor C_{int} (see Fig. 15.1.2). The integration/reset time constant is controlled by the voltage level of the reset signal. The transistor M1 is followed by a readout transistor pair M3/M4 acting as a differential pair with an attached offset-compensation circuitry (blind reference pixel). The differential-pair stage is biased by the voltage on the common node of the antenna.

In terms of the readout circuit design, the key challenge is to achieve low power consumption levels. A single row is therefore biased up at-a-time by a 5-bit row encoder and the differential pairs in each column share a common active load (M6-M7) providing a simulated open-loop gain of 50dB per pixel. A digitally controlled multiplexer selects a single pixel to be further buffered by a unity-gain amplifier (0.4MHz gain-bandwidth). This readout scheme enables parallel operation of 1024 pixels, while the readout circuitry activates only a single row (32 elements).

In order to improve the RF and noise performance of a pixel, its detector transistor was designed using two differentially driven 1µm-wide isolated-well low-power and low-threshold RF NMOS transistors with a minimum gate length of 60nm.

The on-chip antennas are designed to feed a commercially available extended hyperhemispherical silicon lens (D=15mm) through the backside of the silicon die in order to minimize the influence of surface waves and to increase the detector gain. In terms of the antenna design, the key challenge is the high input impedance of the detector transistors in the range of 500 to 1000Ω, making it difficult to design a broadband conjugate impedance match. The antenna layout includes the full metal stack with dummy fill to be compliant with an industrial qualified CMOS process technology. The detector transistors are located in the antenna center and are fed differentially. Other pixel circuitry, including integrating capacitors, the blind reference pixel and the differential cascode are placed below the ground shield surrounding each pixel. This layout symmetry enabled a wide-band radially symmetric antenna pattern. The silicon die (15Ω-cm resistivity) was thinned down to 150µm and active layers were selectively blocked to minimize substrate incurred losses. The simulated radiation efficiency of the antenna radiating into a hypothetical semi-infinite lossless silicon substrate through the die is about 70 to 77% from 0.8 to 1THz.

The 32x32 FPA exhibits an 80µm pitch and was aligned with the lens center and glued together using a low-shrinkage UV epoxy. The ratio of the chip width-to-lens radius (R) is 0.34 in order to avoid excessive reflection losses at the air-silicon interface (no antireflection coating). The FPA is thereby located slightly below the elliptical position with a lens extension (X) of 2.75mm. Including the die thickness, the X/R ratio is 0.366 [4] resulting in a residual reflection loss of about 2 to 3dB and an experimentally confirmed field of view of about ±23 degrees [5]. To demonstrate low-power and low-cost packaging solutions for hand-held applications, the overall assembly was mounted and wire-bonded onto a low-cost FR4 PCB (see Fig. 15.1.3), which provides a considerable cost benefit compared to other waveguide based THz technologies.

In terms of imager-characterization, the key issue is that the detector circuit with its on-chip antenna and lens assembly cannot be characterized independently from each other at THz frequencies. The antenna directivity can only be estimated, therefore we measure an isotropic optical system performance through the use of an isotropic referred voltage responsivity (Rvi) and an isotropic referred noise equivalent power (NEPi), which both take into account implementation losses and include the unknown directivity of the receiver antenna. Figure 15.1.4 shows the measured Rvi and NEPi at 900GHz vs. bias conditions for a center pixel at different chopping frequencies (10 to 1024Hz). The figure also shows the roll-off of the peak Rvi and NEPi versus frequency for two different chopping frequencies (100Hz, 1024Hz), thus confirming its broadband characteristics. At 900GHz and at a 1kHz chopping frequency, the minimum NEPi is 47fW/√Hz and the maximum Rvi is 566MV/W. Based on an estimated 40dBi antenna directivity, the minimum detector NEP is 470pW/√Hz and the maximum Rv is 56.6kV/W. These numbers are different from previously reported results of a single (cold) resistive mixer in [1] because the active pixel includes additional noise and gain from the readout transistors (M3-M4).

Figure 15.1.5 shows a one-second stand-off video sequence (pan shot) captured at a frame rate of 25fps. The pan shot was taken by turning the camera vertically on the horizontal axis, while the camera was facing two point sources in line-of-sight. Both sources (0.65 and 0.9THz) were positioned in the lens near-field at a distance of about half a meter, thus spilling over some of the incident power onto neighbor pixels. The 25 consecutive recorded images are arranged from the top-left to bottom-right and indicate the vertical motion of the two point sources. The chip output was first amplified by 34dB and sampled with a 16bit ADC at 25.7kHz (411.2kb/s). Fixed-pattern noise was removed after dark-image calibration and the image data is plotted on a log scale to visualize residual image noise. The residual noise is uniformly distributed across the array with a 20mV_{rms} (400μV_{rms} excl. 34dB gain). A comparison of CMOS FPAs is shown in Fig. 15.1.6.

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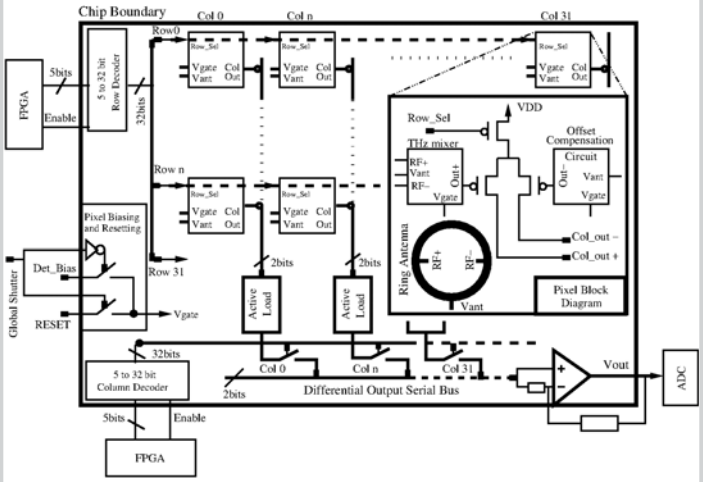

Figure 15.1.1: THz camera block diagram.

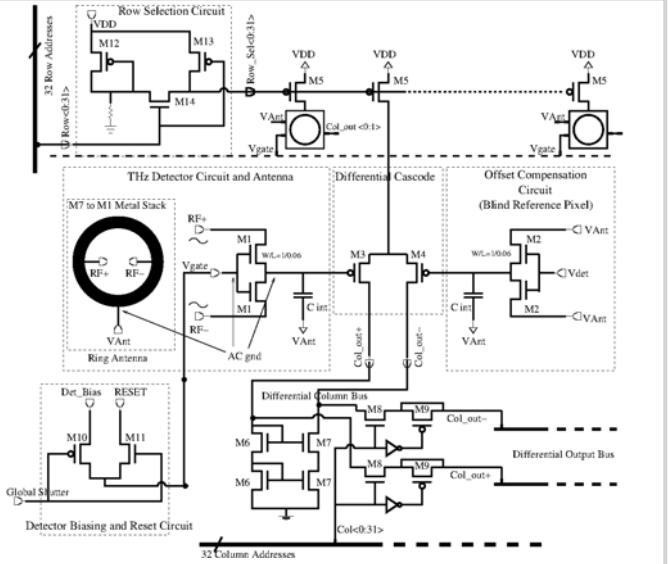

Figure 15.1.2: Detailed circuit schematic of the THz camera.

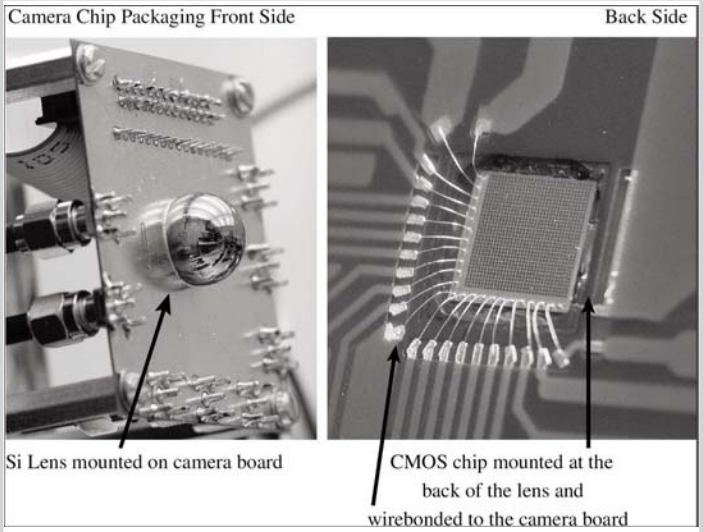

Figure 15.1.3: Photograph of the THz CMOS camera chip packaging from the front and the back side.

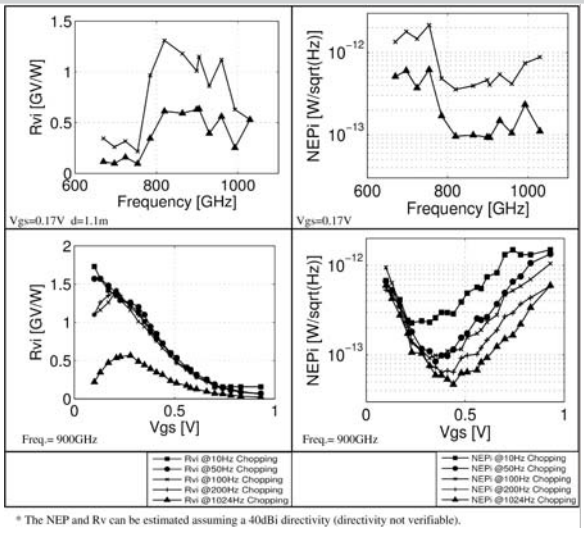

Figure 15.1.4: NEPi and Rvi versus frequency at 1.1 meters for V_{gs}= 0.17V (top) and at 900GHz versus gate bias (bottom).

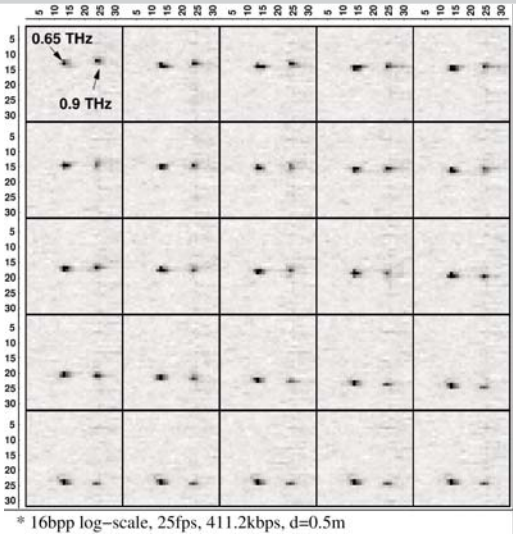

Figure 15.1.5: A 1-kpixel 25fps video sequence of two point sources (0.65 and 0.9THz).

Technology	FPA array size [X×Y]	[1]BW/Freq. [THz]	Power Diss. [μW/pixel]	max Rv [V/W]	min NEP [pW/√Hz]	Frame Rate [fps]	Optics	Reference
Bolometer (7K cryo-cooled for passive imaging)								
NbN	64x1	0.3-1 (no 3dB)	-	-	0.008	conical scan 6fps	micro-lens	[6]
CMOS-based (room temperature active imaging)								
0.65μm bulk	1024 (32x32)	0.75-1	2.5	[2]566M, 0.9THz [3](56.6k, 0.9THz)	[2]0.047, 0.9THz [3](470, 0.9THz)	25fps, 0.6-1THz	Si lens	this work
0.65μm bulk	15 (3x5)	0.65-1	-	800, 1THz	66, 1THz	scanned, 1THz	Si lens	[1]
0.25μm bulk	15 (3x5)	0.65	5500	80k, 0.6THz	300, 0.6THz	scanned, 0.6THz	-	[3]
0.13μm	12 (3x4)	0.3-1 (no 3dB)	97	1.8k, 1.05THz	-	scanned, 0.3THz	-	[2]

[1]3-dB Rv bandwidth if not stated otherwise
[2]Measured isotropically referred Rvi and NEPi (assuming an isotropic antenna directivity)
[3]Estimated Rv and NEP under the assumption of a 40dBi antenna directivity (antenna directivity not verifiable)

Figure 15.1.6: Comparison table of state-of-the-art active THz imagers in CMOS.

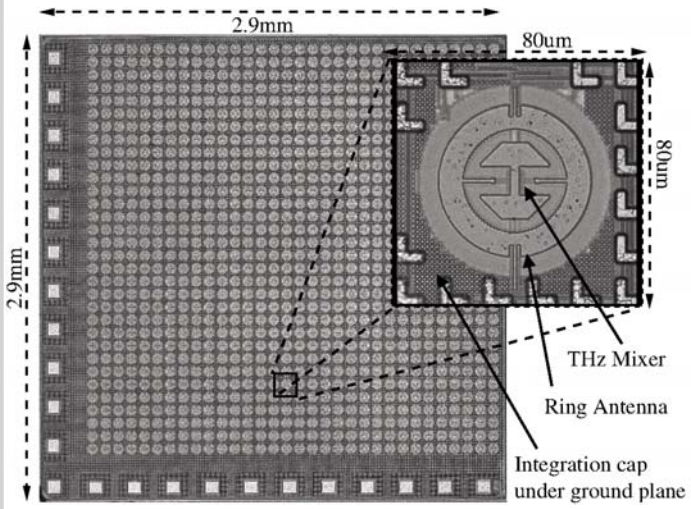

Figure 15.1.7: Chip micrograph.

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