Thermal Image and Analysis of a 28.3 THz 0.18μm CMOS Detector

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***Abstract*— This paper presents the measured results of the distributed thermal image of a 28.3 THz CMOS thermal detector of area 65 um * 45 um, consisting of antenna, thermal-coupling and thermal sensing circuit elements integrated monolithically. In contrast to the conventional THz thermal detectors, the proposed detector design shows subtle temperature distribution profile of the CMOS detector, leading to understanding of the individual role of the building element of the detector and confirmation of the design approach for future improvement.**

I. INTRODUCTION

It had been reported recently that post-CMOS technology could be applied for designing THz and IR thermal sensor. For example, thermopiles consisting of p-type and n-type polycrystalline silicon with micromachining were reported [1]. In some approaches the sensing component is integrated with antennas to enhance the response of received THz signals [2]. These types of thermal sensors usually required CMOS electronic circuit to convert the thermal information to meaningful voltage signals.

This paper presents a new approach to the design of THz sensor using direct antenna thermal coupling to the electronic thermal sensing circuit. The electronic temperature-sensing circuit is a direct way for sensing the temperature variation. This leads to a compact THz CMOS sensor design with the complete CMOS THz sensor schematics and the package of the monolithic sensor shown Fig.1 and Fig.2, respectively.

When increasing the operating frequency of the THz sensor, one observes that the size of sensor will be larger than the operating wavelength. On the other hand, in our particular THz sensor design, the size of the THz sensor is larger then the laser beam width as shown in Fig.2. In the 0.18 um CMOS foundry employed in our design, most of the circuit elements of Fig.1, including transistors and resistors, have dimensions comparable or considerably larger than that of the antenna operating at 28.3 THz.

The effect of non-uniform temperature distribution of the THz CMOS sensor of dimension much larger than the operating bandwidth is an important phenomenon for sensing application. In this paper, for the first time, we will report the distributed temperature phenomena of the CMOS THz sensor, which is not a global temperature, but a distinct measure of temperature as a function of position. By scanning the THz laser beam across the chip, we can construct the two-dimensional thermal image of the THz sensor of size much larger than the operating wavelength. The resultant image shows that we may differentiate the subtle details of the THz sensor image two-dimensionally.

Section II briefly describes the physics of temperature dependence of the constituting elements of the PTAT (proportional-to-absolute-temperature) electronic temperature-sensing circuit in CMOS. Section III reports the layout of the proposed PTAT sensing circuit and the thermal simulation of the entire CMOS THz sensor, followed by the display of the measured two-dimensional thermal map in Section IV, which also discusses the temperature-distributed characteristics of the CMOS THz sensor.

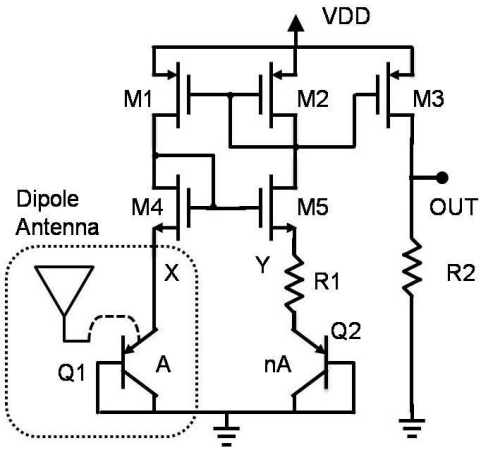

Fig. 1 Schematic of the CMOS detector at 28.3 THz. The dipole antenna is integrated with Q1 (the dashed block)

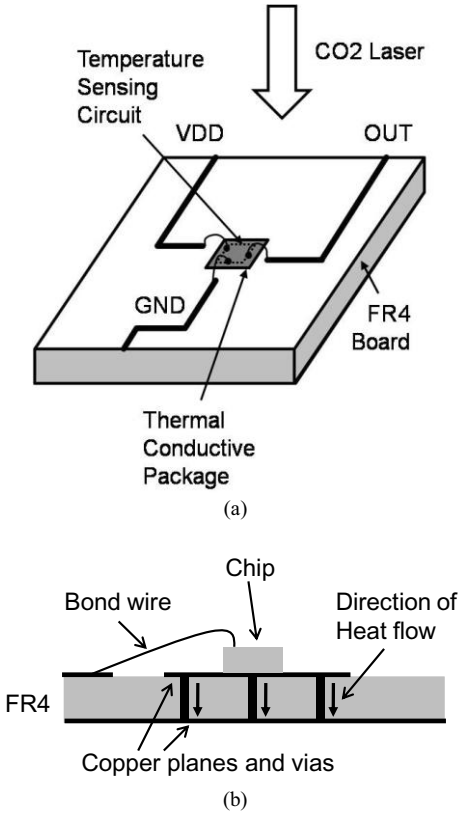

Fig. 2 (a) The diagram of the detecting system including single-chip 0.18um CMOS sensor and packaging. (b) Side view of the package and heat flow paths.

II. Temperature Dependency of PTAT Circuit Components

The PTAT circuit is a common configuration for temperature sensing purpose (see Fig. 1) [4], [5]. Basically the PTAT circuit adopts two bipolar junction transistors (BJTs) of unequal emitter areas. The relationship between temperature and the collector current of a bipolar junction transistor is

$$I_C = I_S\left(e^{V_{EB}/V_T} - 1\right) \quad (1)$$

$$V_t = \frac{kT}{q} \quad (2)$$

It can be seen that the collector currents of the two BJTs are unequal, and the difference between their emitter-base voltages is proportional to absolute temperature [5]. Note that I_s is saturation current, V_t is called thermal voltage, and k is Boltzmann constant. In general I_S and V_t are both proportional to temperature. The PTAT circuit can be easily realized in CMOS process, and is commonly used for designing voltage reference or temperature sensing circuits.

The CMOS THz sensor intercepts 28.3 THz signal acting as a heat source. [3] The temperature variation caused by the heat source will result in the change of current of the transistor. Suppose the temperature of both Q1 and Q2 are the same, and defining $V_x = V_y$ by the MOS current mirror, the output voltage is [5]

$$V_{out} = \frac{R_2}{R_1} V_T \ln n \quad (3)$$

Note that this formula assumes the resistance is not a function of temperature. In reality, the formula should be revised to

$$V_{out} = \frac{R_2(T)}{R_1(T)} V_T \ln n \quad (4)$$

More, the properties of resistor with temperature are in principle modelled by first-order and second-order temperature coefficients of resistors (TC1 and TC2):

$$R(T+\Delta T) = R(T)\left(1 + TC1(\Delta T) + TC2(\Delta T)^2\right) \quad (5)$$

If TC1 is positive, the resistance will increase with temperature, and vice versa. Typically, the TC1 decreases as the doping decreases [6], [7]. In this process, the TC1 of p-type polycrystalline silicon is nearly zero, however it can vary slightly positive or negative depending on the device layout or process variation.

As for the MOSFET, the drain current is represented as

$$I_D = \frac{1}{2} k' \frac{W}{L}\left(V_{GS} - V_t\right)^2 \quad (6)$$

Note that V_t here is threshold voltage. Both threshold voltage and k' are temperature sensitive. The threshold voltage decreases as temperature increases, giving rise to a factor of the increment of drain current. However, the dominant factor is k', which decreases as temperature increases, and the drain current thus decreases [8]. In our case, we assume the MOS current mirror in Fig. 1 is ideal, so the relationship of the output voltage and the MOS with temperature can be ignored.

The process variation will also affect the output value described in (3). This is due to the variation of R2/R1 term mainly. In our particular design reported here, if R2/R1 has variation of 1%, the output value will deviate 10mV approximately.

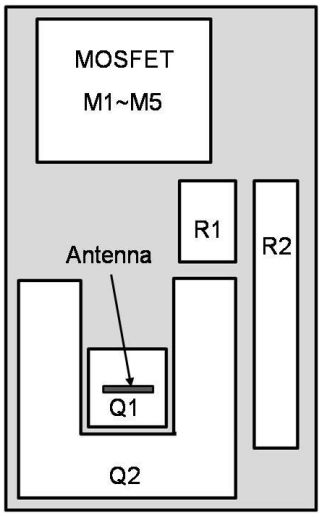

Fig. 3 Layout of the 0.18um CMOS detector at 28.3 THz.

III. Layout of Sensing Circuit and Thermal Simulation

Fig. 3 shows the layout of the PTAT circuit. The temperature sensing circuit is fabricated on 0.18um 1P6M CMOS foundry process. Two bipolar junction transistors, Q1 and Q2, are of junction area ratio about 1:7. The size of Q1 is 10 um*10um. Q2 is seven transistors of the size of Q1 connected in series, placed around Q1 to achieve compact layout. The resistor R1 is of p-doped polycrystalline silicon (P-poly) film, while resistor R2 is connected by films high-resistivity polycrystalline silicon (HR-poly), which resistance is about 20 times of R1. According to the previous section on temperature coefficient, the TC1 value of R1 is nearly zero, and the TC1 of R2 is negative. The area of this PTAT circuit is 65um*45um, and the area of Q1 and Q2 core is 30um*30um.

The test chip has volume about 800*800*500 um^3, mounted on a 1.6mm thick FR4 board without molding. Gold bond wires of 1 mil diameter are used. FR4 board originally prohibits heat dissipation from chip because it is a low thermal conductivity material. In order to produce temperature distribution with less global temperature rise, we design a thermal conductive package on the board to transport heat (see Fig. 2(b)). This is realized by adding via holes connecting to the back side ground plane of the PC board, touching the 3D position stage of the measurement system. In this case when the test chip is heated, its temperature rises locally but with minor global temperature rise at about 0.9℃(see Fig. 4), no matter how small the thermal load area is.

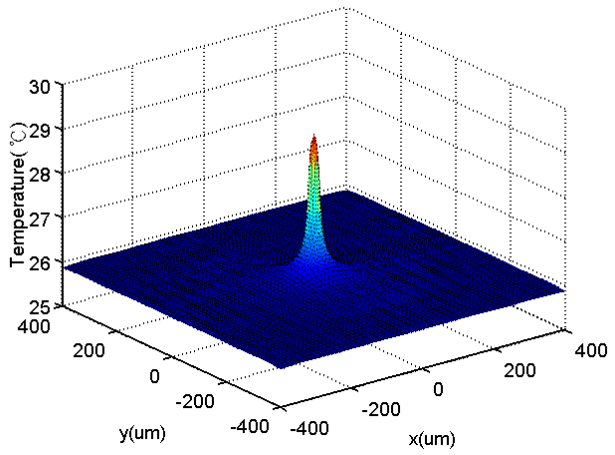

Fig. 4 Simulated result of temperature distribution of packaged single-chip CMOS detector with CMOS chip dimension of 800um*800um*500um.

To know the role the copper planes and vias on the die bounding interface (Fig. 2(b)) plays, we set two simulation settings with or without the copper plane and vias on FR4 board using Ansoft EPhysics. In simulation, we set a uniformly-distributed heat source on a circle with diameter 26um, which is approximately equal to the laser beam width. The power of the heat source is set 20 mW, which is about the laser power dissipated in the chip in out experiment. The ambient temperature is 25℃. The simulation result in Fig. 5 shows the steady state solution with thermal conductive boundary. In two cases we can see that if no conductive plane set, the maximum, minimum and average temperature are 54.1 ℃, 51.2℃, and 52.0℃, respectively, and this means that the temperature increment is almost global. If the conductive plane is attached (see Fig. 2(b)), the maximum, minimum and average temperature become 29.1℃, 25.7℃, and 26.5℃, respectively (see Fig. 4). The results show that by adding metal planes and vias on the FR4 board, the temperature distribution can be approximated to no global heating. The local heating effect on the chip thus can be observed clearly.

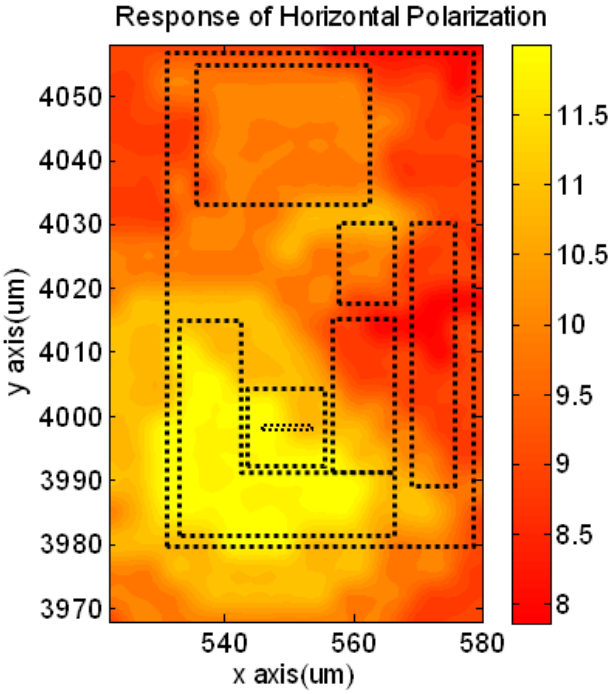

Fig. 5 Thermal image of the PTAT circuit with 28.3THz wave scanning. The pattern of response image fit the circuit layout properly. The output voltage increases most in the region of the antenna and BJT Q1 and Q2. The dashed line indicates the layout shown in Fig. 4.

IV. Measurement Result of Temperature Variation and Response Image

In this experiment, the CO_2 laser is applied to observe the thermal effect. The laser intensity is adjusted by a polarizer-analyzer-attenuator, and a pyroelectric power meter is used monitor the real time laser power. The output laser beam is controlled horizontal polarized by the thin film polarizer. A convex-concave lens with no chromatic aberration focalize the beam on the chip. By using knife-edge scan method, the measured beam width is 26 micrometer, which is closed to the diffraction limit at 10.6 um wavelength. The packaged chip is placed on a 3D position-adjustable stage, which precision is 1 um. After adjusting to the focal spot, we use the laser to scan through the whole area of temperature sensing circuit point-by point, and get the two-dimensional spatial response by moving

through x or y direction. The incident power of the CO_2 laser is 103 mW.

When there is no laser power incidence, the initial output voltage of PTAT circuit is designed about at 960 mV. When the laser is incident on the chip, voltage output increases, generally from about 7 mV to 12 mV around the circuit, depending on what circuit component the beam intercept, and how many power the illuminated area absorbs. Standing on the voltage increment at each point, the thermal image is demonstrated in Fig. 5.

In room temperature, the measured initial output is 961mV. The measured response image is shown in Fig. 6. When the incident wave is impinging on the two BJTs and dipole antenna, the antenna and following circuit elements covert the electromagnetic energy into heat. When the laser beam energy focuses on the core region of 30um*30um, temperature rising of the antenna, Q1 and Q2 makes output voltage increase most. This result confirms the proposed THz sensing approach successfully. If we assumed conventionally that Q1 and Q2 heated nearly uniformly, the output increment in this area is all as predicted in (3). However, we observe that the output level is different from the BJT core. On the upper right half of the core, the output incremental voltage is obviously less than the bottom left half.

This result is derived from the negative TC1 value of R2. As the laser beam moves near R2, some power is absorbed by R2, resulting in the decreasing of the resistance of R2. From (4) and (5), the resistance of R2 becomes lower when temperature grows, and the output voltage is therefore lower than predicted in (3). This implies that the local temperature distribution of temperature sensing circuit can influence the performance of the circuit in CMOS ICs. This influence should be considered in designing THz and infrared antenna-coupled thermal sensor.

V. Conclusions

The temperature-distributed two-dimensional thermal image of the CMOS THz sensor is presented for the first time. The thermal image reveals subtle variation of circuit elements under local heating. Analyzing the meanings of the subtle variation, the image reveals more physical understandings and insight. These results show us observations of temperature distribution inside temperature sensing circuit in um-scale, and provide more precise and practical reference on THz thermal sensor design.

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