Terahertz Imaging Detectors in a 65-nm CMOS SOI Technology

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***Abstract*—Terahertz imaging detectors implemented in a 65-nm CMOS SOI technology are presented. Low-noise square-law power detection is provided by distributed self-mixing in NFET-based passive mixers with optional integrated amplifiers. The pixels of the imaging array are equipped with folded-dipole antennas designed for through-substrate illumination by an integrated silicon lens. With front-side illumination and conductor backing of the chip a maximum non-amplified responsivity ($\mathbf{R}_v$) of 1.1 kV/W and a minimum noise-equivalent power (NEP) of 50 pW/$\sqrt{\text{Hz}}$ is achieved. In the intended lens-integrated back-side illumination configuration a further 8-dB improvement of $\mathbf{R}_v$ and NEP due to the elimination of substrate modes is predicted by EM simulations.**

I. Introduction

The use of terahertz radiation (0.3-10 THz) is gaining interest in imaging [1] and biomedical analysis applications [2]. The main advantage of this frequency range is the ability to use non-ionizing radiation for penetrating imaging of dielectric materials. However, the use of single-pixel detectors based on bolometers or Schottky diodes in mechanical scanning configurations has hampered the development of highly integrated video-rate terahertz imagers. By contrast, low cost multi-pixel CCD and CMOS sensors are commonly used in optical imaging. Hence, integration of terahertz detection capability in such a process technology would be an important step towards wide-spread use of terahertz imaging.

Square-law terahertz power detectors for imaging applications have previously been demonstrated in a 0.25-μm CMOS technology [3]. Cold FETs (non-biased channel) were used to generate the detection voltage by self-mixing in a resistive mixer [4], which has also been previously demonstrated at lower frequencies in [5] and [6]. In [7] it has been shown that by considering the distributed self-mixing effect in the FET channel, terahertz detection can be obtained at frequencies far above the transit-time limited cutoff frequency of the technology. However, the use of fast small-feature-size devices is expected to improve the detection and lower the noise through more efficient modulation of the channel. Silicon-on-insulator (SOI) technology offers a way of improving sensitivity by lowering the parasitics of the detector devices. Terahertz detection using SOI NFETs has been investigated in [8] but no calibrated responsivity or noise data was provided.

A critical component of an integrated CMOS terahertz pixel is an efficient antenna, which should provide good coupling to the optical system. The folded-dipole antennas integrated with the CMOS detector devices in [3] suffer from reduced efficiency due to the presence of a low-resistivity silicon substrate underneath the radiator. While the substrate-shielded patch antennas presented in [7] are not subject to such losses, the bandwidth of such patch antennas is limited to 5% by the thin dielectric layer available in the SiO_2 backend. Silicon-on-insulator (SOI) technology with high-resistivity mechanical substrates offers an alternative for a low-loss implementation of through-substrate radiating dipole antennas. The back-side illumination is especially useful in monolithic focal-plane arrays where a silicon lens is brought into direct contact with the detector die. Due to the reduced wavelength in the silicon material, the pitch can be reduced for a given diffraction-limited optical resolution. Since the area, and thus the cost, of a monolithic FPA is primarily dominated by the antennas and the pixel pitch, through-substrate illumination can lead to significant cost savings.

In this paper, terahertz imaging pixels implemented in a 65-nm CMOS SOI technology are presented. The use of fast nanometer devices and dipole antennas on a high-resistivity SOI substrate yields pixels with improved responsivity and lower noise compared to the previously demonstrated 650-GHz detectors in 0.25-μm (Bi)CMOS technology in [3] and [7].

II. CMOS Detector Design

In an imaging application, a focal-plane array (FPA) of pixels is used together with an optical system. Each pixel consists of a terahertz square-law detector circuit with an optional integrated pre-amplifier as well as an on-chip folded dipole antenna.

A. Terahertz Square-Law Detector Circuit

Figure 1 shows a schematic diagram of the square-law detector circuit based on NFET transistors with non-biased (cold) channels. The gates of the differential NFET pair T1/T2 are provided with the received terahertz signal from the dipole balanced antenna. A gate-bias voltage V_{fet} is also applied through the antenna. Since the V_{opamp} bias node forms a

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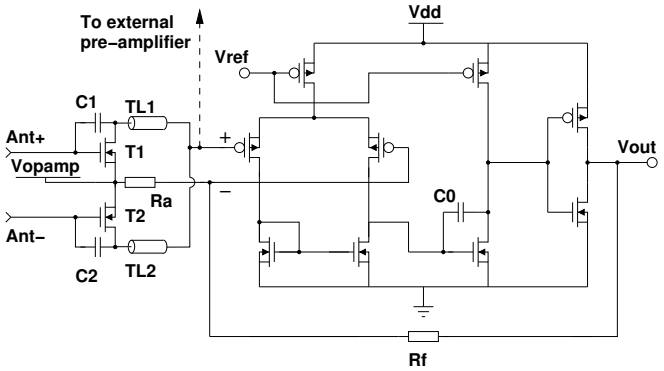

Fig. 1. Schematic diagram of a single pixel with the optional integrated operational amplifier included. The square-law detectors T1/T2 are provided with gate bias and the differential input signal through the $Ant+/Ant-$ terminals while the V_{opamp} node forms a virtual ground.

virtual ground, half of the input signal appears as a time-varying $v_{gs}(t)$ gate-source voltage across each transistor. Two 6-fF large MOS coupling capacitors C1/C2 are used to tie the drain potentials of the transistors to their respective gates at terahertz frequencies. Hence, the $v_{ds}(t)$ voltage across the channel shifts simultaneously with the $v_{gs}(t)$-modulated channel conductance over a period of the terahertz wave, thus generating a dc current by square-law detection. Two quarter-wave long transmission-line stubs TL1/TL2 are used to extract the generated dc signal to the on-chip or off-chip amplifier without disturbing the terahertz signal at the drain nodes.

The three-stage operational amplifier uses PMOS transistors in its differential input stage due to their lower flicker noise. The input transistors drive an active load followed by a second gain-stage with a feedback capacitor, which improves the stability. In order to drive an off-chip low-impedance load, an inverter is used as an output stage. Negative feedback employed for the three-stage amplifier by a resistive divider. The simulated closed-loop gain is 38 dB with a 1-MHz 3-dB bandwidth and a phase margin of approximately 50-degrees. The amplifier consumes 3.6 mW from a 1.2-V power supply.

B. On-chip Antenna

Figure 2 shows the on-chip antenna of a pixel, which is based on the asymmetric coplanar strip-line folded dipole described in [9]. Different strip widths W_{a1} and W_{a2} have been used in the folded dipole design for an increased antenna impedance. Hence, a better match to the high-impedance input of the CMOS detector circuit could be obtained. The antenna is implemented in the M6 top-metal layer of the thick Cu/SiO_2 backend of the SOI technology. In this environment the maximum simulated (Agilent ADS Momentum) impedance achievable with a practical radiator geometry is 800+j800Ω, which requires a width of W_{a1} = 20 μm and W_{a2} = 2 μm as well as a spacing S_a of 4 μm. A length L_a of 84 μm is required for a 650-GHz resonance. In a 2×400-Ω system the -10-dB bandwidth of the antenna is 110 GHz.

The excitation of substrate modes can be a dominant loss mechanism of mmWave and terahertz dipole antennas implemented on semiconductor substrates. If the chip is mounted on a metallic carrier, a maximum simulated front-lobe gain of -7.4 dBi with a 1.7-dBi directivity is obtainable. This corresponds to an antenna efficiency of only 12.5% due to high substrate-mode losses. However, in SOI technologies, guided substrate modes can be avoided by back-side illumination through the low-loss silicon carrier. With a silicon lens placed in direct contact with the substrate, as shown in Fig. 2, simulations indicate that an antenna efficiency of over 80% can be achieved, which corresponds to an 8-dB improvement over the front-side illumination case.

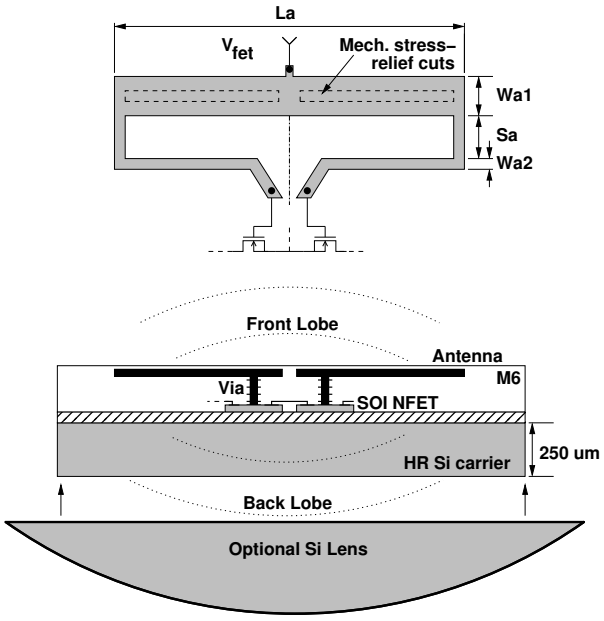

Fig. 2. Layout and cross section of the asymmetric folded-dipole antenna with the optional lens for back-side illumination included.

III. Layout and Manufacturing

Imaging pixels have been arranged in a 3×5 array as shown in Fig. 3. Pixels with and without integrated operational

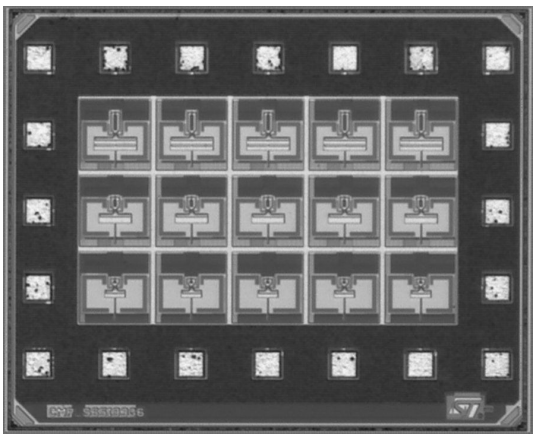

Fig. 3. Micrograph of the 1×0.9-mm^2 large multi-pixel test chip in 65-nm CMOS SOI.

amplifiers are interleaved in the array for evaluation purposes. The detectors have been manufactured in a 65-nm CMOS SOI process from STMicroelectronics, which features a six-metal-layer backend.

IV. Characterization Setup

Figure 4 depicts the R_v and NEP characterization setup together with a setup for 2D-imaging by mechanical scanning of objects through the terahertz beam. A multiplied 650-GHz source with an effective isotropic power (EIRP) of 23.1 dBm is used as the illumination source. For the characterization of the detectors without an integrated operational amplifiers an external 60-dB gain voltage amplifier with a 6 nV/$\sqrt{Hz}$ noise floor is used. The output power of the signal source is gated (chopped) by a 2-kHz square-wave and detected by a lock-in amplifier in order to mitigate the effects of dc-offsets and 1/f-noise in the measurement system. In the R_v and

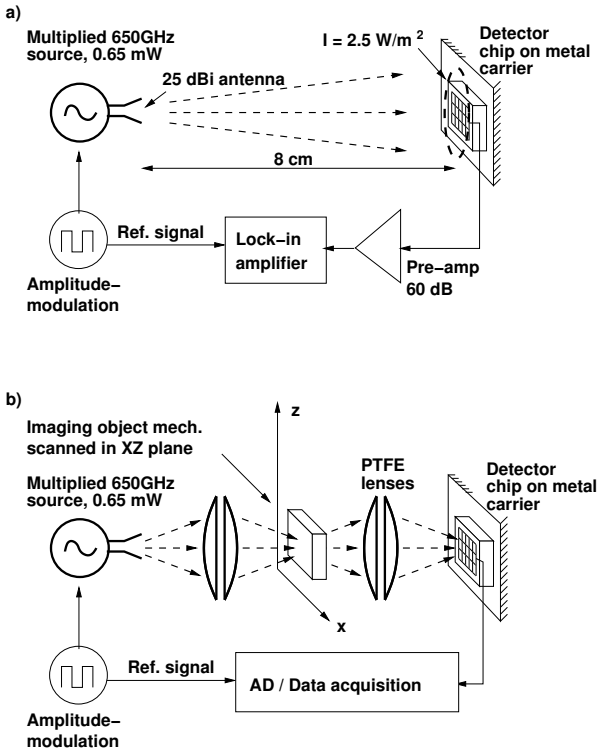

Fig. 4. Free-space setup for R_v and NEP measurements of non-amplified pixels (a). Transmission-mode imaging is provided by mechanical scanning in the XZ plane (b).

NEP free-space characterization setup (Fig. 4a), the detector chip is positioned at a distance of 8 cm in front of the 25-dBi horn antenna of the 0.65-mW source. Hence, using Friis transmission equation, a 2.5-W/m^2 irradiance I at the plane of the detector can be calculated. The irradiance has been verified through measurements of the beam profile as well as the total radiated power, yielding a value of 2.3 W/m^2, which is in reasonable agreement with the calculated irradiance. The input power P_{in} available to each detector is calculated from the irradiance and the effective antenna area A_{eff}. Due to the symmetry of the array structure, the incident power is shared between adjacent pixels. Thus, the maximum A_{eff} in the multi-pixel array is restricted to the physical area of the 150×150-μm^2 large pixel. This area is also in close agreement with $2.5 \cdot 10^{-8}$ m^2 A_{eff} calculated from the simulated 1.7 dBi directivity of an antenna in the array. Hence, the power P_{in} available to a pixel can be calculated as the product of the irradiance I and the effective area A_{eff}.

In Fig. 4b the setup used for transmission-mode terahertz imaging is shown. The output signal of a single pixel with an integrated amplifier is sampled by a data-acquisition system while the object is scanned over the XZ plane through the beam by computer-controlled stepper motors.

V. Results

The measured and simulated (foundry transistor model) responsivity for a non-amplified pixel is presented in Fig. 5 for a swept V_{gs} bias voltage of the detector devices T1/T2. The simulated R_v includes the 12% efficiency of the integrated dipole antenna predicted by an EM-simulator. A maximum

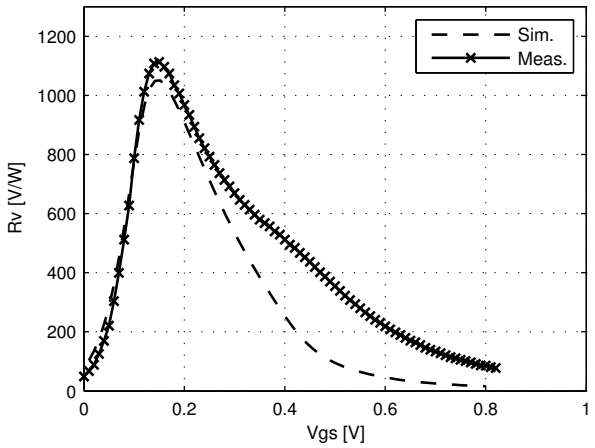

Fig. 5. Measured (crosses) and simulated (dashed line) responsivity (R_v) of a non-amplified pixel with a detector-device V_{gs} bias swept from 0 to 0.8 V. Note that the 12% antenna efficiency predicted by an EM simulator is included in the simulated result. The capacitive load of the measurement system and cables (included in the simulation) causes a roll-off of R_v in the high-impedance sub-threshold region.

measured R_v of 1.1 kV/W is obtained at a 0.15-V bias, which can be compared to a simulated R_v of 1.05 kV/W. The roll-off of R_v at V_{gs}-voltages below the maximum is caused by the capacitive loading presented by the connecting cable between the detector chip and the external pre-amplifier. This cable load was also included in the simulation. A pixel equipped with an integrated amplifier yields an R_v of 72 kV/W at 0.2-V V_{gs} bias. This result agrees well with the product of the 38-dB voltage gain of the operational amplifier and the measured R_v of the non-amplified pixel.

Figure 6 shows the measured and simulated NEP of a pixel without an integrated amplifier. Due to the reduced channel noise obtained with a higher V_{gs}-voltage, a minimum measured NEP of 50 pW/$\sqrt{\text{Hz}}$ is obtained at a 0.35-V gate

bias. The measured NEP has not been corrected for the noise generated by the measurement system and the external pre-amplifier. Hence, a discrepancy between the measured and the simulated NEP is observed for V_{gs} larger than 0.4 V since the reduced R_v in this region causes the output signal to drop below the noise floor of the measurement equipment. The obtained NEP result represents a marked improvement over the previously reported 300 pW/$\sqrt{\text{Hz}}$ of a 0.25-μm CMOS technology in [7]. It also compares well to the 20 pW/$\sqrt{\text{Hz}}$ reported in [10] for III-V Schottky detectors at 800 GHz.

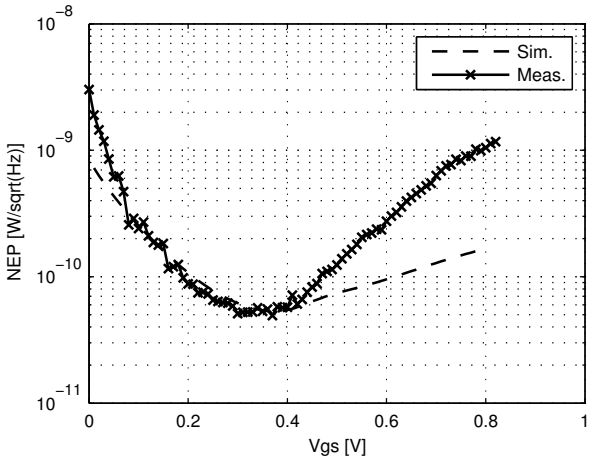

Fig. 6. Measured (crosses) and simulated (dashed line) noise-equivalent power (NEP) of a non-amplified pixel with the T1/T2 detector V_{gs} bias swept from 0 to 0.8 V. At $V_{gs} > 0.4$ V the measured signal approaches noise floor of the measurement setup, thus leading to an increased measured NEP in this region.

In Fig. 7 a transmission-mode image of polystyrene construction foam with an embedded cutter blade is shown. The scanned image was captured using a single 650-GHz pixel with an integrated amplifier. The transmission-mode imaging

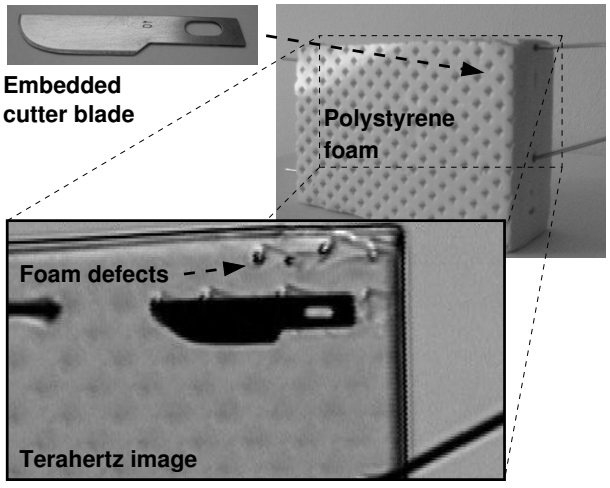

Fig. 7. A scanned transmission-mode image of a cutter blade embedded in polystyrene construction foam. The image was captured at 650 GHz using a pixel with an integrated pre-amplifier.

setup provides a 35-dB S_0/N ratio (no object in the beam) in a 1-Hz bandwidth, which is sufficient to resolve the structure of the foam as well as the presence of the metal cutter blade. The scanned image also reveals the cracks inside the polystyrene foam caused by the embedding of the blade. As these cracks are not obvious from the outside, it shows the capability of using the implemented terahertz detectors in industrial quality control and process monitoring without physical intrusion or contact to detect manufacturing defects and imperfections. Using an external pre-amplifier with a 6-nV/$\sqrt{\text{Hz}}$ input-referred noise, the measured S_0/N (1-Hz bandwidth) of the imaging setup could be improved to 57 dB.

VI. Conclusion

Terahertz pixels based on a 65-nm CMOS SOI technology have been presented. The results show a significantly improved detector responsivity and noise performance compared with the previously published 0.25 μm CMOS detectors presented in [3] and [7]. The SOI technology favours a back-side illumination through silicon lenses attached to the back-side of the chip, which leads to an improved antenna efficiency. Transmission-mode imaging of semi-transparent objects at 0.65 THz has finally demonstrated the potential of silicon high-resistivity SOI technologies for low-cost terahertz applications.

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