2013 IEEE Radio Frequency Integrated Circuits Symposium

Seattle, Washington, USA
2–4 June 2013

IEEE

PROGRAM

Washington State Convention Center

Sponsored by

IEEE Microwave Theory and Techniques Society
IEEE Electron Devices Society
and
IEEE Solid-State Circuits Society

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RFIC Plenary and Reception (Sunday Evening, 2 June 2013)

After a busy day of excellent RFIC Workshops see page (55–73) the Plenary Session and RFIC Reception will be held on Sunday evening – 2 June 2013. The Plenary Session starts at 18:00 in the Washington State Convention Center (WSCC), Level 6, Room 6B. The Plenary Session will include two outstanding speakers (see pages 8–9) and the Student Paper Awards ceremony. Immediately following the RFIC Plenary Session is the RFIC Reception in Room 6E. This social event is a key component of the RFIC Symposium, providing the opportunity to connect with old friends, make new acquaintances, and catch up on the latest news in the wireless industry. Admittance is included with the RFIC Symposium registration. Additional tickets can also be purchased separately at registration. The RFIC Reception is sponsored by the RFIC Steering Committee, and through generous gifts from our corporate sponsors including our inaugural Diamond Level (RFMD), Platinum Level (Sonnet Software), and Silver Level (Anadigics and Skyworks).

RFIC Symposium Activities (2–4 June 2013)

Saturday, 1 June 2013

14:00–18:00 Registration — WSCC South Lobby

Sunday, 2 June 2013

07:00–19:00 Registration — WSCC South Lobby
07:00–08:00 Speakers' Breakfast — WSCC 6A
07:00–08:00 Workshop Breakfast — WSCC 6th Floor, East & West Lobby Areas
08:00–17:00 Workshops and Tutorials — WSCC
12:00–13:30 Workshops Lunch — WSCC 6A
18:00–19:30 RFIC Plenary — WSCC 6BC
19:30–21:30 RFIC Reception — WSCC 6E

Monday, 3 June 2013

07:00–19:00 Registration — WSCC South Lobby
07:00–08:00 Speakers' Breakfast — WSCC 6A
08:00–09:40 RMO1A, RMO1C, RMO1D — WSCC
10:10–11:50 RMO2A, RMO2B, RMO2C, RMO2D — WSCC
12:00–13:15 RFIC Panel — WSCC 6BC
13:30–15:10 RMO3A, RMO3B, RMO3C — WSCC
15:40–17:20 RMO4A, RMO4C, RMO4D — WSCC

Tuesday, 4 June 2013

07:00–18:00 Registration — WSCC South Lobby
07:00–08:00 Speakers' Breakfast — WSCC 6A
08:00–09:40 RTU1B, RTU1C — WSCC
10:10–11:50 RTU2A, RTU2B, RTU2C, RTU2D — WSCC
12:00–13:30 RFIC Panel — WSCC 6A
13:30–17:00 Interactive Forum — WSCC 6E

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The RFIC Symposium will be held in Seattle, Washington at the Washington State Convention Center (WSCC) on 2–4 June 2013 in conjunction with the International Microwave Symposium. It opens Microwave Week 2013, the largest RF/Microwave meeting of the year. The RFIC Symposium brings focus to the technical accomplishments in RF systems, circuit device, and packaging technologies for mobile phones, wireless communication systems, broadband access modems, radar systems and intelligent transport systems.

Welcome Message from Chairpersons

Welcome to the 2013 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, which will take place in Seattle, WA, on 2–4 June 2013. Our Symposium is held in conjunction with the IEEE Microwave Theory and Technology Society's (MTT-S) International Microwave Symposium (IMS) and opens Microwave Week 2013, the largest worldwide RF/microwave meeting of the year, with three days focused exclusively on RFIC technology and innovation.

As in past years, the focus of the 2013 RFIC Symposium will be on emerging technologies and applications of Radio Frequency Integrated Circuits. This year, several forums will feature multiband reconfigurable, software-defined and cognitive radios, and the use of system-on-chips (SOCs) for realizing high data-rate, urban-environment, RF solutions for smart-phone, notepad, and notebook applications. The continued exploitation of frequencies above 60GHz in the realization of silicon millimeter wave circuits and systems will be presented throughout the conference. Lastly, the emergence of RF for biomedical applications and the reintroduction of wireline transceivers for high-speed I/O to our conference, reflect some of the exciting developments in the radio IC community. As in previous years, the latest advances in RFIC design from the device to the system level will be covered in various forums including workshops, panel sessions, and two exciting days of technical paper presentations.

The 2013 RFIC Symposium will open in grand style on Sunday, 2 June with a full lineup of 13 half-day and full-day workshops covering a wide array of topics with presentations from experts in their respective fields. This year's workshops will have a combination of tutorial and advanced presentations on some of the hottest topics in our community, including High-Efficiency Supply Modulated PAs, and Signal Generation at THz frequencies. The workshops will have a special full-day interactive Doherty tutorial workshop which will be offered with lab exercises where attendees can simulate (using ADS) designs and practice circuit concepts covered in the lecture, culminating in a complete high-power Doherty amplifier circuit design. One of the workshops, "Interference Robust Radio Receiver Techniques," focuses on the performance needs of modern integrated radios in an increasingly crowded spectrum. More advanced topics include SDR transmitters, the influence of MEMs on RF architectures, RF assisted Medicine, Self-Healing Circuits and Compensation, Near Field Communication, and VCO design in modern silicon processes. Other workshops will focus on the design of inductorless frontends, and how to push the RF performance limits in modern CMOS technologies.

The Plenary Session will be held on Sunday evening with keynote addresses given by two renowned industry leaders from the Pacific Northwest. They will share their insight on the direction of and challenges faced by the RFIC design community. The first speaker is Neville Ray, CTO of T-Mobile, who will discuss some of the exciting system developments from the cellular carrier perspective, with the talk, "*Wireless Spectrum Challenges & Opportunities: Maximizing Assets for Growth.*" The second speaker is Barrie Gilbert, ADI Fellow, who will share his insight on the history of RF and wireless transceivers and present his vision of the future of RFIC design. The title of his talk will be "*Microwave Technology: The First Century*." During the plenary session, students with outstanding contributions to the conference will be recognized with the three best paper awards. Immediately following the Plenary Session, conference attendees can gather at the RFIC Reception, which provides a relaxing time for all to mingle with old friends and catch up on the latest news.

The RFIC technical sub-committees were further re-organized this year to align with the dynamic trends in industry and academia. Technical papers will be presented during oral sessions throughout Monday and Tuesday morning, followed by an interactive poster forum in the afternoon.

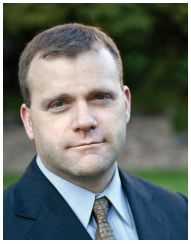
This session features papers presented in poster format, giving the attendee a chance to speak directly with the authors regarding their work.

On both Monday and Tuesday, the conference will feature lunchtime panel sessions that traditionally draw lively debates among the panelists and stimulating interaction with the attendees. The Monday panel session is titled "*Cellular vs. WiFi: Future Convergence or an Utter Divergence*" and will debate how much future high speed data will be shared between WiFi and cellular networks and the implication on IC design. The Tuesday panel session titled "*Universities are from Venus, Industries are from Mars,*" explores the diverging aspects of University–Industry research, resource, and educational needs. A panel of leading academics and industrialists will explore the shared needs and differences between the university and corporate world, as well as discuss improved interactive models to better serve both industry and academics.

Seattle is one of the most beautiful cities in North America with countless activities both within the city, and the immediate surrounding area. The conference will be held at the Washington State Convention Center in downtown Seattle, just a few minutes' walk from several local attractions. Conference attendees can enjoy a cup of coffee at the original Starbuck's, watch flying fish at the world-renowned Pike Place Market, or take a ride to the top of the city's iconic Space Needle. For the outdoor enthusiasts, several spectacular hiking trails can be found within an hour's drive of the downtown area.

On behalf of the RFIC Steering Committee, we would like to extend to all of you a warm welcome to this year's 2013 RFIC Symposium. We are looking forward to an exciting program and ask all of you to "come as you are," this June in Seattle!

We look forward to seeing you!



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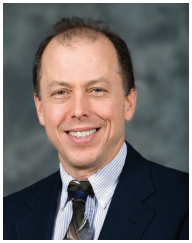

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RFIC 2013 Schedule

The RFIC Symposium will be held in Washington State Convention Center (WSCC).

Saturday, 1 June 2013

14:00–18:00 Registration — WSCC South Lobby

Sunday, 2 June 2013

07:00–19:00 Registration — WSCC South Lobby
07:00–08:00 Speakers' Breakfast — WSCC 6A
07:00–08:00 Workshop Breakfast — WSCC 6th Floor, East & West Lobby Areas
08:00–17:00 Workshops and Tutorials — WSCC
12:00–13:30 Workshops Lunch — WSCC 6A
18:00–19:30 RFIC Plenary — WSCC 6BC
19:30–21:30 RFIC Reception — WSCC 6E

Monday, 3 June 2013

07:00–19:00 Registration — WSCC South Lobby
07:00–08:00 Speakers' Breakfast — WSCC 6A
08:00–09:40 RMO1A: WSCC 618-620: *Low-Power Pulse-Based Radios*
RMO1C: WSCC 611-612: *Phase Noise Reduction Techniques*
RMO1D: WSCC 613-614: *Active and Passive Device Modeling for RFIC Applications*
09:40–10:10 Break
10:10–11:50 RMO2A: WSCC 618-620: *Low-Power Transceivers for Wireless Applications*
RMO2B: WSCC 615-617: *RF & mm-Wave Front-End Techniques*
RMO2C: WSCC 611-612: *Frequency Generation Circuits*
RMO2D: WSCC 613-614: *Mobile & Wireless Connectivity*
12:00–13:15 RFIC Panel — WSCC 6BC
13:00–14:30 RFIC Steering Committee Lunch Meeting — Sheraton Seattle Hotel: Redwood Room
13:30–15:10 RMO3A: WSCC 618-620: *Advances in RF Data Converter Circuits*
RMO3B: WSCC 615-617: *RF LNAs and RF Rectifiers*
RMO3C: WSCC 611-612: *Wideband VCO Circuits and Architectures*
15:10–15:40 Coffee Break
15:40–17:20 RMO4A: WSCC 618-620: *Baseband Circuits and Modulators/Demodulators*
RMO4C: WSCC 611-612: *Reactively-Coupled Oscillators*
RMO4D: WSCC 613-614: *High-Speed Data Transceiver Circuits*
17:30–19:00 International Microwave Symposium Plenary Session — WSCC 6BC

Tuesday, 4 June 2013

07:00–18:00 Registration — WSCC South Lobby
07:00–08:00 Speakers' Breakfast — WSCC 6A
08:00–09:40 RTU1B: WSCC 615-617: *mm-Wave Power Amplifiers*
RTU1C: WSCC 611-612: *Millimeter and Sub-Millimeter Wave Transceivers*
09:40–10:10 Break
10:10–11:50 RTU2A: WSCC 618-620: *Reconfigurable and Software-Defined Radio Front-End Techniques*
RTU2B: WSCC 615-617: *Efficiency and Linearity Enhancement for RF/MW Power Amplifiers*
RTU2C: WSCC 611-612: *Millimeter-Wave Beamforming and Power Combining Techniques*
RTU2D: WSCC 613-614: *Advanced Silicon Devices for High Speed, High Power, ESD and MEMS Applications*
12:00–13:30 RFIC Panel — WSCC 6A
13:00–14:30 RFIC TPC Lunch Meeting — Sheraton Seattle Hotel: Redwood Room
13:30–17:00 Interactive Forum — WSCC 6E

Plenary Session Schedule

Sunday, 2 June 2013

18:00
Washington State Convention Center (WSCC) – Room 6BC
RFIC Plenary

Chair: Jacques C. Rudell, University of Washington

Co-Chair: Lawrence Kushner, BAE Systems

Co-Chair: Bertan Bakkaloglu, Arizona State University

18:00 Welcome Message from General and TPC Chairs, Student Paper Awards

18:30 RSU5A-1
Wireless Spectrum Challenges & Opportunities: Maximizing Assets for Growth
Neville Ray, T-Mobile

19:00 RSU5A-2
Microwave Technologies: The First Century
Barrie Gilbert, Analog Devices Inc.

19:30
Washington State Convention Center (WSCC) – Room 6E
RFIC Reception

Plenary Speaker 1

Neville Ray
CTO and Executive Vice President
T-Mobile

Wireless Spectrum Challenges & Opportunities: Maximizing Assets for Growth

Abstract: In an industry needing to support phenomenal growth, spectrum is key. Networks and devices must support multiple technologies and frequency bands without sacrificing performance. The industry has to come together to provide innovative and cost-effective RFIC design that utilizes all available resources.

Smarter utilization of industry assets is essential, for example building small cell solutions (HetNets) that include tighter integration and interworking between cellular and WiFi. Since unlicensed spectrum is a great augment to carriers' licensed spectrum assets, it opens a myriad of opportunities for increasing network capacity. Better integration between WiFi and cellular would allow customers greater capacity and flexibility with data transmissions based on cost or desired quality level and network load. Therefore, RFIC innovation is necessary for future wireless systems.

About Neville Ray

Neville Ray serves as chief technology officer for T-Mobile USA. He is responsible for the national management and ongoing development of the T-Mobile USA national wireless network and the company's IT services and operations. He joined the company (then Voicestream) in 2000.

Mr. Ray serves as the Chairperson of 4G Americas, an organization with a mission to promote deployment throughout the Americas of the 3GPP family of technologies, including HSPA, HSPA+ and LTE.

Prior to T-Mobile, Ray was vice president of network operations at Pacific Bell Mobile Services in California. His previous experience includes the design and deployment of cellular, microwave and broadcast telecommunications systems in Europe, the Middle East, Africa and the Far East.

Mr. Ray is an honors graduate of City University, London, UK and a member of the Institution of Electrical and Electronic Engineers and the Institution of Civil Engineers.

Plenary Speaker 2

Barrie Gilbert
ADI and IEEE Life Fellow
Analog Devices Inc.

Microwave Technologies: The First Century

Abstract: The talk describes the history of microwave technologies, reaching back to the late 1800s, a time of experimentation with spark-gaps and waveguides up to 60GHz. Marconi and Hertz also investigated this regime, but turned their attention to low frequencies. For decades crude galena rectifiers were used for detectors, setting the stage for the later development of semiconductor diodes. The triode tube was a great leap for radio, but not as a source of microwave power, due to its long transit times. The 1920 Barkhausen-Kurz oscillator made use of this transit time to generate frequencies up to 700MHz.

Once the idea of exploiting transit times was out of the box, the majority of microwave power sources for the next several decades were based on such methods and some invoked the use of crossed magnetic and electric fields. The cavity magnetron, today found in every home, was invented in 1937 by Boot and Randall at Birmingham University in England. It possessed the astonishing ability to instantly convert simple DC power into RF power in the centimetre range of wavelengths with hitherto unimaginable efficiency. It was followed by a rash of amazing electron tubes with mysterious names: the klystron, twystron, dematron, amplitron, and the scary-sounding carcinotron. Later semiconductor devices would generate their own list of odd abbreviated names: BARRIT, TED, IMPATT, TRAPATT and LSA.

The commercialization of radio communication systems has led to a greater emphasis on two imperatives: very high performance, and extremely low cost. Modern microwave technologies have moved into a new commodity phase, like plastics or steel. However, it is safe to say "You ain't seen nuthin' yet!"

About Barrie Gilbert

Barrie Gilbert (IEEE Life Fellow) has had a severely limited life experience. He has spent all of it doing nothing but dabbling in analog circuits, more or less seriously, dipping his toes into inhospitable digital waters only rarely. He has contributed several seminal cells, and terms, now in common use across the industry. Of especial value has been the concept of translinear cells, allowing algebraic functions to be accurately implemented with great elegance and efficiency. After a long career in both the UK and the US, he founded the first remote design center of Analog Devices Inc., in 1972, later re-located from England to Beaverton, Oregon, and now directs most affairs there, as a freewheeling inventor of new product concepts, urging his team members to follow their instincts. He has received 100+ patents worldwide and a number of IEEE and industry awards. In 1990, he was elected as Oregon Researcher of the Year, and awarded an Honorary Doctorate from Oregon State University in 1997. He was inducted into the National Academy of Engineering in 2009.

Monday, 3 June 2013
08:00–09:40
Room 618-620
Session RMO1A: Low-Power Pulse-Based Radios
Chair: Gernot Hueber, NXP Semiconductors
Co-Chair: Pedram Mohseni, Case Western Reserve University

RMO1A-1 08:00
A High-Resolution Short-Range CMOS Impulse Radar for Human Walk Tracking

Piljae Park, Sungdo Kim, Sungchul Woo, Cheonsoo Kim; ETRI, Korea

Abstract: A single-chip impulse radar transceiver is presented. A high-resolution, enhanced SNR and controllability are achieved with a proposed architecture. By controlling timing between the transmit (TX) pulse and sampling clock of the receiver, echo pulses from targets are received and recovered. The TX pulse can adjust its spectrum occupancy by changing impulse shape. The 4-channel sampling receiver consists of a low noise amplifier, track and hold samplers, integrators, and a cascaded triple delay locked loop. The embedded control logic allows the radar to enhance the SNR of the received pulse using an averaging technique, and to operate at multiple reception modes.

The real-time radar system measurements show that echo pulses are recovered with ≥100-psec range resolution while consuming 80 mW from 1.2-V of V_{dd}. An indoor human walking trace is successfully recorded. The transceiver is fabricated in a 130-nm CMOS technology occupying chip area of 3.4 mm^2.

RMO1A-2 08:20
An All-Digital IR-UWB Transmitter with a Waveform-Synthesis Pulse Generator in 90nm CMOS for High-Density Brain Monitoring

Ali Ebrazeh, Pedram Mohseni; Case Western Reserve University, USA

Abstract: This paper reports an all-digital impulse radio ultra wideband transmitter (IR-UWB TX) fabricated in 90-nm CMOS, which incorporates a waveform-synthesis pulse generator and a timing generator for OOK/PPM pulse modulation and scrambling. The UWB pulse generator includes ten identical taps, each comprising an impulse generator and an output driver. Upon triggering by the timing generator, these taps create a programmable number of individual lobes with 4b control over their duration and amplitude, which are then combined at a shared output node to generate the UWB pulse. With a high-performance receiver, the TX might be used for moderate-data-rate (<50Mbps), m-range telemetry, suitable for brain-behavior studies, with energy consumption in the range of 12 to 20pJ/pulse, and for high-data-rate (>100Mbps), cm-range telemetry, suitable for brain-machine interfaces, with energy consumption in the range of 3.6 to 6pJ/pulse from 1.2V.

RMO1A-3 08:40

A 0.32nJ/bit Noncoherent UWB Impulse Radio Transceiver with Baseband Synchronization and a Fully Digital Transmitter

Ashutosh Mehra[1], Martin Sturm[1], Dan Hedin[2], Ramesh Harjani[1]; [1]University of Minnesota, USA, [2]Advanced Medical Electronics, USA

Abstract: This paper presents a low-power noncoherent ultrawideband (UWB) impulse-radio (IR) transceiver operating at 5GHz in 0.13-μm CMOS. The super-regenerative amplifier (SRA) based energy-detection receiver utilizes early/late detection for a two-step baseband synchronization algorithm. A fully-digital transmitter generates a shaped output pulse of 1GHz 3-dB bandwidth. DLLs provide a PVT-tolerant time-step resolution of 1ns over the entire symbol period and regulate the pulse generator center frequency. Measured results show a receiver efficiency of 0.32nJ/bit at 20.8Mb/s and operation with inputs as low as -70dBm. The transmitter outputs -31dBm (0.88pJ/pulse at 1Mpulse/s) with a dynamic (energy) efficiency of 16pJ/pulse.

RMO1A-4 09:00

A 0.7V Intermittently Operating LNA with Optimal On-Time Controller for Pulse-Based Inductive-Coupling Transceiver

Teruo Jyo, Tadahiro Kuroda, Hiroki Ishikuro; Keio University, Japan

Abstract: This paper presents a low-power LNA for a inductive-coupling transceiver. Intermittently operating technique to turn on LNA only at the moment when the pulse signal appears is used to reduce power consumption. To optimally control the On-time of LNA, pulse width detector based on self-oversampling TDC is used and compensate the PVT variations of On-time width and of pulse signal width. The fabricated test chip in 65nm CMOS occupies 0.06mm^2 and achieved the intermittently operating frequency at the range from 60 to 400Mbps. The power consumption is 0.42mW at 400Mbps and the supply voltage of 0.7V which corresponds to 37% power reduction from the power consumption without optimal On-Time Controller.

Monday, 3 June 2013
08:00–09:40
Room 611-612
Session RMO1C: Phase Noise Reduction Techniques
Chair: Timothy M. Hancock, MIT Lincoln Laboratory
Co-Chair: Kamran Entesari, Texas A&M University

RMO1C-1 08:00
A Wideband Voltage-Biased LC Oscillator with Reduced Flicker Noise Up-Conversion

F. Pepe, A. Bonfanti, S. Levantino, C. Samori, A.L. Lacaita; Politecnico di Milano, Italy

Abstract: The demand of voltage-controlled oscillators (VCOs) with a broad tuning range can lead to unacceptable degradation of the $1/f^3$ phase-noise component if traditional voltage-biased topologies are implemented. In this paper, a novel VCO architecture is proposed, where a segmented transconductor tailors the negative g_m depending on the operating range to ensure that flicker-noise up-conversion remains minimal. The implemented oscillator covers both 4G and WiMAX 2.5-GHz operation modes and achieves a 10-dB reduction of the $1/f^3$ phase noise without impairing the $1/f^2$ phase-noise performance.

RMO1C-2 08:20
A 220dB FOM, 1.9GHz Oscillator Using a Phase Noise Reduction Technique for High-Q Oscillators

Kannan Sankaragomathi[1], Lori Callaghan[2], Richard Ruby[2], Brian Otis[1]; [1]University of Washington, USA, [2]Avago Technologies, USA

Abstract: We present a technique to reduce the close-in phase noise of high-Q (FBAR/MEMS/crystal) oscillators. The proposed technique suppresses the up-conversion of 1/f noise via AM-PM conversion by the addition of a non-linear capacitor to the tank. The proposed AM-PM suppression technique has no additional power penalty and incurs a minimal area penalty. Measurements from multiple dies of a 1.9GHZ FBAR oscillator show ≥3.5dB reduction in close-in phase noise using the proposed technique. The FBAR oscillator achieves a measured phase noise of -88dBc/Hz @ 1kHz, -116dBc/Hz @10kHz, -146dBc/Hz @ 1MHz offsets. The oscillator with the proposed technique achieves a Figure of Merit (FOM) of 220dB, which is 5.5dB better than the FBAR oscillator with lowest close-in phase noise reported to date [1].

RMO1C-3 08:40
A Current-Reuse Class-C LC-VCO with an Adaptive Bias Scheme

Teerachot Siriburanon, Wei Deng, Kenichi Okada, Akira Matsuzawa; Tokyo Institute of Technology, Japan

Abstract: This paper proposes a low-power current-reuse complementary differential LC-VCO which is composed of a pair of NMOS and PMOS transistors with an adaptive bias scheme for both transistors to ensure its robust startup and achieve maximum swing in Class-C operation. The proposed VCO has been implemented in a standard 0.18μm CMOS technology, which oscillates at the carrier frequency

of 4.6 GHz. The measured phase noise is -139.5dBc/Hz at 10 MHz offset while drawing a current consumption of 1.6 mA from 1.5 V supply. The Figure of Merit is -189.1 dBc/Hz. To the author's best knowledge, this is the first class-C current-reuse VCO with an adaptive bias scheme.

RMO1C-4 09:00

A 0.5V, 2.41GHz, 196.3dBc/Hz FoM Differential Colpitts VCO with an Output Voltage Swing Exceeding Supply and Ground Potential Requiring No Additional Inductor

Joo-Myoung Kim, Seong Joong Kim, Seok-Kyun Han, Sang-Gug Lee; KAIST, Korea

Abstract: A low-voltage differential Colpitts VCO that achieves an output voltage swing above the supply voltage and below the ground potential to improve the phase noise while requiring no additional inductor for a small chip area is proposed. Implemented in a 65nm CMOS process, the proposed VCO achieves the phase noise of -131.05dBc/Hz at an offset of 1MHz from an oscillation frequency of 2.41GHz and a FoM of 196.3dBc/Hz while dissipating 1.74mW from a 0.5V supply.

RMO1C-5 09:20

Ultra-Low Phase Noise 7.2–8.7GHz Clip-and-Restore Oscillator with 191dBc/Hz FoM

Masoud Babaie[1], Akshay Visweswaran[1], Zhuobiao He[2], Robert Bogdan Staszewski[1]; [1]Technische Universiteit Delft, The Netherlands, [2]HiSilicon, China

Abstract: In this paper we investigate benefits of a recently introduced clip-and-restore (C&R) oscillator for ultra-low phase noise RF applications and reconsider the original choices in light of further insight into the oscillator behavior. We also tackle undesired resonance frequencies and exploit them to facilitate clipping with proper choices of tuning capacitances. Based on the new theory, the proposed oscillator was implemented in 65-nm CMOS and verified to achieve 4 dB better phase noise and 1.8 dB better FoM than the original C&R oscillator, thus making it the lowest phase noise CMOS oscillator ever published. The measured phase noise is -145 dBc/Hz at a 3 MHz offset from a 4.2 GHz carrier. The resulting average FoM is 191 dBc/Hz and varies less than 2 dB across the tuning range. It covers the 7.2–8.7 GHz frequency band for a 19% tuning range, drawing 32 mA from a 1.3 V power supply.

Monday, 3 June 2013
08:00–09:40
Room 613-614
Session RMO1D: Active and Passive Device Modeling for RFIC Applications

Chair: Francis Rotella, Peregrine Semiconductor
Co-Chair: Harish Krishnaswamy, Columbia University

RMO1D-1 08:00
HF Mismatch Characterization and Modeling of Bipolar Transistors for RFIC Design

Tzung-Yin Lee, Yuh-Yue Chen; Skyworks Solutions Inc., USA

Abstract: This paper presents a methodology to characterize and model BJT's mismatch behavior for RFIC design. A measurement technique based on the conventional S-parameter measurement is developed to measure the mismatch behavior at high frequencies (HFs). First, besides the typical de-embedding, the bondpad mismatch is subtracted statistically from the capacitance mismatch measurement. Second, a semi-empirical methodology using physical parameters, such as window CD and vertical doping, is developed to model the measured AC mismatch behavior for transistors of different size. Finally, a systematic procedure is proposed to extract the mismatch parameters, which can be used in the SPICE Monte-Carlo mismatch simulation. The proposed mismatch modeling methodology is validated on an industrial 0.35μm RF BiCMOS process. The proposed model fits the mismatch characteristics of the key AC parameters, such as C_{BE}, C_{BC}, and f_T at different current densities. The model also scales well with geometry for the transistors with sizes useful for RFIC application.

RMO1D-2 08:20
CMOS RF Noise, Scaling, and Compact Modeling for RFIC Design

Angelos Antonopoulos[1], Matthias Bucher[1], Konstantinos Papathanasiou[1], Nikolaos Makris[1], Rupendra K. Sharma[1], Paulius Sakalas[2], Michael Schroter[2]; [1]Technical University of Crete, Greece, [2]Technische Universität Dresden, Germany

Abstract: This work presents an analysis of high frequency noise and linearity performance of a 90 nm CMOS process. Measurements are performed for a wide range of nominal gate lengths and bias points at high frequency. Modeling is based on the EKV3 compact model in Spectre RF circuit simulator from Cadence. The model shows correct scalability for noise and linearity accounting for short channel effects (SCEs), such as velocity saturation (VS) and channel length modulation (CLM). Results are presented versus a common measure of channel inversion level, named inversion coefficient. Optimum performance is shown to gradually shift from higher to lower levels of moderate inversion, when scaling from 240 nm to 100 nm. The same trend is observed from investigating the transconductance frequency product (TFP) of a common-source (CS) LNA for technology nodes ranging from 180 nm to 22 nm.

RMO1D-3 08:40

An Automatic Parameter Extraction and Scalable Modeling Method for Transformers in RF Circuit

Jian Yao, Zuochang Ye, Yan Wang; Tsinghua University, China

Abstract: In this paper, an automatic parameter extraction and scalable modeling method for transformer with 2π-based equivalent circuit-topology is established for the first time. In contrast to traditional optimization extraction, the adaptive boundary compression technique, combining a new correlated parameter extraction method with the neighboring geometry parameters, is introduced. The method is validated by 42 industry transformers and both accuracy and scalability have been achieved.

RMO1D-4 09:00

A 12ps True-Time-Delay Phase Shifter with 6.6% Delay Variation at 20–40GHz

Qian Ma, Domine M.W. Leenaerts, R. Mahmoudi; Technische Universiteit Eindhoven, The Netherlands

Abstract: A fully integrated 2-channel Ka-band True Time Delay (TTD) phase shifter with 12ps continuous changing delay time has been realized in a 0.25μm SiGe:C BiCMOS technology. A delay variation cancellation technique is proposed, resulting in less than 0.8ps delay variation over a 20–40GHz frequency span, meanwhile maintaining a constant input impedance. In the high (low) power mode, the measured input 1dB compression point and input IP3 are +9.7dBm (+3.6dBm) and +18dBm (+13dBm) at 30GHz with an averaged power consumption per channel of 145mW (33mW) for the same TTD performance. The size of the core phase shifter is less than 0.1mm^2.

Monday, 3 June 2013
10:10–11:50
Room 618-620
Session RMO2A: Low-Power Transceivers for Wireless Applications
Chair: Li-Wu Yang, Shanghai Jiao Tong University
Co-Chair: Jenshan Lin, University of Florida

RMO2A-1 10:10
A PLL-Based BFSK Transmitter with Reconfigurable and PVT-Tolerant Class-C PA for MedRadio & ISM (433MHz) Standards

Karthik Natarajan, Daibashish Gangopadhyay, David Allstot; University of Washington, USA

Abstract: An RF transmitter that uses closed-loop PLL-based BFSK modulation and is reconfigurable for both the MedRadio (402–405MHz) and 433 MHz ISM bands is introduced. Innovations include the first reconfigurable class-C PA, the first class-C PA with automatic calibration against PVT variations, and a low-power NMOS delay-based ring-VCO PLL. Several performance records are achieved: (1) The PA realizes a peak efficiency of 47% in the high-power (ISM) (-2 dBm) mode and 43% (33%) in the MedRadio -12 dBm (-16 dBm backoff) modes. (2) The PLL dissipates only 72 μW with a phase noise of -111 dBc/Hz @ 1 MHz, and (3) the overall transmit efficiencies are 29% and 17% for the -12 dBm and -16 dBm backoff levels for the MedRadio band and 44% for the ISM (433 MHz) bands.

RMO2A-2 10:30
A Low Power Miniaturized 1.95mm² Fully Integrated Transceiver with fastPLL Mode for IEEE 802.15.4 / Bluetooth Smart and Proprietary 2.4GHz Applications

Franz Pengg, David Barras, Martin Kucera, Nicola Scolari, Alexandre Vouilloz; CSEM, Switzerland

Abstract: This paper presents an ultra-low power miniaturized single chip transceiver operating in the ISM band at 2.4GHz. Targeting low power and minimum die size, while excluding RF-options and minimizing the count of external components for low-cost, asks for appropriate architectural choices to obtain high performance. Fast PLL locking and immediate RX-TX turnaround minimize the consumption overhead at wake-up and turnaround. With a die size of only 1.95mm² in a 90nm standard digital CMOS technology, the receiver achieves a sensitivity of -94.5dBm (1Mbps, BER 10E-3) while consuming only 7.1mA and the transmitter consumes 9.2mA for 0dBm output power. The base-band is compliant with the IEEE 802.15.4 standard, the Bluetooth Smart standard (former Bluetooth low energy BLE) and can be configured for proprietary standards at 2.4GHz, with data-rates up to 3Mbps.

RMO2A-3 10:50
A 1.9nJ/bit, 5Mbps Multi-Standard ISM Band Wireless Transmitter Using Fully Digital PLL

Sudipto Chakraborty[1], Viral Parikh[1], Swaminathan Sankaran[1], Tomas Motos[1], Indu Prathapan[1], Krishnaswamy Nagaraj[1], Frank Zhang[2], Oddgeir Fikstvedt[1], Ryan Smith[1], Srividya Sundar[1], Danielle Griffith[1], Patrick Cruise[1]; [1]Texas Instruments Incorporated, USA, [2]NVIDIA Incorporated, USA

Abstract: This paper presents an energy efficient transmitter for multi-standard applications (IEEE802.15.4, BLE, 5Mbps) in ISM2.4GHz band. It incorporates a fully digital PLL with two point modulation to achieve up to 5Mbps data rate at 9.5mW power consumption (including all power management blocks) at 0dBm output power, leading to 1.9nJ/b efficiency. The proposed digital PLL uses a counter based area and power efficient re-circulating TDC, current reuse low area DCO using resistive tail, process compensated high speed divider, class-AB PA stages, and fully integrated on-chip LDOs. The entire transmitter occupies 0.35mm^2 Silicon area in a 65nm digital CMOS process.

RMO2A-4 11:10

A Sub-GHz Low-Power Wireless Sensor Node with Remote Power-Up Receiver

Jaesik Lee[1], Inseop Lee[1], Jubong Park[2], Junho Moon[2], Seungsoo Kim[2], Jaeyoung Lee[2]; [1]Navitas Solutions, USA, [2]Navitas Solutions, Korea

Abstract: A fully integrated low-power sub-GHz sensor node is presented for wireless sensor networks (WSN). The sensor node features a sensor IC and a RF transceiver IC, vertically assembled in a single QFN package. A unique remote power-up scheme is configured to supply the power to a sensor node from power-down state. It features a technique of centralized remote power-up scheme combined with local broadcasting power-up sequence to achieve ultra-low standby current, fast power-up time, and extended coverage. It proposes a time division switch to separate power-up message from data information, both propagated at the same frequency band. The standby current in power-down state draws less than 450nA. The sensitivity of power-up receiver is -24dBm, while the sensitivity of data receiver is -103dBm. The Sensor and RF transceiver ICs were fabricated in 0.25μm CMOS and 0.18μm RF CMOS, respectively.

Monday, 3 June 2013
10:10–11:50
Room 615-617
Session RMO2B: RF & mm-Wave Front-End Techniques
Chair: Osama Shana'a, MediaTek
Co-Chair: Marc Tiebout, Infineon Technologies

RMO2B-1 10:10
A Receiver with In-Band IIP_3>20dBm, Exploiting Cancelling of OpAmp Finite-Gain-Induced Distortion via Negative Conductance

Dlovan H. Mahrof, Eric A.M. Klumperink, Mark S. Oude Alink, Bram Nauta; University of Twente, The Netherlands

Abstract: Highly linear CMOS radio receivers increasingly exploit linear RF V-I conversion and passive down-mixing, followed by an OpAmp based Transimpedance Amplifier at baseband. Due to the finite OpAmp gain in wideband receivers operating with large signals, virtual ground is imperfect, inducing distortion currents. We propose to apply a negative conductance to cancel this distortion. In an RF receiver, this increases In-Band IIP_3 from 9dBm to >20dBm, at the cost of 1.5dB extra NF and <10% power penalty. In 1MHz bandwidth, a Spurious-Free Dynamic Range of 85dB is achieved at <27mA up to 2GHz for 1.2V supply voltage.

RMO2B-2 10:30
A Current-Mode mm-Wave Direct-Conversion Receiver with 7.5GHz Bandwidth, 3.8dB Minimum Noise-Figure and +1dBm $P_{1dB,out}$ Linearity for High Data Rate Communications

Hao Wu[1], Ning-Yi Wang[2], Yuan Du[1], Yen-Cheng Kuan[1], Frank Hsiao[1], Sheau-Jiung Lee[1], Ming-Hsien Tsai[3], Chewn-Pu Jou[3], Mau-Chung Frank Chang[1]; [1]University of California at Los Angeles, USA, [2]Broadcom, USA, [3]TSMC, Taiwan

Abstract: A current-mode mm-wave direct-conversion receiver breaking trade-offs among bandwidth, NF and linearity is designed and realized in 65nm CMOS. The 60GHz receiver employs novel Frequency-staggered Series Resonance Common Source (FSRCS) stage to extend RF bandwidth with superior noise performance. The receiver's current-mode operation offers excellent out-of-band blocker tolerance and linearity. With on-chip quadrature LO generations, the fabricated receiver simultaneously achieves minimal noise figure of 3.8dB, RF bandwidth of 7.5GHz, output P1dB of 1dBm, maximum conversion gain of 32dB, and IRR of -35dB. The receiver is capable of tolerating out-of-channel blocker up to -9dBm at 3.5GHz away. It occupies silicon area of 1.3mm^2 and draws 25.5mA from 1V supply.

RMO2B-3 10:50
Co-Design of 60GHz Wideband Front-End IC with On-Chip Tx/Rx Switch Based on Passive Macro-Modeling

Lixue Kuang[1], Baoyong Chi[1], Haikun Jia[1], Zuochang Ye[1], Wen Jia[2], Zhihua Wang[1]; [1]Tsinghua University, China, [2]RITS, China

Abstract: Co-design of 60GHz wideband front-end IC with on-chip Tx/Rx switch in 65nm CMOS is presented. Passive macro-modeling (pmm) is utilized to convert S-parameter files from passive component EM simulations to state-space models in circuit netlist format which could be used in commercial SPICE simulator for various analyses without convergence issues. The co-design of on-chip switch and LNA/PA could achieve wideband matching and reduce the effects of insertion loss of on-chip Tx/Rx switch. Combining with gain boosting technique in LNA design and lumped-component based design methodology, the implemented 60GHz front-end IC with on-chip Tx/Rx switch achieves 3dB gain bandwidth of 12GHz with maximum gain 17.8dB and minimum NF 5.6dB in Rx mode and 3dB gain bandwidth of 10GHz with saturated output power 5.6dBm in Tx mode, and only consumes 1.0mm×1.2mm die area (including pads).

RMO2B-4 11:10

A 0.18-μm CMOS Fully Integrated Antenna Pulse Transceiver with Leakage-Cancellation Technique for Wide-Band Microwave Range Sensing Radar

Nguyen Ngoc Mai Khanh, Kunihiro Asada; University of Tokyo, Japan

Abstract: This paper presents a leakage cancellation technique for on-chip transceiver for range sensing radar. A 180-nm CMOS transceiver with on-chip antennas is implemented with a 9–11-GHz damping-pulse transmitter (Tx) and a receiver (Rx) including a mixer and a 3-stage low-noise amplifier (LNA). By adding a polarity-reversal switch to the receiver mixer, leakage, reflected signals, and traveling time of transmitted pulses can be measured. Another improvement is the design of the Rx's mixer and the 3-stage wide-band LNA to reduce on-chip DC blocking capacitors. Experimental results with/without reflector placed at several distances from the transceiver are performed to demonstrate the technique. Pulse traveling times are measured with 0.8 ns, 1 ns, and 1.25 ns for the distance of 10 cm, 14 cm, and 18 cm, respectively. Furthermore, reflected signals are measured separately from leakage in cases of different distances.

RMO2B-5 11:30

245GHz Subharmonic Receivers in SiGe

Yanfei Mao[1], K. Schmalz[1], J. Borngräber[1], J. Christoph Scheytt[2], Chafik Meliani[1]; [1]IHP, Germany, [2]Universität Paderborn, Germany

Abstract: Two subharmonic receivers for 245 GHz spectroscopy sensor applications in the 245 GHz ISM band have been proposed. One receiver consists of an 2nd APDP (antiparallel diode pair) passive SHM (subharmonic mixer), a 120 GHz push-push VCO with 1/64 divider, and a 120 GHz PA (power amplifier). The other consists of a single-ended four-stage CB (common base) LNA, an 2nd APDP passive SHM, an IF amplifier, a 120 GHz push-push VCO with 1/64 divider, and a 120 GHz PA. The receivers are fabricated in a SiGe:C BiCMOS technology with f_T/f_{max}=300/500 GHz. The measured conversion gain are -17 dB rsp. 10.6 dB at 245 GHz with 3-dB bandwidths of 13 GHz rsp. 14 GHz, and the single-side band noise figure are 17 dB rsp. 20 dB; the two receivers dissipates a power of 213 mW and 312 mW, respectively.

Monday, 3 June 2013
10:10–11:50
Room 611-612
Session RMO2C: Frequency Generation Circuits
Chair: Jaber Khoja, Qualcomm
Co-Chair: Chun-Ming Hsu, IBM

RMO2C-1 10:10
A mm-Wave FMCW Radar Transmitter Based on a Multirate ADPLL
Wanghua Wu[1], Xuefei Bai[2], Robert Bogdan Staszewski[1], John R. Long[1]; [1]Technische Universiteit Delft, The Netherlands, [2]USTC, China

Abstract: We present a 60-GHz FMCW radar transmitter based on an all-digital phase-locked loop (ADPLL) with ultra-wide linear frequency modulation. Multirate, two-point modulation generates an ultra-linear programmable frequency ramp. A novel, closed-loop DCO gain linearization method employing 24kb of SRAM realizes a GHz-level triangular chirp with high sweep linearity, and enables hitless modulation through multiple DCO tuning banks. Measured frequency error (i.e., nonlinearity) in the FMCW ramp is only 117-kHz_{rms} for a 62-GHz carrier with 1.22-GHz bandwidth. The synthesizer is transformer-coupled to a 3-stage neutralized power amplifier that delivers +5 dBm to a 50-Ω load. Implemented in 65-nm CMOS, the transmitter prototype consumes 89 mW from a 1.2-V supply.

RMO2C-2 10:30
A 440-μW 60-GHz Injection-Locked Frequency Divider in 65nm CMOS
Yue Chao, Howard C. Luong; HKUST, China

Abstract: An ultra-low-power millimeter-wave injection-locked frequency divider (ILFD) based on transformer-feedback and transformer-distribution technique is proposed to operate with a very small injection signal. The proposed ILFD measures a locking range from 60.9GHz to 64.7GHz with -7dBm input power while consuming 440μW, which features the minimum power consumption among all the reported V-band frequency dividers. An interesting injection-saturation phenomenon is also identified and verified by measurement results.

RMO2C-3 10:50
An Automatically Placed-and-Routed ADPLL for the MedRadio Band Using PWM to Enhance DCO Resolution
Muhammad Faisal, David D. Wentzloff; University of Michigan, USA

Abstract: An all-digital phase-locked loop for the MedRadio bands is presented. This ring oscillator based ADPLL was entirely designed and placed-and-routed using digital design flows and was fabricated in a 65 nm CMOS process. Pulse width modulation of the DCO control signals is introduced as a technique to improve the resolution of the DCO to 59 kHz/LSB. This ADPLL operates as a subsampling integer-N frequency synthesizer from 400 to 460 MHz, and consumes 2.1 mA from a 1 V supply, with an rms jitter of 13.3 ps.

RMO2C-4 11:10

A 2.4-GHz Low Power High Performance Frequency Synthesizer Based on Current-Reuse VCO and Symmetric Charge Pump

Ye Zhang, Lei Liao, Muh-Dey Wei, Jan Henning Mueller, Bastian Mohr, Aytac Atac, Yifan Wang, Martin Schleyer, Ralf Wunderlich, Renato Negra, Stefan Heinen; RWTH Aachen University, Germany

Abstract: This paper presents a low power high performance frequency synthesizer. Based on the current-reuse VCO architecture, the whole system power consumption is significantly saved with excellent phase noise performance. Imbalance amplitude problems caused by the unsymmetrical VCO are solved by the pre-tuning mechanism, which automatically chooses the correct frequency band for the certain frequency channel. Besides, the symmetric charge pump (CP) can minimize the current mismatches and phase offset. The frequency synthesizer is fully integrated in 130-nm CMOS technology consuming 5.8mW. Measurement results show performance of -130 dBc/Hz at 1MHz offset phase noise, 450 fs rms jitter. The reference spur is below -75 dB, and it operates successfully with 1 Mbps GFSK signals as the two-point modulated transmitter.

RMO2C-5 11:30

A 73.9–83.5GHz Synthesizer with -111dBc/Hz Phase Noise at 10MHz Offset in a 130nm SiGe BiCMOS Technology

J.-O. Plouchart, Mark Ferriss, Bodhisatwa Sadhu, Mihai Sanduleanu, Benjamin Parker, Scott Reynolds; IBM, USA

Abstract: A 73.9–83.5 GHz synthesizer is implemented in a 130nm SiGe BiCMOS technology. The measured phase noise at 10KHz and 10MHz offset of the 82.4GHz carrier are -88.5dBc/Hz and -111dBc/Hz respectively. Reference spurs are -67 dBc. The synthesizer integrates voltage regulators and power management for SoC applications; it consumes 0.51 W from 1.5 V and 2.7 V supplies, and occupies 0.85 mm × 2.9 mm.

Monday, 3 June 2013
10:10–11:50
Room 613-614
Session RMO2D: Mobile & Wireless Connectivity
Chair: Julian Tham, Broadcom
Co-Chair: Li Lin, Marvell Semiconductor

RMO2D-1 10:10
A 60nm WiFi/BT/GPS/FM Combo Connectivity SOC with Integrated Power Amplifiers, Virtual SP3T Switch, and Merged WiFi-BT Transceiver

Chia-Hsin Wu[1], Tsung-Ming Chen[1], Wei-Kai Hong[1], Chih-Hsien Shen[1], Jui-Lin Hsu[1], Jen-Che Tsai[1], Kuo-Hao Chen[1], Yi-An Li[1], Sheng-Hao Chen[1], Chun-Hao Liao[1], Hung-Pin Ma[1], Hui-Hsien Liu[1], Min-Shun Hsu[1], Sheng-Yuan Su[1], Albert Jerng[2], George Chien[2]; [1]MediaTek, Taiwan, [2]MediaTek, USA

Abstract: A highly integrated WiFi/BT/FM/GPS connectivity combo SOC is implemented in a 60nm CMOS process. This work presents the proposed WiFi/BT merged RF transceiver, a virtual SP3T switch, and DPD algorithm to save chip area, reduce BOM and enhance performance simultaneously. The WiFi/BT/FM/GPS RF transceiver areas are 1.7/1.3/0.8/1.0mm^2, respectively. The measured WiFi 11g 54Mbps RX sensitivity is -78dBm and Pout is 20dBm with EVM of -28dB. The measured BT GMSK RX sensitivity is -94dBm and Pout is 10dBm. FM sensitivity is -110dBm and GPS cold/hot-start TTFF sensitivity is -148/-163dBm.

RMO2D-2 10:30
Novel Silicon-on-Insulator SP5T Switch-LNA Front-End IC Enabling Concurrent Dual-Band 256-QAM 802.11ac WLAN Radio Operations

Chun-Wen Paul Huang, Joe Soricelli, Lui Lam, Mark Doherty, Phil Antognetti, William Vaillancourt; Skyworks Solutions Inc., USA

Abstract: An innovative SOI SP5T switch-LNA integrated circuit is presented. The switch-LNA consists of a diplexer that provides out-of-band rejection and enables dual-band concurrent operation, a dual-band LNA with bypass attenuators, and three high linearity transmit paths. Tx paths feature 0.1 dB compression at > 33 dBm input power, with > 35 dB Tx to Rx isolation, and 0.8 and 1.2 dB insertion loss for low and high bands respectively. Receive paths feature 12 dB gain with 2.5–2.8 dB NF. Cascading the design with a dual-band WLAN PA, a complex dual-band front-end module can be easily constructed in a 3 × 4 mm package, which demonstrates transmit and receive LNA linearity with EVM < 2% at >16 dBm and > -5dBm output power respectively and compliant with the linearity requirements of the 802.11ac standard up to of 256-QAM 80 MHz operations.

RMO2D-3 10:50
A Digitally-Calibrated 20-Gb/s 60-GHz Direct-Conversion Transceiver in 65-nm CMOS

Seitaro Kawai, Ryo Minami, Yuki Tsukui, Yasuaki Takeuchi, Hiroki Asada, Ahmed Musa, Rui Murakami, Takahiro Sato, Qinghong Bu, Ning Li, Masaya Miyahara, Kenichi Okada, Akira Matsuzawa; Tokyo Institute of Technology, Japan

Abstract: This paper presents a digitally-calibrated 60-GHz direct-conversion transceiver. To improve the error vector magnitude (EVM) performance over the wide bandwidth, a digital calibration technique is applied. The 60-GHz transceiver implemented by 65nm CMOS achieves the maximum data rates of 20 Gb/s in 16QAM mode. The transmitter and receiver consume 351mW and 238mW from 1.2V supply, respectively. As a 60-GHz transceiver, the best Tx-to-Rx EVM performance of -26.2 dB is achieved for 16QAM 7Gb/s data rate.

RMO2D-4 11:10

A Low-Current Digitally Predistorted 3G-4G Transmitter in 40nm CMOS

Manel Collados[1], Hongli Zhang[2], Bernard Tenbroek[1], Hsiang-Hui Chang[3]; [1]MediaTek, UK, [2]MediaTek, Singapore, [3]MediaTek, Taiwan

Abstract: To create a wide-band transmit path with high current efficiency a single-balanced passive modulator is combined with a class-B single-ended resonant driver. The linearity of such configuration is limited by a strong 3rd harmonic response of the modulator combined with a strong third-order intermodulation in the driver. A novel digital pre-distortion approach is presented to enable good linearity under these highly non-linear conditions. Implemented in 40nm CMOS, the modulator and driver combined consume only 45mW to deliver a +3dBm Release 99 WCDMA signal with 1.1% EVM, -54dBc ACLR and -160dBc/Hz noise in the RX band. The ACLR remains below -50dBc over temperature, frequency and TX-power without adjustment of the predistortion coefficients. The transmitter delivers +0dBm 10MHz LTE with -51dBc ACLR.

RMO2D-5 11:30

A Passive Mixer-First Receiver Front-End without External Components for Mobile TV Applications

Inyoung Choi, Bumman Kim; POSTECH, Korea

Abstract: This paper describes a passive mixer-first receiver front-end (RFE) for mobile TV covering 100MHz to 800MHz without any external components. The proposed input matching technique with RC discharging circuit achieves a simple topology with a low noise. The out-of-band linearity is enhanced using the low pass filtering of sampling capacitor, delivering an outstanding out-of-band linearity. The out-of-band IIP3 and IIP2 are 7dBm and 36dBm, respectively at the maximum gain setting of 36dB. The third and fifth harmonic rejection ratios (HRR) are 49dB and 42dB, respectively. The power consumption is 23mW and the maximum NF is 3.6dB. The active area occupies 0.33mm^2 in 65nm CMOS technology.

Monday, 3 June 2013
13:30–15:10
Room 618-620
Session RMO3A: Advances in RF Data Converter Circuits
Chair: Eric Fogleman, MaxLinear
Co-Chair: Ed Balboni, Analog Devices Inc.

RMO3A-1 13:30
A 2-D GRO Vernier Time-to-Digital Converter with Large Input Range and Small Latency

Ping Lu[1], Pietro Andreani[1], Antonio Liscidini[2]; [1]Lund University, Sweden, [2]University of Toronto, Canada

Abstract: The proposed time-to-digital converter (TDC) arranges two Vernier gated-ring-oscillator (GRO) branches in a 2-dimension (2-D) fashion. All delay differences between X phases and Y phases can be used, rather than only the diagonal line. The large latency time inherited from Vernier structure is therefore dramatically reduced. The TDC is implemented in a 90nm CMOS process and consumes 1.8mA from 1.2V. The measured input range can safely cover a full period of a 50MHz sampling signal. With the same delay elements, the latency time is less than 1/6 of that needed in a standard Vernier TDC.

RMO3A-2 13:50
A 130nm CMOS Polar Quantizer for Cellular Applications

Peyman Nazari, Byung-Kwan Chun, Vipul Kumar, Eric Middleton, Zheng Wang, Payam Heydari; University of California at Irvine, USA

Abstract: A polar quantizer is presented for detection and quantization of modulated signals in cellular applications. It consists of amplitude and phase quantizers. A time-to-digital converter (TDC) is designed to measure and quantize the phase, while a typical ADC is used for amplitude quantization. Polar quantizer significantly reduces the sensitivity of the quantizer to amplitude resolution. The 10 bit polar quantizer fabricated in 130nm CMOS achieves 5.5dB of SQNR improvement compared to rectangular quantizer for signal bandwidths as high as 20MHz.

RMO3A-3 14:10
A 6GHz Input Bandwidth 2$V_{pp\text{-}diff}$ Input Range 6.4 GS/s Track-and-Hold Circuit in 0.25μm BiCMOS

Matthias Buck[1], Markus Grözing[1], Manfred Berroth[1], Michael Epp[2], Sébastien Chartier[2]; [1]Universität Stuttgart, Germany, [2]Cassidian, Germany

Abstract: A 0.25 μm SiGe-BiCMOS 6.4 GS/s track-and-hold circuit with an input bandwidth exceeding 6 GHz and up to 2 $V_{pp\text{-}diff}$ input voltage range applies a hold-mode muted preamplifier that reduces signal feedthrough and improves linearity. The track-and-hold circuit provides more than 59 dBc hold-mode SFDR3 for 1.0 to 6.0 GHz 1$V_{pp\text{-}diff}$ input signals at 6.4 GS/s, outperforming the best commercial THs operated at only 4 GS/s.

RMO3A-4 14:30

A 10-b, 300-MS/s Power DAC with 6-V_{pp} Differential Swing

Mohammad S. Mehrjoo, James F. Buckwalter; University of California at San Diego, USA

Abstract: A 10-bit digital-to-analog converter (DAC) is presented that delivers 6-V_{pp} into a 100-Ω differential load. The circuit is implemented in 45-nm CMOS SOI, which provides benefits for using a FET-stack current buffer. The measured DNL is better than 0.44 LSB. The DAC consumes 476 mW and achieves a peak SFDR of 54.4 dB and a minimum IM3 of -55.6 dBc. This DAC demonstrates the largest output swing and highest power efficiency for a high-resolution (>8b), high-speed (>100MS/s) DAC.

RMO3A-5 14:50

A 2×13-bit All-Digital I/Q RF-DAC in 65-nm CMOS

Morteza S. Alavi, George Voicu, Robert Bogdan Staszewski, Leo C.N. de Vreede, John R. Long; Technische Universiteit Delft, The Netherlands

Abstract: This paper presents a 2×13-bit I/Q RF-DAC-based all-digital modulator realized in 65 nm CMOS. The proposed quadrature up-converter uses a 25% duty-cycle clock to isolate the in-phase (I) and quadrature-phase (Q) modulating signals before combining. Using a 1.2 V supply and an on-chip power combiner, the modulator provides more than 21 dBm RF output power within a frequency range of 1.36 to 2.51 GHz. The peak RF output power, overall system and drain energy efficiencies of the modulator are 22.3 dBm, 31.5%, and 39.7%, respectively. Applying digital predistortion (DPD), 64 & 256 constellation points are measured with EVM better than -30 dB. The measured noise floor is below -160 dBc/Hz, with an IQ image rejection and LO leakage of -65 and -63 dBc, respectively. Its linearity has been evaluated with WCDMA modulation. Using DPD, the linearity improves by more than 15 dB.

Monday, 3 June 2013
13:30–15:10
Room 615-617
Session RMO3B: RF LNAs and RF Rectifiers
Chair: Frank Henkel, IMST GmbH
Co-Chair: Domine Leenaerts, NXP Semiconductors

RMO3B-1 13:30
Ultra-Low Voltage and Low Power UWB CMOS LNA Using Forward Body Biases

Chih-Shiang Chang, Jyh-Chyurn Guo; National Chiao Tung University, Taiwan

Abstract: An ultra-wideband (UWB) low noise amplifier (LNA) was designed and fabricated using 0.18μm 1.8V CMOS technology. The adoption of forward body biases (FBB) in a 3-stage distributed amplifier enables an aggressive scaling of the supply voltages and gate input voltage to 0.6V. The low voltage feature from FBB leads to more than 50% power consumption saving to 4.2mW. The measured power gain (S_{21}) is higher than 10dB in 3.1~8.1GHz and noise figure is 2.83~4.7 dB in the wideband of 2~10GHz. Superior linearity is achieved with IIP3 as high as 4.2dBm and 12.5dBm at 6.5GHz and 10GHz, respectively.

RMO3B-2 13:50
A DC-9.5GHz Noise-Canceling Distributed LNA in 65nm CMOS

Jianxun Zhu, Harish Krishnaswamy, Peter R. Kinget; Columbia University, USA

Abstract: A low noise amplifier is presented that uniquely achieves wide-band input matching and good low-frequency noise performance at the same time. Its topology is a hybrid of distributed amplifier and a common-source common-gate noise-canceling amplifier. The proof-of-principle prototype in 65nm CMOS operates from DC up to 9.5GHz with more than 12dB gain, achieves a minimum noise figure of 2.8dB, P_{1dB} of -7dBm, IIP_3 of +4dBm, consumes 18mW from a 1.4V power supply and occupies a total active area of 0.4mm^2.

RMO3B-3 14:10
A Highly Linear Low-Noise Amplifier Using a Wideband Linearization Technique with Tunable Multiple Gated Transistors

Jaeyoung Lee[1], Jeiyoung Lee[2], Bonkee Kim[3], Bo-Eun Kim[4], Cam Nguyen[1]; [1]Texas A&M University, USA, [2]Samsung, Korea, [3]HiDeep Inc., Korea, [4]RAONTECH Inc., Korea

Abstract: A wideband linearization technique using tunable multiple gated transistors (MGTRs) is proposed. Extra tunable input capacitors and the modified derivative superposition (DS) method are also adopted to increase the amplifier's linearity at RF. A low-noise amplifier (LNA) employing the proposed linearization technique has been developed with 0.18-μm CMOS process for various mobile TV standards in UHF band (470–862 MHz). The LNA achieves 19-dBm IIP_3, 16.5-dB gain, and 1.33-dB NF with 10.8-mW power consumption. Over the desired UHF band, the LNA increases the average IIP_3 obtained with off-state auxiliary transistor by 11.7 dBm.

RMO3B-4 14:30

A Highly Selective LNTA Capable of Large-Signal Handling for RF Receiver Front-Ends

M. Mehrpoo, Robert Bogdan Staszewski; Technische Universiteit Delft, The Netherlands

Abstract: To achieve ultimately flexible multi-core radio operation, wide-band receiver RF front-ends must be robust against interference well in excess of the requirements usually specified by a radio standard. In this paper, a highly selective, very linear low-noise transconductance amplifier (LNTA) capable of large-signal handling for current-mode receiver (RX) front-ends is proposed and implemented in 65-nm CMOS. It is shown that by combining on-chip high-Q bandpass filters with a push/pull class-AB common-gate stage, a measured 1-dB desensitization point (B_{1dB}) and large-signal IIP3 of +8 dBm and +20 dBm, respectively, can be achieved. In addition, by applying a noise cancellation technique, via an auxiliary push/pull class-AB common-source stage, the proposed LNTA measures a moderate NF of 5.9 dB, which is a very competitive number for such high value of B_{1dB}. The circuit consumes 7.5 mA at 1.5 V.

RMO3B-5 14:50

A 62GHz Inductor-Peaked Rectifier with 7% Efficiency

Hao Gao, Marion K. Matters-Kammerer, Dusan Milosevic, Arthur van Roermund, Peter Baltus; Technische Universiteit Eindhoven, The Netherlands

Abstract: This paper presents the first 62 GHz fully on-chip RF-DC rectifier in 65nm CMOS technology. The rectifier is the bottleneck in realizing on-chip wireless power receivers. In this paper, efficiency problems of the mm-wave rectifier are discussed and the inductor-peaked rectifier structure is proposed and realized. By using an inductor-peaked diode connected transistor, self-threshold voltage modulation, and an output filter, the measured rectifier reaches 7% efficiency with 1 mA current load. Compared to previous state-of-art 45 GHz rectifier with 1.2% efficiency [1], our solution achieves a higher efficiency at a higher frequency, providing a better solution for mm-wave wireless power receivers.

Monday, 3 June 2013
13:30–15:10
Room 611-612
Session RMO3C: Wideband VCO Circuits and Architectures
Chair: Jane Gu, University of California at Davis
Co-Chair: Fred Lee, Fairchild Semiconductor

RMO3C-1 13:30
A 5.12–12.95GHz Triple-Resonance Low Phase Noise CMOS VCO for Software-Defined Radio Applications

M. Moslehi Bajestan, K. Entesari; Texas A&M University, USA

Abstract: This paper presents a wide-tuning range Voltage-Controlled Oscillator (VCO) for software-defined radio (SDR) applications using a resonator with three potential oscillation modes. The implemented prototype in 0.18μm CMOS technology achieves a continuous tuning range of 86.7% from 5.12GHz to 12.95GHz while drawing 5 to 10mA current from 1-V supply. The measured phase noise at 1MHz offset from carrier frequencies of 5.9, 9.12 and 12.25GHz is -122.9, -117.1 and -110.5dBc/Hz, respectively. The VCO occupies a chip area of 0.33mm^2.

RMO3C-2 13:50
A -189dBc/Hz FOM$_T$ Wide Tuning Range Ka-Band VCO Using Tunable Negative Capacitance and Inductance Redistribution

Qiyang Wu[1], Salma Elabd[1], Tony K. Quach[2], Aji Mattamana[2], Steve R. Dooley[2], Jamin McCue[1], Pompei L. Orlando[2], Gregory L. Creech[1], Waleed Khalil[1]; [1]Ohio State University, USA, [2]AFRL, USA

Abstract: An ultra wideband LC voltage-controlled oscillator (LC-VCO) operating in the Ka-band with equally spaced sub-band coarse tuning characteristics is proposed and characterized. A tunable negative capacitance (TNC) circuit technique is used to cancel the fixed capacitance in the LC-tank to extend the tuning range (TR). A digitally-switched varactor coarse tuning structure with an inductance redistribution technique is utilized to reduce VCO gain (K_V) and retain uniform spacing between tuning curves. The proposed VCO structure and a baseline VCO are fabricated in a 130 nm CMOS process. Compared to the reference VCO, the proposed VCO achieves a 34% increase in TR with maximum K_V of 450 MHz/V. The measured worst-case phase noise is -100.1 dBc/Hz at 1 MHz offset across the TR from 30.5 GHz to 39.6 GHz. The power dissipation of the VCO core is 11 mW from a 1.2 V supply. The TNC-based VCO achieves a FOM$_T$ of -189 dBc/Hz, which is the highest reported at the Ka-band.

RMO3C-3 14:10
A Dual-Band LO Generation System Using a 40GHz VCO with a Phase Noise of -106.8dBc/Hz at 1-MHz

Ying Chen, Yu Pei, Domine M.W. Leenaerts; NXP Semiconductors, The Netherlands

Abstract: This paper demonstrates a dual-band LO generation system using a low phase noise single-band 40GHz VCO as the signal source. The LO generation system has two outputs: single-band LO1 at 20GHz and dual-band LO2 switchable between 10GHz and 15GHz. Implemented in 0.25-μm

SiGe:C BiCMOS, the VCO achieves a phase noise of -106.8dBc/Hz at 1-MHz offset from 40GHz with a frequency tuning range of 9.7%.

RMO3C-4 14:30

A 120GHz Quadrature Frequency Generator with 16.2GHz Tuning Range in 45nm CMOS

Wouter Volkaerts, Michiel Steyaert, Patrick Reynaert; Katholieke Universiteit Leuven, Belgium

Abstract: This paper presents a new architecture for a 120GHz quadrature frequency generator with large tuning range and immunity against PA-VCO coupling. Combining the output signals of two independent oscillators, the pulling effect is removed and the oscillator can be integrated with a PA and an antenna on the same chip. This architecture also makes quadrature generation with large tuning range feasible at 120GHz. The chip is fabricated in a 45nm CMOS technology and shows a tuning range of 16.2GHz (13.5%), a phase noise of -112dBc/Hz @ 10MHz offset and a phase error of 5°.

Monday, 3 June 2013
15:40–17:20
Room 618-620
Session RMO4A: Baseband Circuits and Modulators/Demodulators
Chair: Madhukar Reddy, MaxLinear
Co-Chair: Ayman Fayed, Iowa State University

RMO4A-1 15:40
An FM Demodulator Operating Across 2–10GHz IF

Akshay Visweswaran, John R. Long, Luca Galatro, Marco Spirito, Robert Bogdan Staszewski;
Technische Universiteit Delft, The Netherlands

Abstract: An FM demodulator operating across 8GHz IF bandwidth for application in low-power, wideband heterodyne receivers is presented. A 4-stage ring oscillator is frequency modulated by a wideband input. Locking to $1/4^{th}$ the input frequency, it divides the FM deviation by four, thereby reducing the energy required for wideband demodulation to 0.75nJ/bit. Autocorrelation of the quadrature-phased outputs using a new low-power folded CMOS mixer is capable of detecting FM up to 400Mb/s over 2–10GHz IF. The inductorless 65nm CMOS prototype circuit occupies $0.17mm^2$ and dissipates 3mW from 1.2V.

RMO4A-2 16:00
A 3.4mW 65nm CMOS 5^{th} Order Programmable Active-RC Channel Select Filter for LTE Receivers

Mohammed Abdulaziz, Anders Nejdel, Markus Törmänen, Henrik Sjöland; Lund University, Sweden

Abstract: In this work a low power 5^{th} order Chebyshev active-RC low pass filter that meets Rel-8 LTE receiver requirements has been designed with programmable bandwidth and overshoot. Designed for a homodyne LTE receiver, filter bandwidths from 700kHz to 10MHz are supported. The bandwidth of the operational amplifiers is improved using a novel phase enhancement technique. The filter was implemented in 65nm CMOS technology with a core area of $0.29mm^2$. Its total current consumption is 2.83mA from a 1.2V supply. The measured input referred noise is $39nV/\sqrt{Hz}$, the in-band IIP3 is 21.5dBm, at the band-edge the IIP3 is 20.7dBm, the out-of-band IIP3 is 20.6dBm, and the compression point is 0dBm.

RMO4A-3 16:20
A Low-Q Resonant Tank Phase Modulator for Outphasing Transmitters

Gilad Yahalom, Joel L. Dawson; MIT, USA

Abstract: A new design concept is proposed for a phase modulator for outphasing transmitter architectures, utilizing the phase shifting capabilities of a resonant tank and the ability to separately control the circuit properties via its components. A prototype in 65-nm CMOS achieves 12 bits of resolution, with a fast settling time of less than five carrier cycles to within 1°. The circuit is also tested as a stand-alone transmitter showing an EVM of less than 5% for 8-PSK modulation at maximum data rate, meeting the FCC requirements for operation at the medical implant communication services (MICS) band.

RMO4A-4 16:40

A Linear-in-dB Analog Baseband Circuit for Low Power 60GHz Receiver in Standard 65nm CMOS

Yanjie Wang[1], Chris Hull[1], Glenn Murata[1], Shmuel Ravid[2]; [1]Intel Corporation, USA, [2]Intel Corporation, Israel

Abstract: This paper presents an analog baseband (ABB) circuit for low power 60 GHz wireless receiver in standard 65 nm CMOS. The proposed analog baseband system combines variable gain amplifiers (VGA) with a 3rd-order type II Chebyshev filter and provides linear steps as well as filter tuning range to achieve sufficient out-of-band rejection. The ABB demonstrates 2 dB gain step tuning range from 3–31 dB, 3-dB bandwidth of 980 MHz, OP1dB of 0dBm, and noise figure of 6 dB to 21 dB. The ABB consumes 48 mW at max gain setting and 32 mW at minimum gain setting from a 1.1 V supply. The entire ABB occupies an area of 1.1 mm^2 with active area of 0.2 mm^2.

Monday, 3 June 2013
15:40–17:20
Room 611-612
Session RMO4C: Reactively-Coupled Oscillators
Chair: Waleed Khalil, Ohio State University
Co-Chair: Reynold Kagiwada, Northrop Grumman

RMO4C-1 15:40
A 100GHz Active-Varactor VCO and a Bi-Directionally Injection-Locked Loop in 65nm CMOS

Shinwon Kang, Ali M. Niknejad; University of California at Berkeley, USA

Abstract: A 100GHz fundamental active-varactor VCO and a bi-directionally injection-locked loop are demonstrated in 65nm CMOS. Without using a conventional passive varactor, the proposed VCO achieves a tuning range of 5.2% at 100GHz and a phase noise of -112.1dBc/Hz at 10MHz offset. By utilizing the proposed transmission-line-based capacitive coupling, four oscillators are injection-locked properly and the loop creates eight phases of the carrier and 6dB(=10log4) of phase noise improvement, realizing a measured phase noise is -118.8dBc/Hz at 10MHz offset.

RMO4C-2 16:00
A Multichannel, Multicore mm-Wave Clustered VCO with Phase Noise, Tuning Range, and Lifetime Reliability Enhancements

Farid Shirinfar[1], Med Nariman[2], Tirdad Sowlati[2], Maryam Rofougaran[2], Reza Rofougaran[2], Sudhakar Pamarti[1]; [1]University of California at Los Angeles, USA, [2]Broadcom, USA

Abstract: Clustering and multi-core transformer coupling techniques are presented to improve phase noise, tuning range, and reliability of a mm-wave VCO. A proof-of-concept design targeting the WiGig protocol is shown. Each cluster of VCOs covers one channel resulting in better phase noise performance. Multicores of VCOs with uncorrelated noise are combined using transformers to further enhance phase noise and combat the voltage swing reliability issues. Furthermore, due to realization of multiple inductive elements in parallel instead of one small inductor, this approach bypasses Q-degradation of small inductors (<50pH). The VCO achieves a phase noise of -101.8dBc/Hz at 1MHz offset with over 12.6% tuning range (50.7GHz to 57.5GHz) and an FOM of -183dB/Hz.

RMO4C-3 16:20
A 105GHz VCO with 9.5% Tuning Range and 2.8mW Peak Output Power Using Coupled Colpitts Oscillators in 65nm Bulk CMOS

Muhammad Adnan, Ehsan Afshari; Cornell University, USA

Abstract: In this work, a loop of unidirectionally coupled oscillators to demonstrate high tuning range and output power is proposed. To achieve large tuning range, two different tuning mechanisms are simultaneously exploited. First each core oscillator is tuned using a variable capacitor. Next, by controlling the phase/delay between the coupled oscillators, the entire loop dynamics and hence its frequency is tuned. In this paper, we analyze a loop of "n" coupled oscillators using Adler's equation and derive the expression for the maximum tuning range. The proposed system is designed and

implemented using four coupled Colpitts VCOs in a 65nm bulk CMOS process. The VCO achieves continuous tuning range of 9.5% at the center frequency of 105GHz with the peak output power of 2.8mW. The circuit consumes 54mW from a 1.2V supply. To the best of our knowledge, this VCO has the highest output power and tuning range among all the CMOS oscillators at or above 100GHz.

RMO4C-4 16:40

Dual-Core High-Swing Class-C Oscillator with Ultra-Low Phase Noise

Massoud Tohidian, Seyed Amir Reza Ahmadi Mehr, Robert Bogdan Staszewski; Technische Universiteit Delft, The Netherlands

Abstract: We propose an ultra-low phase noise oscillator topology that works on the premise that coupling a second identical oscillator core would reduce the overall phase noise by 3 dB. For each core, a high-swing class-C oscillator is used to achieve the lowest phase noise. The realized oscillator is tunable from 4.07–4.91 GHz, drawing 39–59 mA from a 2.15 V power supply. The measured phase noise is -146.7 dBc/Hz and -163.1 dBc/Hz at 3 MHz and 20 MHz offset, respectively, from 4.07 GHz carrier. This is the lowest ever reported phase noise in bulk CMOS IC. This phase noise meets GSM900 normal basestation receiver and mobile station transmitter standards, which have the toughest phase noise requirements in cellular communications.

Monday, 3 June 2013
15:40–17:20
Room 613-614
Session RMO4D: High-Speed Data Transceiver Circuits
Chair: Steven Turner, BAE Systems
Co-Chair: Ramesh Harjani, University of Minnesota

RMO4D-1 15:40
A 42 to 47-GHz, 8-bit I/Q Digital-to-RF Converter with 21-dBm P_{sat} and 16% PAE in 45-nm SOI CMOS

Amir Agah[1], Wei Wang[1], Peter M. Asbeck[1], Lawrence Larson[2], James F. Buckwalter[1]; [1]University of California at San Diego, USA, [2]Brown University, USA

Abstract: A novel stacked FET digital-to-RF converter is implemented in 45-nm SOI CMOS, which shares DC current through an I/Q digital-to-analog converter (DAC), I/Q mixer, and stacked-FET PA to provide high output power. The proposed architecture transmits at 1.25 Gbps for QPSK at 45GHz. This transmitter exhibits a 21.3-dBm saturated output power, while achieving a peak PAE of 16%. The circuit occupies 0.3mm^2 including pads, while the PAE and P_{sat} remains above 13% and 18 dBm from 42 to 47 GHz.

RMO4D-2 16:00
A 32-Gbps 4×4 Passive Cross-Point Switch in 45-nm SOI CMOS

Donghyup Shin, Gabriel M. Rebeiz; University of California at San Diego, USA

Abstract: This paper presents a passive 4×4 cross-point switch in 45-nm SOI CMOS technology for LVDS systems with near-zero power consumption. The CMOS switch dimensions and layout structures are optimized using full-wave electromagnetic simulations for the highest 3-dB bandwidth in order to maximize the data-rate for digital signal transmission. Also, a novel series switch is used between the cells to enhance the bandwidth. The 4×4 switch matrix results in a measured 3-dB bandwidth of ~ 20–25 GHz (depending on the path) and an isolation > 40 dB at 26.5 GHz. The group delay variation is < ±5 psec, and results in very low jitter as seen from eye measurements (< 1.3 psec). Good eye-openings are obtained at 26 Gbps and up to 31.5 Gbps. The design is readily scalable to an 8×8 cross-point switch matrix.

RMO4D-3 16:20
A 20Gb/s 136fJ/b 12.5Gb/s/μm On-Chip Link in 28nm CMOS

Meisam Honarvar Nazari, Azita Emami-Neyestanak; Caltech, USA

Abstract: A high data rate, low power on-chip link in 28nm CMOS is presented. It features a double-sampling receiver with dynamic offset modulation and a capacitively-driven transmitter. The functionality of the link was validated using 4–7mm minimum-pitch on-chip wires. It achieves up to 20Gb/s of data rate (13.9Gb/s/μm) with BER< 10^{-12}. It has better than 136fJ/b of power efficiency at 10Gb/s. The total area of the transmitter and receiver is 1110μm^2.

RMO4D-4 16:40

A Wideband Injection Locking Scheme and Quadrature Phase Generation in 65nm CMOS

Mayank Raj, Azita Emami-Neyestanak; Caltech, USA

Abstract: A novel technique for wideband injection locking in an LC oscillator is proposed. PLL and injection locking elements are combined symbiotically to achieve wide locking range while retaining the simplicity of the latter. This method doesn't require a phase frequency detector or a loop filter to achieve phase lock. 13.4GHz–17.2GHz locking range and an average jitter tracking bandwidth of up to 400 MHz was measured in a high-Q LC oscillator. This architecture is used to generate quadrature phases form a single clock without any frequency division, and to provide high frequency jitter filtering while retaining the low frequency correlated jitter essential for clock forwarded receivers.

RMO4D-5 17:00

Electronic Laser Phase Noise Reduction

Firooz Aflatouni[1], Behrooz Abiri[1], Angad Rekhi[1], Hooman Abediasl[2], Hossein Hashemi[2], Ali Hajimiri[1]; [1]Caltech, USA, [2]University of Southern California, USA

Abstract: The first integrated wideband laser phase noise reduction scheme is presented where the laser phase noise is first detected using a photonic chip, processed using an electronic chip, and subtracted from the laser phase in a feed-forward manner. The proof-of-concept experiments on a commercially available 1553nm distributed feedback laser show linewidth reduction from 6MHz to 250kHz equivalent to 14dB phase noise improvement. The hybrid integration of the photonic and electronic chips enables dramatic power consumption and area reduction compared to bench-top designs. This feed-forward scheme performs wideband phase noise reduction independent of the light source and, as such, it is compatible with several types of lasers.

Tuesday, 4 June 2013
08:00–09:40
Room 615-617
Session RTU1B: mm-Wave Power Amplifiers
Chair: Jyoti Mondal, Northrop Grumman
Co-Chair: Gary Zhang, Guangdong University of Technology

RTU1B-1 08:00
A 53-to-73GHz Power Amplifier with 74.5mW/μm² Output Power Density by 2D Differential Power Combining in 65nm CMOS

Wei Fei[1], Hao Yu[1], Wei Meng Lim[1], Junyan Ren[2]; [1]Nanyang Technological University, Singapore, [2]Fudan University, China

Abstract: Towards wide bandwidth and high output power density for 60GHz PA design in 65nm CMOS, this paper introduces a 2D differential power combining network by metamaterial-based zero-phase-shifter. Simultaneous distributed amplification and power combining can be achieved with improved performances in both power density and bandwidth. The PA measurement results show 13.2 dB gain, 8.7% PAE, 13dBm P1dB, and 20GHz bandwidth (53 to 73GHz) within an area of 0.268mm².

RTU1B-2 08:20
Analysis, Design and Implementation of mm-Wave SiGe Stacked Class-E Power Amplifiers

Kunal Datta, Jonathan Roderick, Hossein Hashemi; University of Southern California, USA

Abstract: Design equations and performance limits of stacked Class-E power amplifiers at mm-waves, including the limitations imposed by device parasitics, are presented in this paper. As a proof of concept of this parasitic aware mm-wave Class-E design methodology and to demonstrate the beyond BVCEO Class-E operation in a stacked architecture at mm-wave frequencies, a Q-band, single ended, two-stage, double-stacked, Class-E power amplifier is designed in a 0.13 μm SiGe HBT BiCMOS process. The measured performance of the fabricated chip show 23.4 dBm maximum output power at 34.9% peak power added efficiency (PAE), and 14.6 dB of power gain across 5 GHz centered around 41 GHz for a supply voltage of 4 V. The total chip area including the pads is 0.8 mm × 1.28 mm.

RTU1B-3 08:40
A Fully Integrated 22.6dBm mm-Wave PA in 40nm CMOS

Farid Shirinfar[1], Med Nariman[2], Tirdad Sowlati[2], Maryam Rofougaran[2], Reza Rofougaran[2], Sudhakar Pamarti[1]; [1]University of California at Los Angeles, USA, [2]Broadcom, USA

Abstract: A fully integrated 60GHz CMOS PA with a P_{SAT} of 22.6dBm is presented. To our knowledge, this is the highest reported P_{SAT} at mm-waves in standard CMOS. To achieve a high power level, 32 differential PAs are combined through a network of transmission lines, Wilkinson combiners, and a multi-port argyle transformer. This method of combining minimizes loss while implementing a low impedance load (~12Ω) at the drains of each of the last stage PAs. Electromigration and other reliability issues are discussed.

RTU1B-4 09:00

Large-Scale Power-Combining and Linearization in Watt-Class mmWave CMOS Power Amplifiers

Ritesh Bhat, Anandaroop Chakrabarti, Harish Krishnaswamy; Columbia University, USA

Abstract: Switching-class PAs employing device-stacking have been recently explored to meet the challenge of efficient power amplification at mmWave frequencies at moderate power levels of around 20dBm. In this paper, we propose the use of a single-step, large-scale (8-way), 75%-efficient lumped quarter-wave power combiner that is co-designed with stacked Class-E-like PA unit cells to enable a Q-band 45nm SOI CMOS PA with a peak P_{sat} of 27.2dBm (>0.5W), peak PAE of 10.7% and 1dB flatness in P_{sat} over nearly the entire Q-band (33–46GHz). This measured output power level is approximately 5× higher than prior reported mmWave silicon PAs. In order to support complex modulations with high average-efficiency, we also propose a novel linearizing architecture that combines large-scale power combining, supply-switching for efficiency under backoff and dynamic load modulation for linearization. A second fully-integrated 42.5GHz 45nm SOI CMOS PA is implemented based on this architecture and achieves 60% of the peak efficiency at 6dB back-off.

RTU1B-5 09:20

A 135–170GHz Power Amplifier in an Advanced SiGe HBT Technology

Neelanjan Sarmah[1], Bernd Heinemann[2], Ullrich R. Pfeiffer[1]; [1]Bergische Universität Wuppertal, Germany, [2]IHP, Germany

Abstract: High-power, broadband power amplifiers (PA) operating in the D-band (110–170 GHz) are essential towards implementation of broadband frequency multiplier chains at sub-mmWave frequencies. In this paper we present the design of a 3-stage power amplifier (PA) with 3-dB bandwidth of 35 GHz (135–170 GHz) and implemented in 130 nm SiGe BiCMOS technology. A staggered tuning approach where the peak gain of the individual or group of individual stages are tuned at offset frequencies is used for broadband operation. In the 135–170 GHz, the small signal gain for the PA is 14–17 dB and the saturated output power (P_{sat}) varies from 5–8 dBm and the output referred 1 dB compression point (P_{1dB}) varies from 1–6 dBm over this frequency range. The nominal dc power consumption of this PA is 320 mW with peak PAE of 1.6%. To our best knowledge, this is the highest bandwidth reported for silicon PAs in the D band.

Tuesday, 4 June 2013
08:00–09:40
Room 611-612
Session RTU1C: Millimeter and Sub-Millimeter Wave Transceivers
Chair: Jeyanandh Paramesh, Carnegie Mellon University
Co-Chair: Hua Wang, Georgia Institute of Technology

RTU1C-1 08:00
24GHz CMOS Transceiver with Novel T/R Switching Concept for Indoor Localization

Amin Hamidian[1], Randolf Ebelt[2], Denys Shmakov[2], Martin Vossiek[2], Tao Zhang[1], Viswanathan Subramanian[1], Georg Boeck[1]; [1]Technische Universität Berlin, Germany, [2]Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany

Abstract: This paper presents a 130 nm CMOS transceiver for 24 GHz wireless indoor localization. Due to a novel Rx/Tx switching concept RF-losses between receiver/transmitter and antenna could be reduced and the T/R isolation was drastically improved. The measured transceiver chip achieves an output power and noise figure of >5 dBm and <6 dB, respectively with 2 mm^2 total chip size. The complete transceiver consumes 16 mW in the Rx- and 26 mW in the Tx-mode. The RF-transceiver-chip was integrated with a DSP-unit and mounted on a PCB for wireless indoor localization demonstration. The measured results show a distance measurement precision in the cm-range.

RTU1C-2 08:20
A Low Power 60-GHz 2.2-Gbps UWB Transceiver with Integrated Antennas for Short Range Communications

Alexandre Siligaris, Fabrice Chaix, Michaël Pelissier, Vincent Puyal, José Zevallos, Laurent Dussopt, Pierre Vincent; CEA-LETI, France

Abstract: A 60-GHz low power fully integrated transceiver including antennas, fabricated in CMOS 65nm SOI and packaged in low cost QFN is described. The circuit achieves 2 Gbps and 500 Mbps rates at 7.5 cm and 22.5 cm transmission ranges respectively. The transceiver energy efficiency is lower than 50 pJ/bit thanks to scalable power consumption using pulse generator and Super Regenerator Oscillator architecture.

RTU1C-3 08:40
A 283GHz Low Power Heterodyne Receiver with On-Chip Local Oscillator in 65nm CMOS Process

José Moron Guerra[1], Alexandre Siligaris[1], Jean-François Lampin[2], François Danneville[2], Pierre Vincent[1]; [1]CEA-LETI, France, [2]IEMN, France

Abstract: A Fully integrated 283 GHz heterodyne receiver in 65 nm CMOS process is presented in this paper. The circuit includes a resistive differential mixer, an intermediate frequency amplifier and a 282 GHz sub-harmonic injection locked oscillator. The on-chip oscillator generates a 94 GHz fundamental tone but exploits a 282 GHz third harmonic. An injection signal of 47 GHz (one sixth of the RF frequency) is used to lock the oscillator on a reference. The receiver measured conversion

gain is -6 dB for a DC power consumption of 97.6 mW. Simulated noise figure is 38 dB. The chip size is 820 μm × 780 μm including matching networks and DC/RF pads.

RTU1C-4 09:00

A 240GHz Direct Conversion IQ Receiver in 0.13μm SiGe BiCMOS Technology

Mohamed Elkhouly[1], Yanfei Mao[1], Srdjan Glisic[1], Chafik Meliani[1], Frank Ellinger[2], J. Christoph Scheytt[3]; [1]IHP, Germany, [2]Technische Universität Dresden, Germany, [3]Universität Paderborn, Germany

Abstract: A 240 GHz direct conversion IQ receiver manufactured in 0.13μm SiGe BiCMOS technology with f_T/f_{max} of 300/500 GHz is presented. The receiver consists of a four stage LNA, an active power divider, an LO IQ generation network, and direct down-conversion fundamental mixers. The integrated IQ receiver yields a conversion gain of 18 dB, an 18 dB simulated DSB NF, and a 3 dB bandwidth of 25 GHz. The required 245 GHz LO power is in the order of - 10 dBm. The receiver exhibits an IQ amplitude and phase imbalance of 1 dB and 3° respectively. It draws 135 mA from the 3.5 V supply and 20 mA from 2 V.

RTU1C-5 09:20

A 240GHz Single-Chip Radar Transceiver in a SiGe Bipolar Technology with On-Chip Antennas and Ultra-Wide Tuning Range

Christian Bredendiek[1], Nils Pohl[2], Timo Jaeschke[1], Klaus Aufinger[3], Attila Bilgic[4]; [1]Ruhr-Universität Bochum, Germany, [2]Fraunhofer FHR, Germany, [3]Infineon Technologies, Germany, [4]KROHNE Messtechnik, Germany

Abstract: This paper presents an ultra-wideband single-chip radar transceiver MMIC around 240 GHz in a SiGe:C bipolar laboratory technology with an f_T of 240 GHz and f_{max} of 380 GHz. The presented transceiver architecture consists of a fundamental 120 GHz VCO, two 240 GHz frequency doublers, a fundamental 240 GHz down-conversion mixer, a divide-by-four stage, a PLL-mixer and two on-chip patch antennas. The complete transceiver architecture is fully differential. The chip facilitates a -1 dBm peak output power (EIRP) at the transmit patch antenna and a tuning range of 61 GHz. The phase noise at 1 MHz offset is -84 dBc/Hz at 240 GHz (and better than -76 dBc/Hz over the full tuning range). The 240 GHz mixer offers a simulated noise figure below 17 dB, a simulated conversion gain of better than 5 dB, and an input referred compression point of -1.3 dBm. The results are achieved with a power consumption of 750 mW from a single 5 V supply.

Tuesday, 4 June 2013
10:10–11:50
Room 618-620
Session RTU2A: Reconfigurable and Software-Defined Radio Front-End Techniques

Chair: Oren Eliezer, Xtendwave

Co-Chair: Eric Klumperink, University of Twente

RTU2A-1 10:10
A 0.5-to-3GHz Software-Defined Radio Receiver Using Sample Domain Signal Processing

Run Chen, Hossein Hashemi; University of Southern California, USA

Abstract: A 0.5-to-3 GHz software-defined radio receiver leveraging Sampled Domain Signal Processing (SPSD) is demonstrated in a 65nm LP CMOS technology. The SDSP approach achieves band-pass filtering, harmonic rejection, and frequency translation simultaneously. Input impedance matching is achieved in an active translational loop that tracks the desired RF frequency. The chip includes a wideband frequency synthesizer, multi-phase non-overlapping clock generation circuitry, bandgap and power supply regulators. It achieves out-of-band IIP3 > 11.7 dBm, IIP2 > 58 dBm, NF = 5.5~8.8 dB, and uncalibrated 3rd and 5th order harmonic rejections exceeding 47 dB and 52 dB, respectively.

RTU2A-2 10:30
A 5–9-mW, 0.2–2.5-GHz CMOS Low-IF Receiver for Spectrum-Sensing Cognitive Radio Sensor Networks

Masaki Kitsunezuka, Kazuaki Kunihiro; NEC Corporation, Japan

Abstract: A low-power, wideband CMOS receiver for spectrum-sensing cognitive radio sensor networks is presented. The low-IF receiver equipped with an inverter-based LNA-balun and I/Q sub-threshold rectifier enables low-power and high-speed spectrum sensing. For further extension to support higher data-rate radio systems, our local oscillator provides a frequency-dividing function when a low-phase-noise signal source is optionally used. A prototype chip fabricated in a 65-nm CMOS process can support a wide frequency range of 0.2–2.5 GHz with 43-dB maximum gain, 6-dB NF, and -9-dBm IIP3 and only occupies 0.6 mm^2 while consuming as low as 5–9 mW at a 0.6-V supply.

RTU2A-3 10:50
A 65nm CMOS High-IF Superheterodyne Receiver with a High-Q Complex BPF

Iman Madadi, Massoud Tohidian, Robert Bogdan Staszewski; Technische Universiteit Delft, The Netherlands

Abstract: We propose a highly reconfigurable superheterodyne receiver that employs a 3rd-order complex IQ charge-sharing band-pass filter (BPF) for image rejection and 1st-order feedback based RF-BPF for channel selection filtering. The operating RF input frequency of the receiver is 500 MHz–

1.2GHz with varying high-IF range of 33–80 MHz. All the gain stages are merely inverter-based g_m stages. The total gain of the receiver is 35 dB and in-band IIP3 at mid-gain is +10 dBm. The NF of the receiver is 6.7 dB, which is acceptable for the receiver without an LNA. The architecture is highly reconfigurable and follows the technology scaling. The RX occupies 0.47mm^2 of active area and consumes 24.5mA at 1.2V power supply.

RTU2A-4 11:10

A Multi-Path Multi-Rate CMOS Polar DPA for Wideband Multi-Standard RF Transmitters

Arnaud Werquin, Antoine Frappé, Andreas Kaiser; IEMN, France

Abstract: A two-path digital power amplifier (DPA) in 1.2V 65nm CMOS is presented. This highly reconfigurable and frequency agile block is designed to be used as an envelope modulator in a wideband multi-standard polar transmitter. Each path is composed of a 12-bit DPA ensuring the modulation of the envelope of the RF signal. The DPAs are controlled by envelope code words (ECW) at different sample rates. This diversity strongly attenuates the images produced by the direct digital to RF conversion, avoiding passive filtering. The baseband sample rate conversion can easily be reconfigured. The proposed front-end can manage spurious emissions depending on the standard, the carrier frequency and the required power. The DPAs also integrate active input impedance compensation cells in order to limit the input impedance modulation when switching the DPA cells. The two-path DPA covers a 0.9–1.9 GHz bandwidth with 16.7dBm output 1dB compression point and 12.4% PAE. 64-QAM presents -28dB EVM while active area occupies 1×0.25mm^2.

RTU2A-5 11:30

A Frequency-Agile RF Frontend for Multi-Band TDD Radios in 45nm SOI CMOS

Sushmit Goswami[1], Helen Kim[2], Joel L. Dawson[1]; [1]MIT, USA, [2]MIT Lincoln Laboratory, USA

Abstract: A tunable and highly digital RF frontend for multi-band TDD radios is integrated in 45nm SOI CMOS. The PA absorbs the TX branch of the TX/RX switch with no added loss. Peak PA output power is 27.5±0.5dBm from 1.6 to 3.4GHz, with up to 30% total efficiency at 2V. For TDD LTE applications, better than -30dBc ACLR and -25dB EVM is measured with 16-QAM, 20MHz signals from 1.65 to 3.5GHz, with up to 16.5% average efficiency and 22.9dBm average power. The broadband LNA achieves A_v > 14dB, NF=4.3 ± 1.6dB and IIP3 > -7dBm from 1.6 to 3.4GHz while drawing just 6mA from 1V.

Tuesday, 4 June 2013
10:10–11:50
Room 615-617
Session RTU2B: Efficiency and Linearity Enhancement for RF/MW Power Amplifiers

Chair: Jeffrey Walling, University of Utah
Co-Chair: Eddie Spears, RFMD

RTU2B-1 10:10
A Single Chip HBT Power Amplifier with Integrated Power Control

David S. Ripley; Skyworks Solutions Inc., USA

Abstract: The GSM power amplifier market continues to drive towards low cost and small size, but remains reluctant to compromise on performance. Current generation PA products utilize InGaP HBT to deliver RF performance and integrate bias and control on a supporting silicon die. This approach is common amongst many PA manufacturers with the exception of CMOS PA [1] solutions. This paper describes a solution using an HBT BiFET [2] technology to integrate both the precision control function and power amplifier onto a common die. The resulting solution opens opportunity for industry leading size and performance at no additional cost or RF performance penalty.

RTU2B-2 10:30
A Novel Load Insensitive RF Power Amplifier Using a Load Mismatch Detection and Curing Technique

Donghyeon Ji[1], Jooyoung Jeon[2], Junghyun Kim[1]; [1]Hanyang University, Korea, [2]Avago Technologies, Korea

Abstract: This paper proposes a new load insensitive RF power amplifier (PA) for mobile handsets using a load mismatch detection and curing technique. The PA controls a tunable output matching network (TOMN) adaptively based on the information of a mismatched load, thereby enhancing PA performances dramatically at a mismatched load without substantial performance degradation at a matched load. A load mismatch detector and TOMN can simply be implemented by using 0.18-μm silicon on insulator (SOI) FET that are integrated with 2-μm InGaP/GaAs HBT PA MMIC into a single module. To verify the idea, the PA module has been designed and implemented especially for a linearity enhancement under load mismatch condition. With WCDMA R'99 signal at 1.95 GHz, the measured results showed that ACLR at output power of 28.25 dBm was improved by as much as 13.7 dB on the worst ACLR-load angle compared to a conventional PA. In this way, the proposed load insensitive PA can keep ACLR under -37 dBc all over the load angle at 2.5:1 voltage standing wave ratio (VSWR).

RTU2B-3 10:50
A WLAN RF CMOS PA with Adaptive Power Cells

Taehwan Joo[1], Bonhoon Koo[2], Songcheol Hong[1]; [1]KAIST, Korea, [2]Qualcomm, USA

Abstract: A CMOS linear PA for IEEE 802.11 b/g applications is implemented in a 0.13 μm process including all matching networks. An adaptive power cell (APC) scheme is proposed to achieve

high linear output power and efficiency and applied to the PA, which delivers the output power of 20.5(19.5) dBm with the PAE of 20.2(17.5)% for an 802.11g modulated signal with the EVMs at -25(-28) dB.

RTU2B-4 11:10

A Ka-Band Doherty Power Amplifier with 25.1dBm Output Power, 38% Peak PAE and 27% Back-Off PAE

Jeffery Curtis[1], Anh-Vu Pham[1], Mohan Chirala[2], Farshid Aryanfar[2], Zhouyue Pi[2]; [1]Davis Millimeter-Wave Research Center, USA, [2]Samsung, USA

Abstract: We present the design and development of the first fully integrated, two stage Doherty power amplifier (DPA) in the Ka-Band. The DPA is fabricated in a 0.15-μm GaAs pseudomorphic high electron mobility transistor (pHEMT) process. At 26.4 GHz, the amplifier achieves measured small signal gain of 10.3 dB, output power at 1-dB compression point (P_{1dB}) of 25.1 dBm, peak power added efficiency (PAE) of 38%, and PAE of 27% at 6 dB back-off power. To the best of the author's knowledge, this Doherty circuit is the first fully integrated millimeter-wave amplifier that achieves the highest power and a recorded 27% PAE at 6-dB back-off and each unit amplifier has 2 stages.

RTU2B-5 11:30

High Efficiency GaN Switching Converter IC with Bootstrap Driver for Envelope Tracking Applications

Young-Pyo Hong[1], Kenji Mukai[1], Hamed Gheidi[1], Shintaro Shinjo[2], Peter M. Asbeck[1]; [1]University of California at San Diego, USA, [2]Mitsubishi Electric Corporation, Japan

Abstract: In this paper, we report a DC/DC converter based on GaN HEMT's with a switching frequency of 200 MHz that can be used to generate envelope-modulated power supply voltages for use in envelope tracking power amplifiers. The converter consists of switching circuits using 0.25-μm GaN HEMTs, inductor, and low pass filter, and can provide output voltages above 28V. An integrated bootstrap driver of the switching circuits is employed in order to reduce DC power consumption of the driver stage. Generation of envelope power supply voltages for 20 MHz LTE signals was demonstrated using 200 MHz switching rates with efficiency of 73% (including dissipation in final and driver stages). The chip size is 1075×990 um^2.

Tuesday, 4 June 2013
10:10–11:50
Room 611-612
Session RTU2C: Millimeter-Wave Beamforming and Power Combining Techniques

Chair: Arun Natarajan, Oregon State University
Co-Chair: Pierre Busson, STMicroelectronics

RTU2C-1 10:10
A 45GHz CMOS Transmitter SoC with Digitally-Assisted Power Amplifiers for 64QAM Efficiency Improvement

Tim LaRocca[1], Yi-Cheng Wu[1], Rob Snyder[1], Jasmine Patel[1], Khanh Thai[1], Colin Wong[1], Yeat Yang[1], Leland Gilreath[1], Monte Watanabe[1], Hao Wu[2], Mau-Chung Frank Chang[2]; [1]Northrop Grumman, USA, [2]University of California at Los Angeles, USA

Abstract: A 45GHz 64QAM system-on-chip (SoC) CMOS transmitter with digitally-assisted power amplifiers (DAPA) is presented. The SoC includes a 7M gate ASIC with 9b reconfigurable symbol mapping, 8X upsampling, 161tap pulse shape filtering, IQ imbalance correction and DAPA envelope/time estimation. The ASIC feeds two 10b IQ current-steering DACs and active IQ modulator. A unique transformer splitting up converter drives eight parallel combined DAPAs. The chip is packaged in aluminum housing with WR22 outputs. A 64QAM signal achieves 1.8% EVM with 33dBc ACPR at 45GHz. The data rate is 450Mbps and the integrated output power exceeds -10dBm.

RTU2C-2 10:30
A 163–180GHz 2×2 Amplifier-Doubler Array with Peak EIRP of +5dBm

F. Golcuk, J.M. Edwards, B. Cetinoneri, Y.A. Atesal, Gabriel M. Rebeiz; University of California at San Diego, USA

Abstract: This paper presents a 2×2 amplifier-multiplier array with on-chip antennas at 163–180 GHz in 45 nm CMOS SOI technology. The measured EIRP is > 2 dBm at 165–175 GHz with a peak value of 5 dBm at 170 GHz meeting the stringiest metal-density rules for antennas. The amplifier-multiplier architecture is scalable to N×M arrays for high EIRP and transmit power.

RTU2C-3 10:50
A Self-Steering I/Q Receiver Array in 45-nm CMOS SOI

Arpit K. Gupta, James F. Buckwalter; University of California at San Diego, USA

Abstract: A novel I/Q receiver array is demonstrated that adapts phase shifts in each receive channel to point a receive beam toward an incident RF signal. The measured array operates at 8.1 GHz and covers steering angles of +/-35 degrees for a four element array. Additionally, the receiver incorporates an I/Q down-converter and demodulates 64-QAM with EVM less than 4%. The chip is fabricated in 45 nm CMOS SOI process and occupies an area of 3.45mm^2 while consuming 143 mW dc power.

RTU2C-4 11:10

75–85GHz Flip-Chip Phased Array RFIC with Simultaneous 8-Transmit and 8-Receive Paths for Automotive Radar Applications

Bon-Hyun Ku, Ozgur Inac, Michael Chang, Gabriel M. Rebeiz; University of California at San Diego, USA

Abstract: This paper presents the first simultaneous 8-transmit and 8-receive paths 75–85 GHz phased array RFIC for FMCW automotive radars. The receive path has two separate I/Q mixers each connected to 4-element phased arrays for RF and digital beamforming. The chip also contains a build-in-self-test system (BIST) for the transmit and receive paths. Measurements on a flip-chip prototype show a gain >24 dB at 77 GHz, -25 dB coupling between adjacent channels in the transmit and receive paths (<-45 dB between non-adjacent channels), and <-50 dB coupling between the transmit and receive portions of the chip.

RTU2C-5 11:30

A Fully-Integrated Dual-Polarization 16-Element W-Band Phased-Array Transceiver in SiGe BiCMOS

Alberto Valdes-Garcia[1], Arun Natarajan[2], Duixian Liu[1], Mihai Sanduleanu[1], Xiaoxiong Gu[1], Mark Ferriss[1], Benjamin Parker[1], Christian Baks[1], J.-O. Plouchart[1], Herschel Ainspan[1], Bodhisatwa Sadhu[1], MD. R. Islam[1], Scott Reynolds[1]; [1]IBM, USA, [2]Oregon State University, USA

Abstract: This paper presents a multi-function, dual-polarization phased array transceiver supporting both radar and communication applications at W-band. 32 receive elements and 16 transmit elements with dual outputs are integrated to support 16 dual polarized antennas in a package. The IC further includes two independent 16:1 combining networks, two receiver down-conversion chains, an up-conversion chain, a 40GHz PLL, an 80GHz frequency doubler, extensive digital control circuitry, and on-chip IF/LO combining/distribution circuitry to enable scalability to arrays at the board level. The fully-integrated transceiver is fabricated in the IBM SiGe BiCMOS 0.13μm process, occupies an area of 6.6×6.7mm^2, and operates from 2.7V (analog/RF) and 1.5V (digital) supplies. Multiple operating modes are supported including the simultaneous reception of two polarizations with a 10GHz IF output, transmission in either polarization from an IF input, or single-polarization transmission/reception from/to I&Q base-band signals (2.5W RX, 2.9W TX). Measurement results show 8dB receiver NF and 2dBm transmitter output power per element at 94GHz in both polarizations.

Tuesday, 4 June 2013
10:10–11:50
Room 613-614
Session RTU2D: Advanced Silicon Devices for High Speed, High Power, ESD and MEMS Applications

Chair: Aditya Gupta, Northrop Grumman
Co-Chair: Richard Chan, BAE Systems

RTU2D-1 10:10

A 130nm SiGe BiCMOS Technology for mm-Wave Applications Featuring HBT with f_T/f_{MAX} of 260/320GHz

Panglijen Candra, Vibhor Jain, Peng Cheng, John Pekarik, R. Camillo-Castillo, Peter Gray, Thomas Kessler, Jeffrey Gambino, James Dunn, David Harame; IBM, USA

Abstract: A manufacturable 130nm SiGe BiCMOS RF technology for high-performance mm-wave analog applications having a high-speed SiGe Heterojunction Bipolar Transistor (HBT) integrated into a full-featured RFCMOS is presented. The technology features a high performance (HP) SiGe HBT with f_T/f_{MAX} of 260/320 GHz, a high breakdown (HB) HBT with BV_{CEO} of 3.5V, 130nm RF CMOS, and a full suite of passive devices. Specific device results pertaining to this BiCMOS8XP technology are discussed in this paper.

RTU2D-2 10:30

Power Handling Capability of an SOI RF Switch

Alvin Joseph, Alan Botula, James Slinkman, Randy Wolf, Rick Phelps, Michel Abou-Khalil, John Ellis-Monaghan, Steven Moss, Mark Jaffe; IBM, USA

Abstract: In this study, we define and investigate the maximum power handling capability (Pmax) in an SOI RF shunt branch switch. One of the critical factor in the Pmax is the non-uniform voltage division across an OFF shunt branch. In this study we provide a simple analytical method to determine the stack voltage imbalance. The Pmax is characterized as a function of various parameters, such as, switch stack height, channel length, Gate and Body bias, and process parameters. Overall, we find that the Pmax can be improved by reducing stack imbalance as well as device leakage currents, namely, GIDL.

RTU2D-3 10:50

Nano Switching Crossbar Array ESD Protection Structures

X. Wang, Z. Shi, J. Liu, L. Wang, R. Ma, H. Zhao, Z. Dong, C. Zhang, Albert Wang; University of California at Riverside, USA

Abstract: We report a new nano-switching ESD protection mechanism and dual-polarity Cu/$Si_xO_yN_z$/W nano crossbar array ESD structures. Experiments show full ESD protection featuring fast response of 100pS, ultra low leakage of <2pA and ESD protection of >9A. New dispersed local ESD tunneling model and CMOS integration are reported.

RTU2D-4 11:10

Reconfigurable Sensors for Extraction of Dielectric Material and Liquid Properties

Laurent Leyssenne[1], Sidina Wane[1], Damienne Bajon[2], Philippe Descamps[1], Rosine Coq-Germanicus[1]; [1]NXP Semiconductors, France, [2]Université de Toulouse, France

Abstract: This paper proposes an analysis and modeling of a reconfigurable sensor for the non-destructive remote extraction and monitoring of dielectric material and liquid properties, towards substance identification or distribution cartography.

RTU2D-5 11:30

A Sticking-Free and High-Quality Factor MEMS Variable Capacitor with Metal-Insulator-Metal Dots as Dielectric Layer

Fumihiko Nakazawa, Takeaki Shimanouchi, Takashi Katsuki, Osamu Toyoda, Satoshi Ueda; ASET, Japan

Abstract: This paper describes a novel design of a MEMS variable capacitor with high operating reliability and high quality factor. Metal-Insulator-Metal (MIM) dots between a fixed electrode and a movable electrode in a variable capacitor is proposed. A Fabricated MEMS capacitor was operated one billion or more times without sticking. It demonstrated a high quality factor of 200 at 0.5 pF. It was experimentally confirmed that MIM dots effectively achieve a sticking-free and high-quality-factor MEMS variable capacitor.

Tuesday, 4 June 2013
13:30–17:00
Room 6E
Session RTUIF: Interactive Forum
Chair: David Wentzloff, University of Michigan
Co-Chair: Danilo Manstretta, University of Pavia

RTUIF-1 13:30
A 71GHz RF Energy Harvesting Tag with 8% Efficiency for Wireless Temperature Sensors in 65nm CMOS

Hao Gao, Marion K. Matters-Kammerer, Pieter Harpe, Dusan Milosevic, Ulf Johannsen, Arthur van Roermund, Peter Baltus; Technische Universiteit Eindhoven, The Netherlands

Abstract: This paper presents the first monolithically integrated RF-power harvesting 71 GHz wireless temperature sensor node in 65nm CMOS technology, containing a monopole antenna, a 71 GHz RF power harvesting unit with storage capacitor array, an End-of-Burst monitor, a temperature sensor and an ultra-low-power transmitter at 79 GHz. At 71 GHz, the RF to DC converter achieves a power conversion efficiency of 8% for 5 dBm input power.

RTUIF-2 13:30
A Compact Millimeter-Wave Energy Transmission System for Wireless Applications

Med Nariman[1], Farid Shirinfar[2], Sudhakar Pamarti[2], Maryam Rofougaran[3], Reza Rofougaran[3], Franco De Flaviis[1]; [1]University of California at Irvine, USA, [2]University of California at Los Angeles, USA, [3]Broadcom, USA

Abstract: A compact energy transmission system in 40nm standard CMOS is presented. The system consists of a 60GHz VCO followed by a quad-core power amplifier as transmitter and an RF-to-DC converter as receiver. The total power delivered by the quad-core PA to its four 50Ω loads is 24.6dBm. The receiver is a complementary cross-coupled rectifier with a measured efficiency of 28% while supplying 1mA of current. The system can support amplitude and frequency modulations and beam-forming capabilities for wireless applications with minimal front-end complexities.

RTUIF-3 13:30
A 0.5GHz–1.5GHz Order Scalable Harmonic Rejection Mixer

Teng Yang, Karthik Tripurari, Harish Krishnaswamy, Peter R. Kinget; Columbia University, USA

Abstract: In this paper, a harmonic rejection mixer architecture capable of operating for a wide range of LO frequencies is demonstrated. The mixer can be configured to suppress any particular harmonic of the LO or multiple harmonics simultaneously. The level of suppression of each harmonic is controlled by a set of independent gain and phase tuning parameters. Feasibility of extension of this concept to higher order harmonics is also demonstrated.

A proof-of-principle prototype has been designed and fabricated in a 45nm SOI technology. Experimental results demonstrate an operation range of 0.5GHz to 1.5GHz for the LO frequency while offering harmonic rejection better than 55dB for the 3rd harmonic and 58dB for the 5th harmonic

across LO frequencies. The mixer consumes 17mW of power from a 1V power supply while occupying an area of 0.352mm^2.

RTUIF-4 13:30

V-Band Dual-Conversion Down-Converter with Low-Doped N-Well Schottky Diode in 0.18μm CMOS Process

Yu-Chih Hsiao[1], Chinchun Meng[1], Hung-Ju Wei[1], Ta-Wei Wang[1], Guo-Wei Huang[2], Mau-Chung Frank Chang[3]; [1]National Chiao Tung University, Taiwan, [2]National Nano Device Laboratories, Taiwan, [3]University of California at Los Angeles, USA

Abstract: In this paper, a V-band dual-conversion down-converter with a silicon-based Schottky diode using low-doped N-well for DC and RF characteristics optimization is demonstrated in standard 0.18 μm CMOS technology. A triple-balanced subharmonic Schottky diode microwave mixer and a double-balanced resistive analog mixer are employed as the first conversion mixer and the second conversion mixer, respectively. As a result, the conversion gain is about -1 dB in the range of 45~64 GHz. The noise figure is about 20 dB, IP_{1dB} is about -5 dBm and IIP3 is about 5 dBm. The total power consumption is 92.4 mW at 2.5 V supply voltage.

RTUIF-5 13:30

A Fully Digital PWM-Based 1 to 3GHz Multistandard Transmitter in 40-nm CMOS

Pieter A.J. Nuyts, Patrick Reynaert, Wim Dehaene; Katholieke Universiteit Leuven, Belgium

Abstract: A fully digital 1 to 3 GHz multimode transmitter is presented which contains two RF modulators: One uses baseband (BB) PWM, while the other uses RF PWM. RF PWM produces less harmonics, while BB PWM has a higher dynamic range (DR) and consumes less power. The BB PWM system satisfies the WLAN EVM limit over the whole frequency range. The RF PWM system achieves sufficient EVM for standards such as EDGE and WCDMA. Both systems support the use of multiple PAs to extend the DR using multilevel PWM.

RTUIF-6 13:30

An UWB CMOS Impulse Radar

Chenliang Du, Hossein Hashemi; University of Southern California, USA

Abstract: This paper presents an integrated UWB short-range impulse radar implemented in a 130 nm CMOS process. The transmitter can digitally generate various waveforms with up to 10 GHz bandwidth at 5 dBm peak power. The receiver utilizes a time interleaved scheme to support a 20 GS/s effective sampling rate. Sample-domain averaging of multiple identical received waveforms reduces the required digitization rate and corresponding power consumption. Sampling clocks for the time interleaved samplers are generated using independent delay locked loops that are locked to the same reference. Measurement results of the individual blocks as well as the entire system are presented.

RTUIF-7 13:30

Simultaneous Linearity and Efficiency Enhancement of a Digitally-Assisted GaN Power Amplifier for 64-QAM

Monte Watanabe, Rob Snyder, Tim LaRocca; Northrop Grumman, USA

Abstract: The first dynamic 4-bit, digitally-assisted GaN high power amplifier (DAPA) system transmitting 7.68-Msymbol/s with 64-QAM modulation is presented. An FPGA is programmed to generate the pulse-shaped 64-QAM signal, perform envelope estimation, and time-align the RF and digital control signals arriving at the DAPA. A high-speed, level-shifting circuit converts the FPGA's low-voltage differential signaling (LVDS) DAPA control signals into single-ended logic levels required for the depletion-mode GaN HEMT DAPA auxiliary cells. Measured results show 9.6% DC power savings, 23% improved PAE, and 23% higher output power at 4% EVM_{RMS} compared to the static PA configuration.

RTUIF-8 13:30

A Low-Noise FBAR-CMOS Frequency/Phase Discriminator for Phase Noise Measurement and Cancellation

Alireza Imani, Hossein Hashemi; University of Southern California, USA

Abstract: A sensitive low-noise frequency/phase discriminator and its applications in phase noise measurement and phase noise cancellation are presented. The discriminator uses a high quality factor thin Film Bulk Acoustic Resonator (FBAR) in a notch filter configuration with common-mode traps to reduce the low-frequency noise up-conversion. The performance of the notch filter, the discriminator transfer function, output noise, and phase noise floor are measured and compared with simulations. A feed-back feed-forward phase noise cancellation scheme is proposed based on the frequency/phase discriminator. Two chips were fabricated in 0.13 μm CMOS technology integrating the discriminator and the phase noise cancellation schemes, respectively. The 1.5 GHz discriminator shows phase noise floor of -128 dBc/Hz at 20 kHz, -142 dBc/Hz at 100 kHz, -162 dBc/Hz at 1 MHz and -166 dBc/Hz at 4 MHz, while consuming 26 mW of power. The measured phase noise of the feedback cancellation circuitry reaches the phase noise floor of the discriminator, verifying the proposed concepts.

RTUIF-9 13:30

A 36GHz/mW Single-Phase Prescaler Using Implication Logic in 0.13μm CMOS

Elkim Roa, Wu-Hsin Chen, Byunghoo Jung; Purdue University, USA

Abstract: This paper presents a non-Boolean digital logic technique used in the design of a high-speed and low-power frequency prescaler. Maximum achievable frequency input of prescalers is limited by the number of devices connected in cascade to the high-speed signal path. In this work, a reduced number of devices is obtained in the prescaler by realizing implication logic operators with a single-phase digital-based flip-flop. The prescaler is implemented in 0.13μm CMOS with a 1.2V supply. A measured efficiency of 36GHz per mW is achieved which represents 3X power consumption reduction compared to prior art in the same technology node, and the highest efficiency reported.

RTUIF-10 13:30

A Sub-1mW 5.5-GHz PLL with Digitally-Calibrated ILFD and Linearized Varactor for Low Supply Voltage Operation

Sho Ikeda, Tatsuya Kamimura, Sangyeop Lee, Hiroyuki Ito, Noboru Ishihara, Kazuya Masu; Tokyo Institute of Technology, Japan

Abstract: This paper proposes an ultra-low-power 5.5-GHz PLL which employs a divide-by-4 injection-locked frequency divider (ILFD) and linearity-compensated varactor for low supply voltage operation. The digital calibration circuit is introduced to control the ILFD frequency automatically. The proposed varactor, which applies a forward-body-bias (FBB) technique, is employed for linear-frequency-tuning under the power supply of 0.5V.

The proposed PLL was fabricated in 65nm CMOS. With a 34.3-MHz reference, it shows a 1-MHz-offset phase noise of -106 dBc/Hz, a reference spur level lower than -65 dBc, and the total power consumption of 950 μW at 5.5 GHz.

RTUIF-11 13:30

Effect of Drift Region Resistance on Temperature Characteristics of RF Power LDMOS Transistors

Kun-Ming Chen[1], Bo-Yuan Chen[1], Hsueh-Wei Chen[1], Chia-Sung Chiu[1], Guo-Wei Huang[1], Chia-Hao Chang[2], Hsin-Hui Hu[2]; [1]National Nano Device Laboratories, Taiwan, [2]National Taipei University of Technology, Taiwan

Abstract: In this work, we investigated the effects of drift region resistance on the temperature behaviors of RF power LDMOS transistors. Devices with various implant doses in the drift region were fabricated. Owing to the quasi-saturation effect, the transconductances at high gate voltages are less dependent on the temperature for low-drift-dose device. In addition, the maximum oscillation frequency exhibits different temperature coefficients for devices with different drift doses. We derived an expression of unilateral power gain with 4^{th}-order frequency term, and found that the drift resistance has a large influence on the device temperature characteristics at high frequencies.

RTUIF-12 13:30

A -78dBm Sensitivity Super-Regenerative Receiver at 96GHz with Quench-Controlled Metamaterial Oscillator in 65nm CMOS

Yang Shang[1], Haipeng Fu[2], Hao Yu[1], Junyan Ren[2]; [1]Nanyang Technological University, Singapore, [2]Fudan University, China

Abstract: One high-sensitivity CMOS super-regenerative receiver is demonstrated for 96GHz mm-wave imaging based on high-Q metamaterial oscillator. Compared to traditional LC-tank based oscillator, the metamaterial oscillator is developed by folded-differential transmission-line loaded complementary split-ring resonator (FDTL-CSRR). With formed sharp stop-band, standing-wave is established with high EM-energy storage at mm-wave region for high-Q oscillatory amplification. As such, one high-sensitivity 96 GHz super-regenerative receiver is realized in 65nm CMOS with measurement results of: -78 dBm sensitivity, 0.67 fW/Hz$^{0.5}$ NEP, 8.5 dB NF, 2.8mW power consumption and 0.014 mm^2 core area.

RTUIF-13 13:30

A T-DMB Mobile TV SoC Tuner with Compact Size, Low Power and BoM in 65nm CMOS

Jeonghoon Lee[1], Shinil Chang[1], Jaehwan Lee[1], Jisun Ryu[2], Kihyeok Ha[3], Yongchang Choi[1], Younghoon Kim[1], Sanghyun Hwang[1], Hongju Song[1], Kiwon Choi[1], Sangyoub Lee[1]; [1]I&C Technology Inc., Korea, [2]Qualcomm, Korea, [3]Samsung, Korea

Abstract: This paper presents a direct conversion Korean standard T-DMB SoC tuner using a 65nm low power CMOS technology with the best feature of size, power and BoM ever reported. A digital F/E enhanced function is implemented to reduce analog signal processing empowered by oversampled A/D converter, digital channel selection filter and lots of digital calibration blocks. And the designed LNA excludes all required inductors. Thus high voltage gain and low current consumption are achieved due to their high Q factor. A single-to-differential signaling down-conversion mixer is also announced which has well balanced output characteristic. A DC/DC converter is adopted as well for the further low power consuming. The tunable clock frequency scheme of DC/DC buck converter can prevent a degradation of sensitivity performances which is planed value to escape the channel center frequency. This reported SoC tuner consumes only 28mA at maximum gain mode. And -103.5dBm of sensitivity and 48dBc of N±1 adjacent-channel selectivity are achieved also with only 5 external LC components. This SoC occupies 2.5×2.5mm^2 die and WLCSP chip size.

RTUIF-14 13:30

A Highly-Linear CMOS RF Programmable-Gain Driver Amplifier with a Digital-Step Differential Attenuator for RF Transmitters

Sunbo Shim[1], Bonhoon Koo[2], Songcheol Hong[3]; [1]University of California at Los Angeles, USA, [2]Qualcomm, USA, [3]KAIST, Korea

Abstract: This paper presents a CMOS RF programmable-gain driver amplifier (RF PGDA) for wireless transmitters. Digital-step differential attenuators precede a programmable-gain amplifier in order to enhance the dynamic range and to save power consumption, especially at low gain region. The RF PGDA fabricated in 0.13-μm CMOS technology with a 1.2 V supply voltage achieves a dynamic range of 49 dB with a step error of less than 0.5 dB and highly-linearized output satisfying the WCDMA/LTE specifications.

RFIC2013 Panel Sessions

Monday, 3 June 2013
12:00–13:15
WSCC 6BC

Cellular vs. WiFi: Future Convergence or an Utter Divergence?

Panel Organizer and Moderator:
Osama Shana'a (Technical Director, MediaTek)

Panelists: **Eduardo Esteves** (Vice President, Qualcomm)
Mike Hlavaty-LaPosa (Director, AT&T)
Alex Reznik (Senior Director, Inter Digital)
Pablo Tapia (MTS, T-Mobile)
Kambiz Shoarinejad (Associate Technical Director, Broadcom)
Pete Gelbman (Former Director, Clearwire, now independent consultant)

Abstract: In recent years, there has been a tremendous need for high-data rate support by modern wireless communication systems due to end users excessive data usage and demand. On the cellular side, the downlink data rate throughput increased from <20Mbps in 3G HSPA to >100Mbps for 3.9G LTE Rel. 8 (and up to 1Gbps for LTE-A Rel. 10 & beyond). Meanwhile, WiFi data rate throughput also increased from <420Mbps for 802.11n to <4.9Gbps for 802.11ac wave 2. The boom of smart phones and social media services has pushed the need for higher data bandwidth, which subsequently has driven cellular networks to their limits. Cellular operators are now thinking of better ways to offload cellular networks from this extreme data stream demand by users. On one hand, femtocells seem promising because the spectrum can be re-used more frequently over a smaller geographical region, as small as a house, with easy access to the network backbone. On the other hand, WiFi networks are readily available in most homes and are easy to install and manage. Going into future 5G cellular with its higher projected data rates, will cellular networks become self-sufficient through proper micro/femto cell design and so meet the needs of end users to the point that WiFi would seize to exist? Or will cellular networks become limited to voice communication and selected data rate demands while high data rate communication is left to WiFi to handle in coordination with cellular networks?

This panel's distinguished experts from cellular/ WiFi chipset providers, cellular operators, and communication network/infrastructure manufacturers will present their perspectives on the topic above, especially the pros and cons of each approach, what the technical challenges are for future cellular generation network data traffic management, and how cellular and WiFi would ultimately converge (or otherwise diverge).

RFIC2013 Panel Sessions

Tuesday, 4 June 2013
12:00–13:30
WSCC 6A

Universities are from Venus, Industry is from Mars

Panel Organizers and Moderators:
Hossein Hashemi (University of Southern California)
Ali Afshahi (Broadcom)

Panelists: **Lawrence Larson** (Dean, Professor, Brown University)
Ali Hajimiri (Professor, Caltech)
Sorin Voinigescu (Professor, University of Toronto)
David Su (Vice President Engineering, Qualcomm Atheros)
Curtis Ling (Co-Founder and Chief Technical Officer, Maxlinear)
Domine Leenaerts (Senior Principal, NXP Semiconductors)

Abstract: Over the past two decades, the reduction in the number of government and industrial pure research labs and the increased demand from industry for highly-trained graduate students together have led to a large increase in the number and role of research universities and programs. For the most part, industry is unable or unwilling to support university research unless it is targeted for a specific, often near-term, application.

Faculty at universities are struggling to balance their main objective of conducting fundamental research with the need to train more graduate students who have specific skills that are of particular interest to industry. This panel will bring together participants from industry and academia to discuss and debate the role and objectives of university research, to define optimal university-industry interactions from both perspectives and to suggest ways to improve the symbiotic relationship between industry and universities. The panel session will also provide an opportunity for the audience to share their experiences and opinions and contribute to a lively discussion.

WORKSHOPS AND SHORT COURSES

Workshops and Short courses are offered on Sunday, Monday and Friday of Microwave Week. Please see daily handout on Sunday, Monday, and Friday in the registration area and from volunteers throughout the meeting floors to confirm room location.

SUNDAY WORKSHOPS – 2 JUNE 2013

WSA (Half Day): Sunday 13:00–17:00
State-of-the-Art RF and Low Noise CMOS Technologies: From Device to Circuit Level

Sponsors: **MTT-6 Microwave and mm-Wave Integrated Circuits**

Organizers: **Jyh-Chyurn Guo**, *National Chiao-Tung University, Taiwan*
François Danneville, *University of Lille, France*

Abstract: FinFETs appears as the most promising device technology for sub-20nm node, attributed to superior short channel integrity and analog performance. However, the potential impact on RF FoM and noise brings new challenges to RF/mm-wave circuits design on single-chip. Prior to sub-20nm, planar CMOS keeps the best choice for RF/mm-wave SoC. This workshop will present successful examples of low noise RF/mm-wave/THz circuits realized in planar CMOS technology, identify emerging challenges and solutions.

Speakers:

1. "The Impact of Layout Dependent Effects and Strain Engineering on High Frequency Performance and Low Frequency Noise in Nanoscale MOSFETs", Jyh-Chyurn Guo, National Chiao Tung University, Taiwan
2. "Millimeter-Wave Ultra-Broadband CMOS LNAs Using Noise Reduction and Linearity Enhancement Techniques", Tian-Wei Huang, National Taiwan University, Taiwan
3. "FinFET Technology for Analog/RF and mm-Wave Applications", Morin Dehan, IMEC, Belgium
4. "Design Considerations for High-Frequency Low-Noise Integrated Circuits in Nanoscale (Bi)CMOS", Payam Heydari, University of California at Irvine, USA

WSB (Full Day): Sunday 08:00–17:00
High Efficiency Supply-Modulated RF Power Amplifier

Sponsor: **RFIC**

Organizers: **Donald Lie**, *Texas Tech University, USA*
Nick Cheng, *Skyworks Solutions, USA*

Abstract: Broadband 3G/4G/WLAN wireless standards utilize inherent spectral-efficient modulation schemes with high peak-to-average power ratios (PAPR) and wide bandwidth, demanding highly linear RF PA design techniques that can offer excellent power-added efficiency (PAE) at both the maximum peak power and the back-off output power levels for mobile applications. As suggested by the recent market trends and the technical literature, the dynamic power-supply modulation schemes (e.g., the envelope-elimination-and-restoration (EER) and the envelope-tracking (ET)) are among the most effective methods for RF PA efficiency enhancement at both peak and back-off output power modes.

Eight world experts from both industry and academia will present the latest design techniques, research, and market trends of high efficiency supply-modulated RF power amplifiers in this workshop. Topics such as "the linearity and efficiency trade-offs, design techniques for integrated ultra-high efficiency wideband supply modulators for RFIC applications", "Co-design of power amplifier and dynamic power supplies for radar and communications transmitters", etc., will be presented. In addition, the switching noise concerns for the envelope-tracking power amplifier (ET-PA), circuits/system design techniques and bandwidth requirements will be discussed in this workshop to address the practical issues in realizing successful supply-modulated high-efficiency RF PA systems.

Speakers:

1. "Design Techniques for Integrated Ultra-High Efficiency Wideband Supply Modulators for RFIC Applications", **Larry Larson**, *Brown University, USA*
2. "High Efficiency Supply-Modulated RF Power Amplifier for Handset Applications", **Bumman Kim**, *POSTECH, Korea*
3. "Design Considerations for Wideband Envelope Tracking Power Amplifiers", **David Ripley**, *Skyworks Solutions, USA*
4. "Power Amplifier Design Techniques for Envelope Tracking", **James Retz**, *RF Micro Devices, USA*
5. "Design of Monolithic Silicon-Based Envelope-Tracking Power Amplifiers for Broadband Wireless Applications", **Donald Lie**, *Texas Tech University, USA*
6. "Co-Design of Power Amplifier and Dynamic Power Supplies for Radar and Communications Transmitters", **Zoya Popovic**, *University of Colorado at Boulder, USA*
7. "Digital Signal Processing for Envelope Tracking Systems", **Paul Draxler**, *Qualcomm, USA*
8. "Envelope Tracking and Energy Recovery Concepts for RF Switch-Mode Power Amplifiers", **Thomas Johnson**, *University of British Columbia, Canada*

WSC (Half Day): Sunday 08:00–12:15

Interference Robust Radio Receiver Techniques

Sponsor: **RFIC**

Organizers: **Eric Klumperink**, *University of Twente, The Netherlands*
Didier Belot, *STMicroelectronics, France*

Abstract: The radio spectrum becomes more and more crowded, and radio devices become interference limited. As there is a demand for multi-mode flexible radio devices, traditional dedicated narrowband filtering is no longer enough and new techniques are wanted for interference rejection.

This workshop will review different approaches to address this challenge, e.g. interference cancellation techniques, linearization, spatial interference rejection via multiple antennas, flexibly tunable N-path filtering.

Speakers:

1. "Linearity Enhancement Techniques in Radio Receiver Front-Ends", **Ranjit Gharpurey**, *University of Texas at Austin, USA*
2. "Translational Loop Filtering for Interferer Rejection at the LNA Input", **Andreas Kaiser**, *IEMN, France*
3. "Mixer-First Receivers with High Out-of-Band Linearity", **Caroline Andrews**, *Passif Semiconductor, USA*
4. "Blocker Tolerant N-Path Filter Techniques", **Ahmad Mirzaei**, *Broadcom, USA*
5. "Spatial Interference Rejection in Multi-Antenna CMOS Radio Receivers", **Michiel Soer**, *University of Twente, The Netherlands*

WSD (Full Day): Sunday 08:00–17:00

Pushing the Ultimate Performance Limits of RF CMOS

Sponsor: **RFIC**

Organizers: **Gernot Hueber**, *NXP Semiconductors, Austria*
R. Bogdan Staszewski, *TU Delft, The Netherlands*

Abstract: Advances in CMOS fabrication technology have enabled the use of CMOS technology in today's RF transceivers for wireless communications. Multi-band and multi-mode radios covering the diversity of communication standards from cellular (2G, GSM, 3G UMTS, to 4G LTE and LTE-advanced) through Bluetooth and WLAN to GPS, etc., impart unique challenges on the RF-transceiver design due to limitations in terms of reconfigurable RF components that meet the demanding RF performance criteria at costs that are attractive for mass market applications.

The focus of this workshop will be to discuss the performance limits of key RF building blocks in CMOS such as oscillators with minimal phase noise, transmitters with maximum modulation rate, and best linearity for the RX.

Approaches include novel architectures, highly configurable analog circuitry, digitally assisted and enhanced analog/RF modules and the integration of digital signal processing into the traditionally purely analog front-end.

Speakers:

1. "System Requirements Pushing the Limits of RF CMOS", **Walid Y. Ali-Ahmad**, *MediaTek, Singapore*
2. "Pushing the Spurious Free Dynamic Range of CMOS RF Front-Ends", **Eric Klumperink**, *University of Twente, The Netherlands*

3. "Pushing the Power in Digital Transmitters", **Jan Craninckx**, *IMEC, Belgium*
4. "Limitations in CMOS Polar PAs", **Jeff Walling**, *University of Utah, USA*
5. "Pushing the Limits of Frequency Synthesizers to Ultra-Low Phase Noise, Spur-Free and mm-Wave", **R. Bogdan Staszewski**, *TU Delft, The Netherlands*
6. "Design of Low-Power RF Circuits in Deep-Submicron CMOS", **Christian Enz**, *CSEM, Switzerland*
7. "Filtering Aspects of an All-Digital Transceiver for Mobile Applications", **Frank Op 't Eynde**, *Audax Technologies, Belgium*
8. "Digital RF Signal Generation for Ultimate Transmitters", **Antoine Frappé**, *IEMN, France*

WSE (Half Day): Sunday 13:00–17:00

Inductor-Less and Noise/Distortion Cancellation and Mitigation Techniques in RF Circuit Design

Sponsor: **RFIC**

Organizers: **Danilo Manstretta**, *University of Pavia, Italy*
Osama Shana'a, *MediaTek, USA*

Abstract: In recent years inductor-less and noise/distortion cancelling design techniques have emerged as key innovations in RF circuit design to improve performance, lower power dissipation, reduce circuit area and save cost. This workshop attempts to provide an overview on the following topics:

1. History and evolution of thermal noise canceling in LNAs and receivers
2. Wideband LNA linearization techniques
3. Blocker and Distortion Cancellation Techniques for 3G/4G Full-duplex Systems
4. PLL noise and spur reduction based on sub-sampling phase detection
5. Nonlinearity mitigation in digital PLLs

Speakers:

1. "Thermal Noise Canceling in LNAs and Receivers: history and developments", **Eric Klumperink**, *University of Twente, The Netherlands*
2. "Linearization Techniques for CMOS Low Noise Amplifiers: A Tutorial", **Heng Zhang**, *Texas A&M University, USA*
3. "Blocker and Distortion Cancellation Techniques for 3G/4G Full-Duplex Systems", **Mohyee Mikhemar**, *Broadcom, USA*
4. "PLL Noise and Spur Reduction Techniques Based on Sub-Sampling Phase Detection", **Xiang Gao**, *Marvell Semiconductor, USA*
5. "Non-Linearity Mitigation in Digital PLLs for High-Performance Transmitters", **Salvatore Levantino**, *Politecnico di Milano, Italy*

WSF (Half Day): Sunday 13:00–17:00

RF Assisted Medicine

Sponsor: **RFIC**

Organizers: **Hua Wang**, *Georgia Institute of Technology, USA*
Sayfe Kiaei, *Arizona State University, USA*

Abstract: With the rapid growth of novel integrated sensors, low-power circuits/systems, and energy-efficient wireless communications, radio-frequency (RF) technology has become one of the major enabling factors for future personalized healthcare. This workshop, entitled "RF Assisted Medicine", is designated to showcase the state-of-the-art technologies in this fast evolving area. We will cover two major and highly correlated topics in this program – RF medically implanted sensors and wireless body area networks (WBAN). The first topic focuses on providing high-performance in vivo sensing and actuation as well as information/power transmission between internal and external devices on the human body, while the second topic aims at establishing efficient wireless communications among multiple miniaturized body sensor units (BSU) and a single body central unit (BCU). The synergistic integration of the two technologies has the potential to enable a plethora of diagnostic and therapeutic applications in future medical care. In order to provide a high-quality education opportunity for the attendees while maintaining a coherent theme, we propose to organize the workshop with four related sessions as follows.

1. Overview of RF technologies in assisted medicine. This session will serve as a high-level review on the field and emphasis on the various applications which utilize RFIC to assist the medicine and a healthy living of the users. Topics including top-level market size/trend, current medical applications, technologies, and system architectures will be covered. This talk therefore serves as an introduction for the workshop and demonstrates the high-level pictures of this rapidly growing field.
2. Power and Data Transmission to Implantable Microelectronic Devices. This talk will focus on how to establish the wireless link into/from inside the body (IMD). Fundamentals of efficient power and wireless data transmission into/from the body will be presented, which is a perfect example of how RF technologies are used in assisted medical applications. This wireless power and data transmission technology is also the core part of many implantable medical electronics. Moreover, design optimization procedures, using two-, three-, and four-coil resonant systems, will be discussed to achieve the highest possible power transmission efficiency. Some of the latest techniques will also be reviewed to establish wideband bidirectional communication links across the skin.
3. WBAN: Medical Applications and Challenges. In parallel to the wireless links across the skin, this session will present another aspect of how to establish energy-efficiency wireless link outside of the body based on Wireless Body Area Networks (WBANs), which is another example of how RF technologies will assist medical applications. This talk will first provide an overview of WBANs, including emerging medical applications and recent standards activity. Challenges and opportunities for WBANs systems will be discussed, including areas where current technology falls short and innovations are required in order to meet targets for reliability, security, and sensor lifetime.
4. Wireless Real-Time Monitoring of Brain Neurochemistry. This presentation will focus on a key example application of RF assisted medicine which performs chemical recording

for neural engineering. The presented wireless real-time monitoring technology achieves high-Mbps data transmission over meter-range distances. The talk will first introduce neural engineering applications and describe the fundamentals of brain interfacing. Then it will showcase one example of engineered devices for real-time, concurrent sensing of neurochemical signals and electrical action potentials in mouse brains. Various design/implementation challenges due to high-site-density wireless monitoring will be highlighted, and emerging wireless communication technologies to potentially address these challenges will be discussed.

Speakers:

1. "Wireless Medical Systems: Concepts and Applications", **Tim Denison**, *Brown University, USA*
2. "Transcutaneous Power and Data Transmission to Implantable Microelectronic Devices", **Maysam Ghovanloo**, *Georgia Institute of Technology, USA*
3. "WBAN:Medical Applications and Challenges", **David Wentzloff**, *University of Michigan, USA*
4. "Wireless Real-Time Monitoring of Brain Neurochemistry", **Pedram Mohseni**, *Case Western Reserve University, USA*

WSG (Full Day): Sunday 08:00–17:00

Radio Frequency Systems for Indoor Localization

Sponsor: **RFIC**

Organizers: **Aly E. Fathy**, *University of Tennessee, USA*
Martin Vossiek, *University of Erlangen-Nuremberg, Germany*

Abstract: Radio frequency systems for indoor localization pose many challenges in RFIC design, since they combine broadband radar, communication and high precision synchronization techniques. In addition, powerful real time signal processing capabilities are needed for signal evaluation, multipath mitigation and sensor fusion. During the last years tremendous development efforts could be noticed in the area of indoor local positioning system. The workshop will cover RFIC design as well as system design aspects and will show recent applications of Radio Frequency Systems for Indoor Localization.

Speakers:

1. "Impulse-Radio UWB Systems for In-Body Localization and Vital Sign Monitoring", **Hermann Schumacher**, *Ulm University, Germany*
2. "24GHz CMOS Transceiver and Wireless Sensor Network for Indoor Localization – Part A Transceiver Design", **Amin Hamidian**, *Berlin University of Technology, Germany*
3. "24GHz CMOS Transceiver and Wireless Sensor Network for Indoor Localization – Part B Sensor Network and Measurement Results", **Randolf Ebelt**, *University of Erlangen-Nuremberg, Germany*

4. "Ultra Wide Band Indoor Precise Localization Systems", **Aly E Fathy**, *University of Tennessee, USA*
5. "CMOS micro-radars for noncontact detection of human vital signs", **Jenshan Lin**, *University of Florida, USA*
6. "UWB Real Time Locating Systems", **Tim Harrington**, *Zebra Technologies, USA*
7. "Impulse Radio for Accurate Indoor Localization", **Xiaoyan Wang**, *Holst Centre, The Netherlands*
8. "Ultra Wideband Ranging Radio Transceiver for Indoor Localization", **Brandon Dewberry**, *Time Domain, USA*
9. "Localization of Standard Compliant Passive RFID Transponders", **Robert Miesen**, *University of Erlangen-Nuremberg, Germany*

WSH (Full Day): Sunday 08:00–17:00

Self-Healing Mixed-Signal Circuitry: Built-In Calibration and Compensation Techniques

Sponsor: **RFIC**

Organizers: **Oren Eliezer**, *Xtendwave, USA*
Ali Afsahi, *Broadcom, USA*
Sudipto Chakraborty, *Texas Instruments, USA*

Abstract: Current day system-on-chip (SoC) RFICs are expected to reliably deliver high performance at low cost, while design cycles of these highly complex products are short and limited in design resources.

Furthermore, a typical SoC in a consumer-market device, such as a cellphone transceiver, is characterized by substantial digital content, including digital processing power and memory, for which high production yield and low testing costs are expected.

Hence, the analog/mixed-signal circuitry in these products, while typically being designed under tight schedules and with limited resources, must meet demanding performance specifications across all corners of the fabrication process, while also allowing for low-cost testing and high production yield. This combination of requirements can be met only if the analog/mixed-signal circuitry accommodates built-in calibration and compensation mechanisms, allowing it to "self-heal" in scenarios where it may fail due to variations in fabrication process, operating conditions, or aging.

The implementation of built-in calibration/compensation involves the capabilities of built-in measurements, as well as signal processing and parameter adjustment (current, voltage, timing, capacitance, etc.), which may be of high complexity. However, such resources can be made affordably available on the SoC, making this design approach an increasingly popular one in the industry.

The workshop includes a total of 8 talks, provided by industry experts and academia researchers, covering the fundamentals of the "self-healing" design approach, many successful implementation examples demonstrating the approach within various industry leaders, and theoretical analysis related modeling and reliability.

The workshop's comprehensive coverage of the topic and its interactive nature, will allow attendees to ask questions and share ideas about all aspects of this topic, and to ultimately become better equipped in making design and design-management decisions in future RFIC SoCs.

Speakers:

1. "Adaptive Digital Pre-Distortion for ET Transmitters", **Paul Draxler**, *Qualcomm, USA*
2. "Loop-Back Design and Applications as the Foundation for BIST and BISC", **Christopher Hull**, *Intel, USA*
3. "Design of Self-Calibration Solutions in Low Power RF Transceivers", **Sudipto Chakraborty**, *Texas Instruments, USA*
4. "Reliability Analysis, Built-In Monitoring, and Modeling of Aging and Failures in RF/Analog Circuits", **Sule Ozev**, *Arizona State University, USA*
5. "Modeling and Self-Healing of Analog/RF Circuits: A Statistical Approach", **Xin Li**, *Carnegie Mellon University, USA*
6. "Calibration and Compensation Techniques for Wireless Transceivers", **Theodoros Georgantas**, *Broadcom, USA*
7. "Self-Healing Mixed-Signal Circuitry: Built-in Calibration and Compensation Techniques", **Jose Silva-Martinez**, *Texas A&M University, USA*
8. "Built-In Digital Calibration/Compensation in Low Cost RF SoCs", **Oren Eliezer**, *Xtendwave, USA*

WSI (Half Day): Sunday 13:00–17:00

Near Field Communication (NFC), Design Techniques and Challenges

Sponsor: **RFIC**

Organizers: **Magnus Wiklund**, *Qualcomm Atheros, USA*
Gernot Hueber, *NXP Semiconductors, Austria*

Abstract: Short-Range Near-Field Communications (NFC) and wireless charging has become a technology on the way to deployment in the high volume market of mobile devices (smartphones, tablets). NFC is used in various applications such as gaming, ticketing, and mobile payments (Google Wallet). Wireless charging is also becoming popular in the quest to remove cables from mobile devices. The interest of the RFIC community is to explore technological challenges and boundaries of what our modern integrated circuit processes have to offer, which architecture and how to design on circuit level. It turns out that RFIC development of NFC circuits is a highly advanced topic. This workshop is to address NFC-forum compliant devices from both, system and circuit design level including testing as well as wireless charging. The format of the workshop is educational. Following up on last years "tradition" we intend to end the workshop with a "hands-on" demo of NFC technology.

Speakers:

1. "Near Field Assisted UWB: TransferJet", **Ichiro Seto**, *Toshiba Corporation, Japan*

2. "WiPower", **Chuck Wheatley**, *Qualcomm, USA*
3. "NFC Fundamentals from a PA Point of View", **Rainer Gaethke**, *Qualcomm Atheros, USA*
4. "Design Techniques for Low Power, Multi-Standard NFC Solutions", **Michael Gebhart**, *NXP Semiconductors, Austria*

WSJ (Half Day): Sunday 08:00–12:00

MEMS in Our World: RF and Analog/Mixed-Signal Circuits and Architectures

Sponsor: **RFIC**

Organizers: **Fred S. Lee**, *Fairchild Semiconductor, USA*
Derek K. Shaeffer, *InvenSense, USA*

Abstract: This workshop covers a variety of MEMS-based systems that have found widespread adoption and growth in our world, as well as nascent MEMS-based technologies that aim to change our lives. There is no doubt that the success of MEMS-based systems rests in the great strides that have been made in MEMs fabrication. However, this workshop will focus on the lesser-known reason for success: empowering collaborations between MEMS and RF/analog/mixed-signal design.

Speakers:
1. "MEMS Timing for the Mobile Era", **Haechang Lee**, *SiTime, USA*
2. "Integrated Micromechanical Circuits for RF Front-Ends", **Clark Nguyen**, *University of California at Berkeley, USA*
3. "MEMS Inertial Sensors for RF Designers", **Derek K. Shaeffer**, *InvenSense, USA*
4. "Optimizing Radio Architectures with MEMS Elements to Enable Reconfigurable Front-Ends and Cognitive/Software-Defined Radio", **Gabriel M. Rebeiz**, *University of California at San Diego, USA*
5. "MEMS-Based Tuning for RF Front-Ends", **Arthur Morris**, *WiSpry, USA*

WSK (Full Day): Sunday 08:00–17:00

Tutorial on Doherty Power Amplifier Circuits and Design Methodologies

Sponsor: **RFIC**

Organizers: **Damon Holmes**, *Freescale Semiconductor, USA*
Jean-Christophe Nanan, *Freescale Semiconductor, France*
Mario Bokatius, *Freescale Semiconductor, China*
Joe Staudinger, *Freescale Semiconductor, USA*

Abstract: The Doherty method has become the power amplifier of choice for cellular infrastructure applications due to its high efficiency at backoff power levels and recent advancements in digital pre-distortion (DPD) techniques that mitigate its non-linear behavior. In this course, the Doherty power amplifier technique will be discussed and analyzed in detail with emphasis on attributes and implementation for high power infrastructure applications. After review of transmitter requirements and driving market forces within the cellular infrastructure market, the material focuses on some of the underlying principles and key fundamentals of the Doherty amplifier. Idealized analysis of symmetric, asymmetric and N-way architectures is given that shows the governing design equations for high efficiency Doherty amplifiers and reveals its advantages beyond cellular infrastructure applications. From this point onward, attention is focused on certain key physical impairments associated with high power Doherty amplifiers which must be considered in practice. Chief amount these are device finite output impedance and degradations resulting from the Peaking sub-amplifier, frequency dispersion, and carrier and peaking sub-amplifier gain and phase inequalities. Each concept is introduced one by one to give the attendee insight into their limitations, and some techniques to compensate their deleterious effects are presented as well. Considerable emphasis is placed throughout the material to identify key challenges faced by those practitioners in this field. Those "real-world" challenges are easily and conveniently demonstrated through the use of large signal device models and loadpull characterization. It is shown how performance can be maximized through input signal splitter, output summing network optimization, and implementing proper phase compensation.

The afternoon portion of the course is a hands-on laboratory exercise where a 500 watt Doherty amplifier is designed and simulated using a CAD tool. The student will import loadpull measurement data into the CAD tool for comparison with device model data. Doherty input and output matching networks will be synthesized by the student with special attention given to tradeoffs between gain, efficiency, power capability and AM/PM distortion. Impairments outlined in the classroom portion of the course will be mitigated by the student to maximize Doherty performance. Final Doherty evaluation will be accomplished using non-linear device models in harmonic balance and circuit envelope simulations. Students are encouraged to take the resulting Doherty CAD project home with them upon completion of the course.

Outline:

1. Market forces, requirements, trends and infrastructure landscape
2. Review of power amplifier concepts
3. Doherty amplifier load modulation
4. High power devices and physical impairments
5. High power Doherty design and realization
6. Simulation laboratory

Instructors:

1. Damon Holmes, Freescale Semiconductor, Tempe, AZ. Damon has extensive experience in the area of RF hardware development, especially Doherty amplifiers, and in optimizing power amplifiers for pre-distortion systems targeting cellular infrastructure.
2. Jean-Christophe Nanan, Freescale Semiconductor, Toulouse, France. Jean-Christophe is a power amplifier architect at Freescale with extensive experience in systems and circuit design.

3. Mario Bokatius, Freescale Semiconductor, Shanghai, China. Mario has over 15 years of experience in designing small signal and high power amplifiers for a variety of wireless applications.
4. Joe Staudinger, Freescale Semiconductor, Tempe, AZ. Joe has 30+ years of experience in the areas of advanced power amplifier systems, transmitter architectures, and large signal device/system modeling for wireless communication systems.

WSL (Half Day): Sunday 08:00–12:00

RFIC VCO Design

Sponsor: **RFIC**

Organizers: **Marc Tiebout**, *Infineon Technologies, Austria*
Domine Leenaerts, *NXP Semiconductors, The Netherlands*

Abstract: VCO performance is critical for numerous RFIC applications including Receivers, Transmitters, Imagers, Radar systems and many more. This educational workshop will refresh the fundamentals of VCO design including an overview of common phase noise theories. State-of-the-art RFIC VCO designs in integrated CMOS and Bipolar/BiCMOS technologies will be covered in detail, not only including a focus on mobile operation, but also on wideband ultra low noise base station requirements. Further contributions will focus on the design for mm-wave operation and ultra low power. In addition, the topic of accurately measuring phase noise will complete the coverage of the VCO design. The topics covered in the workshop include:

1. VCO basics and specifications
2. Phase Noise Theories
3. Topology comparison of cross-coupled, Colpitts, ring-type, etc.
4. Mobile phone VCO design
5. Ultra low phase noise for base stations
6. Harmonic VCO design
7. mm-wave design
8. Ultra low power design
9. Ultra low phase noise design
10. Octave-band tuning
11. Accurate measurements

Speakers:

1. "VCO Basics and Harmonic VCO Design in CMOS", **Andrea Bevilacqua[1], Pietro Andreani[2]**, *[1]University of Padova,Italy, [2]Lund University, Sweden*
2. "VCO-Based Frequency Synthesis in SiGe for mmWave Radar Systems", **Nils Pohl**, *Fraunhofer FHR, Germany*
3. "The Design of Ultra Low Power Oscillators", **Christian Enz**, *CSEM/EPFL, Switzerland*

4. "Ultra Low Noise Octave Band VCO's for Base-Stations", **Ulrich Rohde**, *Synergy Microwave, USA*
5. "VCO Design Workshop Accurate Phase Noise Measurements", **Salam Marougi**, *Agilent Technologies, USA*

WSM (Half Day): Sunday 13:00–17:00

Software Defined Radio Frequency Transmitters

Sponsor: **RFIC**

Organizers: **Sanjay Raman**, *Virginia Tech and DARPA, USA*
Walid Y. Ali-Ahmad, *MediaTek, Singapore*

Abstract: Flexibility and reconfigurability are the new keywords in RF design; many applications require transceivers operating in different modes and bands to fulfill market requirements. Recent research has shown two very different trends. Classical analog-inspired architectures focus on performance numbers that are on par with dedicated radios, while employing circuits and techniques that offer some level of programmability at low cost. Digital-intensive approaches offer flexibility almost for free, and scale well to new technology nodes, but still face RF performance challenges.

This workshop covers the latest research developments in the area of software defined radio transmitters. With the advancement in semiconductor technologies, highly-programmable transmitter architectures leveraging digital and mixed-signal processing have become more prevalent. Some examples include Digital Polar Transmitters (DPT), Radio-Frequency Digital to Analog Converters (RF DAC), high-power digital waveform generation and synthesis (PowerDAC), and switched-capacitor based transmitters.

The invited speakers are prominent researchers in the area of SDR transceiver circuits, and represent both academia and industry at leading organizations in the US and Europe.

Speakers:

1. "Overview of SDR Transmitters, Analog vs. Digital Architectures", **Jan Craninckx[1], Sayfe Kiaei[2]**, *[1]IMEC, Belgium, [2]Arizona State University, USA*
2. "Byting the Digit: RF and mm-Wave 'Digital' Transmitters", **Ali Niknejad**, *University of California at Berkeley, USA*
3. "From Software Radio-Frequency Transmitters to Highly-Reconfigurable mm-Wave Transmitters", **R. Bogdan Staszewski**, *TU Delft, The Netherlands*
4. "Polyphase Upconversion Techniques", **Bram Nauta**, *University of Twente, The Netherlands*
5. "High-Power Efficient RF Digital-to-Analog Converter (HiPERDAC)", **Gerhard Solner**, *Raytheon, USA*

WSN (Full Day): Sunday 08:00–17:00

Signal Generation, Amplification, Detection and System Implementation at THz Frequencies

Sponsors: **RFIC, MTT-4 Terahertz Technology and Applications**

Organizers: **Georg Boeck**, *Berlin Institute of Technology, Germany*
Ullrich Pfeiffer, *University of Wuppertal, Germany*

Abstract: Recently integrated circuits in silicon and III/V-technologies have been pushed towards terahertz frequencies which present both challenges and opportunities for emerging applications and circuits. This workshop presents recent attempts to operate circuits close to and beyond their transistor cut-off frequencies.

Silicon process technologies have reached fmax as high as 0.5 THz, which enables circuits to operate fundamentally up to about 250 GHz with reasonable RF circuit performance. Cut off frequencies of III/V transistors are currently touching the 1 THz border. Beyond fmax, where transistors do not provide power gain, circuits may be operated sub-harmonically to extend further the operation region. Despite their increased receiver NF, such circuits prove to be useful for emerging applications. At terahertz frequencies, on-chip antennas may be implemented with reasonably high efficiencies and very small area, thus eliminating the need for additional external components such as expensive waveguides or horn antennas. Topics covered during the workshop include:

1. THz applications
2. Technology overview
3. Signal generation and detection at THz frequencies
4. III/V, SiGe, CMOS and Schottky diode circuit design at THz frequencies
5. Transceiver and integration technologies, integrated antennas, packaging
6. Circuit characterization methodologies up to and beyond 1 THz
7. Emerging terahertz applications and systems

Speakers:

1. "THz Technologies: Transistors, ICs, Systems", **Mark Rodwell**, *University of California at Santa Barbara, USA*
2. "THz Transceiver Circuits in InP-DHBT Technology", **Herbert Zirath**, *Chalmers University of Technology, Sweden*
3. "mHEMT-Based MMIC Frontends for THz Radar and Communication", **Ingmar Kallfass**, *University of Stuttgart, Germany*
4. "Schottky and MOS Diodes in CMOS for Sub-Millimeter Wave Signal Generation and Detection", **Kenneth K. O**, *University of Texas at Dallas, USA*
5. "Ideas for THz Power Generation and Radiation in Silicon", **Ali Hajimiri**, *Caltech, USA*
6. "Compact 680GHz Wave Imaging Radar Systems", **Adrian Tang**, *NASA Jet Propulsion Laboratory, USA*
7. "THz in CMOS: Challenges and Opportunities", **Ehsan Afshari**, *Cornell University, USA*

8. "THz Sources and Imaging Systems Based on CMOS and SiGe Arrays with High-Efficiency On-Chip Antennas", **Gabriel M. Rebeiz**, *University of California at San Diego, USA*
9. "Towards Single-Chip Silicon Transceivers for Sensors and Radios Above 200GHz", **Sorin Voinigescu**, *University of Toronto, Canada*
10. "Silicon RF Front-Ends for Active THz Imaging Systems", **Ullrich Pfeiffer**, *University of Wuppertal, Germany*

WSO (Full Day): Sunday 08:00–17:00

Holistic Approach to Transceiver Architectures and Technologies to Femto/Pico Cell Based Communication Systems

Sponsor: **MTT-20 Wireless Communication**

SUNDAY SHORT COURSES – 2 JUNE 2013

SC-1: Sunday 08:00–17:00

Compact Modeling and Design of RF Switches

Sponsor: **MTT-1 Computer Aided Design**

SC-2: Sunday 08:00–17:00

Demystifying Device Characterization – An Interactive Course for Transistor Characterization Through Behavioral and Compact Modeling and Load Pull

Sponsor: **MTT-11 Microwave Measurements**

SC-3: Sunday 08:00–17:00

Spectrum Policy Issues for Innovative RF Engineers

Sponsor: **MTT-20 Wireless Communications**

SC-4: Sunday 08:00–17:00

Co-Design of On-Chip Antennas and RF Circuits for System-on-Chip Applications

Sponsors: **RFIC, MTT-6 Microwave and mm-Wave Integrated Circuits**

MONDAY WORKSHOPS — 3 JUNE 2013

WMA (Full Day): Monday 08:00–17:00

Advancements in InAlN/GaN Device and Microwave/MMW Circuit Technology

Sponsors: **MTT-6 Microwave and mm-Wave Integrated Circuits**

WMB (Half Day): Monday 08:00–12:00

How to Start and Grow Your High Tech Company

Sponsor: **MTT-16 Microwave Systems**

WMC (Full Day): Monday 08:00–17:00

The Importance of Low-Frequency Measurements on High-Frequency Characterization

Sponsors: **ARFTG, MTT-11 Microwave Measurements**

WMD (Full Day): Monday 08:00–17:00

Technologies for THz Integrated Systems

Sponsors: **RFIC, MTT-4 Terahertz Technology and Applications**

Organizers: **Mona Hella**, *Rensselaer Polytechnic Institute, USA*
Arun Natarajan, *Oregon State University, USA*

Abstract: Sub-mm-wave and terahertz frequencies have long been attractive for imaging and communication applications. However, technological limitations have impeded the development of commercial systems at such frequencies. THz systems integration is critical for lowering the cost and enabling mass-markets. Several technologies have been proposed and are currently being investigated to address this need. In this workshop, speakers from academia and industry will address the capabilities of state-of-the-art technologies and compare their potential for widespread THz applications. Technologies discussed include CMOS, SiGe, InP, GaAs, GaN and AlGaN.

Speakers will describe sub-mm-wave and terahertz devices, circuits and systems currently being investigated in various technologies to demonstrate their potential, while also discussing future roadmaps. The workshop will be of interest to RFIC and IMS attendees interested in exploring the THz domain for different market sectors (commercial, defense and startups) and seeking to understand the capabilities and limitations of different technologies suitable for such applications.

The workshop will include question and answer sessions after each presentation as well as time at the end of the workshop for the audience to address questions to all the speakers.

Speakers:

1. "Technologies for Terahertz Science", **Goutom Chattopadhyay**, *NASA Jet Propulsion Laboratory, USA*
2. "GaN and 2D Materials: Extreme Materials for Extreme Frequencies", **Tomas Palacios**, *MIT, USA*
3. "GaN HEMTs and Schottky Diodes for Sub-Millimeter-Wave MMICs", **Keisuke Shinohara**, *HRL Laboratories, USA*
4. "AlGaN/GaN Plasmonic Terahertz Detectors", **Michael Shur**, *Rensselaer Polytechnic Institute, USA*
5. "THz Transistors: Present and Future", **Berinder Brar**, *Teledyne, USA*
6. "Transistors for THz Systems", **Mark Rodwell**, *University of California at Santa Barbara, USA*
7. "The Evolution and Future of SiGe Technologies for THz Applications", **John Pekarik**, *IBM, USA*
8. "Silicon THz: An Opportunity for Innovation", **Ali Hajimiri**, *Caltech, USA*
9. "SiGe BiCMOS Technologies for Commercial mmWave Imaging Systems", **Vipul Jain**, *SaberTek, USA*

WME (Full Day): Monday 08:00–17:00

High Speed Signal Integrity Workshop

Sponsor: **ARFTG**

WMF (Half Day): Monday 13:00–17:00

Electro-Nanoporation: An Emerging Biomedical Electromagnetic Application

Sponsor: **MTT-10 Biological Effects and Medical Applications**

MONDAY SHORT COURSES – 3 JUNE 2013

SC-5: Monday 08:00–17:00

Inkjet Printed RF Electronics

Sponsors: **MTT-8 Filters and Passive Components, MTT-17 HF/VHF/UHF Technology, MTT-24 RFID Technologies**

SC-6: Monday 08:00–17:00

Using CAE to Model PLL Noise and Transient Performance

Sponsor: **MTT-22 Signal Generation and Frequency Conversion**

SC-7: Monday 08:00–17:00

Theory and Design of Phase Locked Loops

Sponsor: **MTT-22 Signal Generation and Frequency Conversion**

SC-8: Monday 08:00–17:00

Fundamentals of Device Modeling for Nonlinear Circuit Simulation and Microwave Design

Sponsor: **MTT-11 Microwave Measurements**

FRIDAY WORKSHOPS – 7 JUNE 2013

WFA: Friday 08:00–17:00

Multi-Octave High Efficiency, High Linearity High Power

Sponsor: **MTT-5 Microwave High-Power Techniques**

WFB: Friday 08:00–17:00

SSPAs vs. Vacuum Tube Amplifiers: An Update

Sponsor: **MTT-5 Microwave High-Power Techniques**

WFC: Friday 08:00–17:00

Microwave Sensors and Biochips for Biomolecules and Cells Characterization

Sponsor: **MTT-10 Biological Effects and Medical Applications**

WFE: Friday 08:00–17:00

RFICs/MMICs and Their Professional Wireless Sensing Applications

Sponsor: **MTT-20 Wireless Communication**

WFF: Friday 08:00–17:00

Recent Advances on RF/Microwave Multi-Function Filtering Devices

Sponsor: **MTT-8 Filters and Passive Components**

WFH: Friday 08:00–17:00

Designing High-Efficiency Microwave Switch-Mode Amplifiers Beyond 2GHz

Sponsor: **MTT-6 Microwave and mm-Wave Integrated Circuits**

WFI: Friday 08:00–17:00

RF-on-Demand for the Internet of Things

Sponsors: **MTT-26 Wireless Energy Transfer and Conversion, MTT-24 RFID Technologies, MTT-25 RF Nanotechnology**

WFJ: Friday 08:00–17:00

Microwave Systems for Security Applications

Sponsor: **MTT-16 Microwave Systems**

WFK: Friday 08:00–17:00

Satcom and Aerospace Beyond Ka-Band: Progress and Challenges

Sponsor: **MTT-20 Wireless Communication**

WFL: Friday 13:00–17:00

Magnetoelectrics: An Emerging Technology for a New Class of RF and Microwave Control Components

Sponsor: **MTT-13 Microwave Ferrites and Ferroelectrics**

FRIDAY SHORT COURSES – 7 JUNE 2013

SC-9: Friday 08:00–17:00

The Dynamics, Bifurcation, and Practical Stability Analysis/Design of Nonlinear Microwave Circuits and Networks

Sponsor: **MTT-16 Microwave Systems**

SC-10: Friday 08:00–17:00

Procedures and Techniques for Characterizing High-Power Devices Using Vector Network Analyzers

Sponsor: **MTT-5 Microwave High-Power Techniques**

SC-11: Friday 08:00–17:00

Sub-picosecond Jitter Fractional Frequency Synthesizer Design

Sponsor: **MTT-22 Signal Generation and Frequency Conversion**

SC-12: Friday 08:00–17:00

Graphene RF Electronics: Modeling and Applications

Sponsor: **MTT-25 RF Nanotechnology**

ADVANCE REGISTRATION

Registration Categories

The Registration process is split into three tiers in order to better serve membership needs. The 1st tier is the Early Bird Registration period. It begins Monday, 4 February and will last through Monday, 6 May. This period provides an opportunity to register for the Symposium at the lowest possible cost. Immediately following the Early Bird period is the 2nd tier or Advance Registration period. It extends from Tuesday, 7 May through Friday, 31 May, just prior to the start of Microwave Week. The 3rd and final tier is the On-site Registration period that will remain the same as in past Symposia, starting on Saturday, 1 June, the first day of Microwave Week, and ending on Friday, 7 June.

EARLY BIRD PERIOD 4 February–6 May (Through Midnight EDT)
ADVANCE PERIOD 7 May–31 May (Through Midnight EDT)
ON-SITE PERIOD 1 June–7 June (Throughout Microwave Week)

Register online: https://reg.mpassociates.com/reglive/PromoCode.aspx?confid=148

Please note: Registration is required for all attendees including SESSION CHAIRS and PRESENTERS. Only paid attendees will be admitted to the breakfasts, workshops, technical sessions, and exhibit hall.

Membership

Check the boxes of all organizations of which you are a member. To receive IEEE member rates, enter your member number and present your IEEE card upon check in at the conference. Registrants who do not have a current IEEE membership card at check in will be charged non-member rates. If you are not a member and would like to learn about the advantages of being a member and receiving the conference member rate, please visit www.ieee.org/services/join or call 1-800-678-IEEE. Please note that you must be a member at the time of registration to receive the member rate.

Symposium SUPERPASS

For one low price, registrants can attend as many technical sessions from any of the three contributing organizations, IMS, RFIC, and ARFTG, as well as attend one full-day workshop (or two half-day workshops, if desired). ***SUPERPASS*** registration includes the electronic proceedings for IMS, RFIC, ARFTG, and the All Workshop electronic proceedings. Also included is admission to the exhibits. In addition, the ***SUPERPASS*** will allow you to attend the IMS Welcome Reception on Monday, the Awards Banquet on Wednesday and the Thursday closing ceremonies.

Symposia

Microwave Week includes the IMS Technical program, and Exhibition, as well as the RFIC Symposium, and ARFTG Conference.

Select the conference(s) you wish to attend. Students, Retiree's, and IEEE Life Members receive a discount on some registration fees. To qualify as a student, a registrant must be either an IEEE Student Member or a full time student carrying a course load of at least nine credit hours. To qualify as an IEEE Life member please reference the IEEE Life Member site for qualifications.

- IMS Technical Sessions are held on Tuesdays, Wednesday, and Thursday. Registration includes admission to the Exhibition and Electronic Proceedings.
- RFIC Technical Sessions are held on Monday and Tuesday. Registration includes admission to the RFIC Reception, the Exhibition, and the Electronic Proceedings.

- ARFTG Technical Sessions are held on Friday. Registration includes breakfast, lunch, Electronic Proceedings, and admission the ARFTG Exhibition. ARFTG Conference member rates are available to both ARFTG and IEEE Members.
- Microwave Week hosts the largest exhibition of its kind with over 400 companies. Exhibit only registration is available.

Guest Registration

Attendees registered for the technical portion of the conference may add a guest to their registration for an additional fee. Guest registration includes access to the hospitality suite, plenary session, and exhibit hall, but does not allow access to technical sessions and workshops.

Exhibit Only Registration

Access to the Exhibition Hall Tuesday through Thursday.

Free Wednesday!

Wednesday exhibit only registration is free. This includes the Industry Hosted Reception in the exhibit hall 17:00 to 18:00.

Workshops

The workshop fee includes electronic proceedings for all the workshops being presented on that particular day. For Early Bird registration **ONLY**, the workshop's printed notes are also included for the workshop you are registered for with the workshop's fee. For Advanced and On-site registration, the workshop's printed notes are **NOT** included in the workshop's fee and must be purchased separately.

Full-day workshops include a continental breakfast, a morning refreshment break, a lunch, and an afternoon refreshment break. Morning workshops include a continental breakfast, and a morning refreshment break. Afternoon workshops include a lunch and an afternoon refreshment break.

All-Workshop Electronic Proceedings

Purchase two full-day workshops and receive the electronic proceedings for all three days of workshops (Sunday, Monday, and Friday). The All-Workshop electronic proceedings are not available for individual sale.

Awards Banquet

The MTT Awards Banquet will be held on Wednesday, 5 June from 1830 to 2200 at the Washington State Convention Center. The evening will include fine dining, an awards presentation, and excellent entertainment. Major society awards will be presented.

Boxed Lunches

Optional boxed lunches are available for purchase by all attendees but are especially convenient for those attending the panel sessions or exhibit hall during lunchtime. It is encouraged to purchase boxed lunches before Microwave Week, as orders will not be available on-site. Refunds for lunches will not be available since these are ordered in advance.

Extra Electronic Proceedings and Digests

Additional Electronic Proceedings (IMS, RFIC, and ARFTG) and digests (RFIC only) are available for purchase and pick-up at the conference. After the Symposium, these digests and Electronic Proceedings will be available for purchase from IEEE.

Payment

Individual payment must accompany the registration form and is payable in U.S. dollars only, using a personal check drawn on US bank or credit card (VISA, MasterCard, or American Express) or bank wire transfer. Personal checks must be encoded at the bottom with the bank account number and check number. Bank drafts, cash, international money order and purchase orders are UNACCEPTABLE and will be returned. Please make checks payable to "2013 IEEE IMS". Written requests for refunds will be honored if received by 6 May 2013. Refer to the Refund Policy for complete details.

Refund Policy

Written requests received by 6 May 2013 will be honored. Refund requests postmarked after this date and those for on-site registration will be processed only if an event is cancelled. This policy applies to the registration for the symposium sessions, workshops, digests, extra electronic proceedings, awards banquet and boxed lunches. Please state the pre-registrants name and provide an email address. If registration was paid for by credit card, the refund will be made through an account credit. Address your requests to:

MTT-S Registration
Nannette Jordan
MP Associates
1721 Boxelder St., Ste. 107
Louisville, CO 80027, USA

nannette@mpassociates.com

ON-SITE REGISTRATION

On-site registration for all Microwave Week events will be available in the South Lobby of the Washington State Convention Center.

Registration Hours

Date	Time
Saturday, 1 June	14:00–18:00
Sunday, 2 June	07:00–19:00
Monday, 3 June	07:00–19:00
Tuesday, 4 June	07:00–18:00
Wednesday, 5 June	07:00–18:00
Thursday, 6 June	07:00–16:00
Friday, 7 June	07:00–09:00

Exhibit Only Registration

Access to the Exhibition Hall Tuesday through Thursday.

Press Registration

Credentialed press representatives are welcome to register without cost, receiving access to IMS technical sessions and exhibits. Digests are not included. The Press Lounge will available from Sunday through Thursday of Microwave Week.

ARFTG Registration

Late on-site registration will be available in the South Lobby of the Washington State Convention Center on Friday from 07:00 to 09:00. If at all possible, please pre-register earlier in the week to reduce the on-site workload.

Registration Rates in USD for IEEE or ARFTG Members and Non-Members	Early Bird (4 Feb–6 May)		Advance (7–31 May)		On-site (1–7 June)	
	Member	Non-Member	Member	Non-Member	Member	Non-Member
Superpass						
IMS, RFIC, and ARFTG Sessions and their Electronic Proceedings, the All Workshop electronic proceedings and attendance to a Full Day (or 2 Half Day) Workshop, Award Banquet Wednesday, 5 June	$995	$1495	$1155	$1730	$1345	$2000
Student, Retiree, Life Member SuperPass	$595		$695		$840	
IMS						
IMS Sessions	$425	$635	$495	$740	$575	$850
Single Day Registration	$215	$320	$250	$370	$290	$435
Student, Retiree, Life Member IMS Sessions	$75	$140	$85	$150	$100	$165
RFIC Symposium						
RFIC Sessions	$230	$330	$260	$380	$280	$415
Student, Retiree, Life Member RFIC Sessions	$160		$180		$200	
ARFTG Conference						
ARFTG Sessions	$220	$330	$255	$385	$290	$435
Student, Retiree, Life Member ARFTG Sessions	$150		$175		$195	
Colocated Seminar						
Wireless Industry Day — Wednesday Only	$165	$245	$180	$265	$225	$335
Wireless Industry Day — Wednesday Only for Student, Retiree, Life Member ARFTG Sessions	$125		$135		$155	
Exhibit Only						
Exhibition Only Pass	$25	$25	$25	$25	$30	$30
Wednesday Exhibition Only Pass	FREE	FREE	FREE	FREE	FREE	FREE
Guest Registration						
Guest Badge	$40	$40	$40	$40	$40	$40

Registration Rates – Workshops and Short Courses

Rates in USD	Early Bird (4 Feb–6 May)			Advance (7–31 May)			On-site (1–4 June)		
	IEEE (or ARFTG) Member	Non-Member	Student, Retiree, Life Member	IEEE (or ARFTG) Member	Non-Member	Student, Retiree, Life Member	IEEE (or ARFTG) Member	Non-Member	Student, Retiree, Life Member
Workshops									
2 Full Day Workshops*	$435	$645	$325	$475	$700	$355	$595	$880	$405
Full Day	$165	$245	$125	$180	$265	$135	$225	$335	$155
Half Day	$85	$125	$65	$95	$140	$70	$115	$170	$80
Printed Workshop Notes	INCLUDED	INCLUDED	INCLUDED	$20	$30	$20	$30	$45	$30
Short Courses									
Full Day Short Course	$285	$425	$200	$335	$500	$235	$390	$585	$270

*includes access to two full day workshops and the electronic proceedings for all three days of workshops (all the workshop proceedings)

Registration Rates – Additional Items

Rates in USD	Early Bird (4 Feb–6 May)		Advance (7–31 May)		On-site (1–7 June)	
	IEEE (or ARFTG) Member	Non-Member	IEEE (or ARFTG) Member	Non-Member	IEEE (or ARFTG) Member	Non-Member
Extra Proceedings and Digests						
IMS Electronic Proceedings	$50	$75	$60	$90	$70	$105
RFIC Digest	$50	$75	$60	$90	$70	$105
RFIC Electronic Proceedings	$50	$75	$60	$90	$70	$105
ARFTG Electronic Proceedings	$50	$75	$60	$90	$70	$105
Wireless Industry Day Proceedings	$50	$75	$60	$90	$70	$105
Events						
RFIC Reception (Sunday Night)	$30	$50	$40	$60	$50	$70
Awards Banquet (Wednesday Night)	$55	$55	$65	$65	$75	$75
Thursday Night Event	$55	$55	$55	$55	$55	$55
Lunch						
Boxed Lunches	$25	$25	$25	$25	N/A	N/A

VISA INFORMATION

United States Visa Advisory

The United States has updated its visa policy for increased security. As a result, it now takes longer to obtain a visa. Advanced planning by travelers is essential to avoid frustration and disappointment.

- Review your visa status to find out if you need a U.S. visa or a visa renewal.
- Plan to submit your visa application well in advance of your intended departure date.
- Contact your nearest U.S. embassy or consulate for current time estimates and recommendations.
- Visit the embassy or consular section website to find important information on how to schedule an interview appointment, finger scanning – if required - and pay fees. An interview is required as a standard part of processing for most visa applicants.

Visa Waiver Program (VWP)

The Visa Waiver Program (VWP) enables nationals of 36 participating countries to travel to the United States for tourism or business (visitor [B] visa purposes only) for stays of 90 days or less without obtaining a visa. The program was established to eliminate unnecessary barriers to travel, stimulating the tourism industry, and permitting the Department of State to focus consular resources in other areas. VWP eligible travelers may apply for a visa, if they prefer to do so. Nationals of VWP countries must meet eligibility requirements to travel without a visa on VWP, and therefore, some travelers from VWP countries are not eligible to use the program. VWP travelers are required to have a valid authorization through the Electronic System for Travel Authorization (ESTA) prior to travel, are screened at the port of entry into the United States, and are enrolled in the Department of Homeland Security's US-VISIT program.

Currently, 36 countries participate in the Visa Waiver Program, as shown below:

Andorra	Hungary	New Zealand
Australia	Iceland	Norway
Austria	Ireland	Portugal
Belgium	Italy	San Marino
Brunei	Japan	Singapore
Czech Republic	Latvia	Slovakia
Denmark	Liechtenstein	Slovenia
Estonia	Lithuania	South Korea
Finland	Luxembourg	Spain
France	Malta	Sweden
Germany	Monaco	Switzerland
Greece	The Netherlands	United Kingdom

For more information, see http://travel.state.gov/visa/temp/without/without_1990.html

VISA INFORMATION (continued)

Passports

A passport with a validity date of at least six months beyond the applicant's intended period of stay in the U.S. is required. If more than one person is included in the passport, each person desiring a visa must make a separate application. Please check with the website, https:/www.cbp.gov, to confirm that your passport is compliant. Temporary Passports will likely merit special scrutiny. To avoid complications, check with your local US consular offices, well ahead of your intended departure dates.

Visa Letters

A visa support letter can be provided for authors and registered attendees upon request. Please submit your requests for letters of support well in advance of your interview dates to allow sufficient time for processing. Spouses and guests requiring visa assistance must be registered for an IMS Guest Program Event (information found on the conference website).

Please submit your requests for letters of support well in advance of your interview dates to allow sufficient time for processing.

For additional visa assistance, please contact Dr. Zaher Bardai at zb@ieee.org.

Disclaimer

This information is provided in good faith but travel regulations do change. The only authoritative sources of information are the U.S. Government websites at www.unitedstatesvisas.gov and http://travel.state.gov/visa/visa_1750.html.

SOCIAL EVENTS/GUEST PROGRAM

SUNDAY, 2 JUNE 2013

RFIC Reception: 19:30–21:30
Washington State Convention Center, Ballroom 6E

Immediately following the RFIC Plenary Session is the RFIC Reception to be held in adjacent Room 6E at the Washington State Convention Center (WSSC). This social event is a key component of the RFIC Symposium, providing an opportunity to connect with old friends, make new acquaintances, and catch up on the wireless industry. Admittance is included with RFIC Symposium registration. Additional tickets can also be purchased separately at registration.

MONDAY, 3 JUNE 2013

IMS2013 Welcome Reception: 19:00–20:00
Sheraton Seattle Hotel

All Microwave Week attendees and exhibitors are invited to attend a reception hosted by IMS2013 in the Sheraton Seattle Hotel, Grand Ballroom, 2nd Floor.

Chapter Chairs' Meeting (CCM): 20:00–22:00
Sheraton Hotel, 3rd Floor, Metropolitan Room

All our Chapter Chairs and their designated Chapter representatives are cordially invited to our Reception/Poster Session followed by the Chapter Chair's Meeting. For further information contact your Regional Chapter Coordinator, or Bela Szendrenyi at bela.szendrenyi@advantest.com.

Sponsor: IEEE MTT-S AdCom and the MGA Committee

TUESDAY, 4 JUNE 2013

Women in Microwaves Reception: 18:00–19:30
Seattle Space Needle, 100-Level

Meet with old friends as well as make new connections to the growing community of women who make a career in the field of high-technology. Enjoy great food, refreshing beverages and warm conversation at the WIM Social Event.

Ham Radio Social: 18:00–19:30
Seattle Space Needle, 100-Level

While enjoying a buffet and open bar, the attendees will have the opportunity to see the accomplishments of amateur radio operators who have skillfully designed and built transceivers for use from VHF to high millimeter wave bands. Some of these transceivers were made from surplus and commercially available components and some are state-of-the-art new designs including SDR. Several will be on display and their builders will be there to answer questions.

All conference attendees are welcome. You will find that amateur radio operators are utilizing their allocated frequency spectrum for very important uses and you may be interested in obtaining your license so you too can test your new designs and microwave propagation.

MTT-S Graduates of the Last Decade (GOLD) and Student Reception: 19:30–21:30
Experience Music Project (EMP) @ Seattle Center

The IEEE MTT Graduates of Last Decade (GOLD) and Student Committees invite all MTT GOLD and student members to a complimentary reception at the Experience Music Project located at Seattle Center. This will be an excellent opportunity not only to relax and entertain, but also to interact and network with other GOLD and student members.

Sponsor: IEEE MTT-S GOLD and Student Committees

WEDNESDAY, 5 JUNE 2013

Industry Hosted Cocktail Reception: 17:00–18:00
Washington State Convention Center, Level 4 — Exhibition Hall

Symposium Exhibitors will host a cocktail reception.

MTT-S Awards Banquet: 19:00–22:00
Sheraton Seattle Hotel, Grand Ballroom C&D

The MTT-S Awards Banquet includes dinner, major society awards presentation and entertainment. Tickets can be purchased at the time of registration. Entertainment will also be provided by Tom Raschko (IMS2013 General Chair) and The Jet City Band.

THURSDAY, 6 JUNE 2013

MTT-S Student Awards Luncheon: 12:00–14:00
Sheraton Seattle Hotel, Grand Ballroom C

All students are invited to attend the luncheon which recognizes recipients of the MTT-S Undergraduate Scholarships, MTT-S Graduate Fellowships, MTT-S PhD Student Initiative Program, IMS2013 Student Volunteers, IMS2013 Student Paper Awards and the participants/winners of the IMS2013 Student Design Competitions.

IMS2013 Closing Reception: 17:30–18:30
Washington State Convention Center, Ballroom 6A

All Microwave Week attendees and exhibitors are invited to attend the Closing Reception hosted by IMS2013 in the Washington State Convention Center in Ballroom 6A.

SUNDAY, 2 JUNE – THURSDAY, 6 JUNE, 07:00–16:30
and FRIDAY, 7 JUNE, 07:00–12:00

Guest Lounge

The Guest Lounge will be located at the Sheraton Hotel on the Lobby Level in the Diamond Room. It will be a place to relax and meet. The Guest Lounge will also have suggestions and discount coupons for various activities to enjoy while in Seattle as well as fun games and crafts for the families. Guest registration is required and fees do apply.

IMS2013 COMPANION TOURS

Attendees should meet at the Sheraton Hotel lobby-level hospitality suite at the starting times shown below.

MONDAY, 3 JUNE 2013

Premier 3-Hour City Tour ($49)
09:45–13:00

This Premier 3-hour City Tour is designed to give you a fantastic overview of Seattle. Sit back and relax in the spacious Tours Northwest coach as our knowledgeable and friendly guide acquaints us with some of Seattle's most interesting neighborhoods and attractions. Sights are numerous and include Pike Place Market, the Seattle waterfront, CenturyLink Field and Safeco Field stadiums, Mercer Island via the floating bridge, the International District, the Fremont neighborhood with its famous Troll, and Seattle's not-to-be-missed landmark Space Needle. Along this 50-mile tour we'll make a stop at historic Pioneer Square, which marks Seattle's original downtown, and also at the Ballard Locks, which provide a passage for boats going between the salt water of the Puget Sound and the fresh water of the Ship Canal. You can also enjoy the underwater viewing at the adjoining salmon ladders. Near the end of our tour we'll have a great city skyline photo opportunity.

TUESDAY, 4 JUNE 2013

Savor Seattle Pike Place Market Tasting Tour ($45)
First tour — 08:45–11:30
Second tour — 09:15–12:00

Become a Pike Place Market insider on our 2-hour, behind-the-scenes adventure. Experience the sights, sounds, and flavors of this 105-year-old landmark while seeing fish fly, cheese being made, and visiting the original Starbucks. Bring your appetite because we'll be treated to at least sixteen tasty samples including crab cakes, chowder, and cheese. We'll be given an insider's look at ten of the Market vendors and hear entertaining stories of the Market's rich history and culture. After our guided tour, you may want to extend your visit and shop among the many craft vendors selling locally-made jewelry, clothing, and gifts.

TUESDAY, 4 JUNE 2013

Fairmont High Tea ($55)
12:30–15:00

Enjoy a traditional Afternoon High Tea at the historic Fairmont Olympic Hotel. In addition to a fine selection of teas, you will enjoy tea sandwiches, savories, and house-made scones. It will be a relaxing afternoon as we luxuriate in the beautiful setting of the Georgian restaurant's high ceilings, Palladian windows, and spectacular chandeliers.

WEDNESDAY, 5 JUNE 2013

Space Needle and Chihuly Garden and Glass ($40)
10:00–15:00

On today's outing we'll be whisked through downtown Seattle via monorail to Seattle Center, home of the iconic space Needle, built for the 1962 World's Fair. We'll ride the elevator up to the observation deck and take in 360 degrees of awesome views of the city and Puget Sound. Lunch will be on our own at a choice of onsite restaurants. Then we'll tour the Chihuly Glass and Garden, opened just last year, where we'll learn why Seattle is so renowned for its art glass. And, we'll have ample time for the gift shops before our return trip by monorail to downtown Seattle.

THURSDAY, 6 JUNE 2013

Snoqualmie Falls and Wine Tasting Tour ($92)
includes: Tours Northwest coach, lunch, and wine tastings
09:15–15:30

Today's tour begins with a drive to one of Washington's most popular scenic attractions, Snoqualmie Falls. From the observation deck we'll be able to view the spectacular falls cascading through a rocky gorge to a pool 270 feet below. While there, we'll also enjoy a peek in at the Salish Lodge & Spa, a quintessential Pacific Northwest retreat. Then it's on to lunch at Purple Café in Woodinville, a restaurant that combines classic American styles with seasonal Northwest ingredients. After lunch we'll tour Chateau Ste. Michelle, Washington's oldest and most acclaimed winery, gracefully situated in beautiful park-like grounds. Your wine knowledge will be enhanced as you learn about their heritage, get an exclusive glimpse at winemaking, and pause to sample their wines. And, you'll love perusing their lovely gift shop. We'll end our day with a contrasting experience by making a visit to the contemporary Novelty Hill + Januik Winery. Here, two independent wineries share a tasting room and the talents of Mike Januik, their acclaimed winemaker. Note: This tour is for those aged 21 and older.

FRIDAY, 7 JUNE 2013

Mount Rainier Tour ($98)
07:00–18:00

Be sure to bring your camera with you on your full-day Tours Northwest outing to the breathtakingly-beautiful Mount Rainier National Park. You will delight in its vast expanses of pristine old-growth evergreen forests, magnificent rivers, mountain lakes, waterfalls, and wildlife. Mount Rainier, which ascends to 14,411 feet above sea level, stands as an icon in the Washington

landscape. You'll appreciate the beauty of this stunning mountain up close, and you'll be able to see the glaciers radiating from its summit. There is an informative Visitor Center with panoramic views and a movie presentation on the park and its history. Snack and gift shops can be found at the Visitor Center and the beautiful Paradise Inn. Comfortable walking shoes and layered clothing are advised. Lunch is on your own.

TUESDAY, 4 JUNE 2013 ($59) & THURSDAY, 6 JUNE 2013 ($59)

The Future of Flight Aviation Center and Boeing Tour
07:45–12:00

The Future of Flight Aviation Center and Boeing Tour offers the only opportunity to tour a commercial jet assembly plant in North America. We'll travel by Tours Northwest coach to the Future of Flight Aviation Center located in Mukilteo, Washington, 25 miles north of Seattle. You'll be able to explore the interactive exhibits and displays and will even have the opportunity to design and virtually test your own jet. Then, after a short video presentation, we'll go behind the scenes at nearby Boeing's Everett, Washington facility for a fascinating 90-minute tour of the world's largest building by volume (472,000,000 cubic feet). Home to the 747, 767, 777, and 787 Dreamliner production lines, you'll see airplanes in various stages of construction being built for their worldwide base of airline customers. And, who knows? You might be flying on one of these very planes some day!

IMPORTANT: Please note all restrictions on Boeing website before signing up (http://www.boeing.com/commercial/tours/index.html)

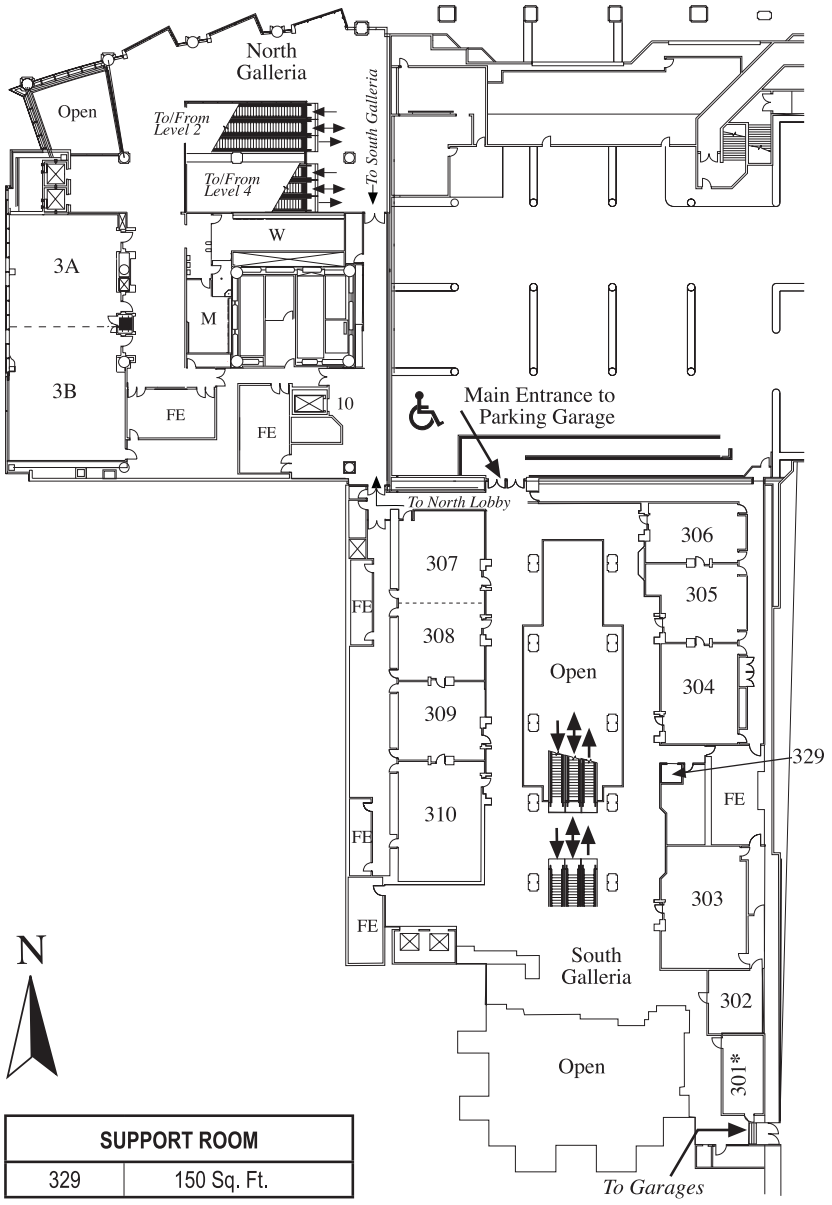
THURSDAY, 6 JUNE 2013

Thursday Night Event ($55)
Seattle's Premier Native Cultural Experience and
Home of the Famous Salmon Bake at Tillicum Village
18:00–22:30 (departs from Pier 55)

Begin your 4-hour escape with a narrated cruise from downtown Seattle, Pier 55 to Blake Island State Park. Upon arrival to Tillicum Village, you are greeted with steamed clams in nectar. Make your way into the longhouse and watch as whole salmon are cooked in a traditional Northwest Coast Indian style. Enjoy a fabulous salmon buffet meal followed by a show that highlights the Coast Salish tribes through storytelling and symbolism. Afterward, you'll have free time to explore the grounds and gift shop before returning to Seattle.

CONVENTION CENTER MAPS

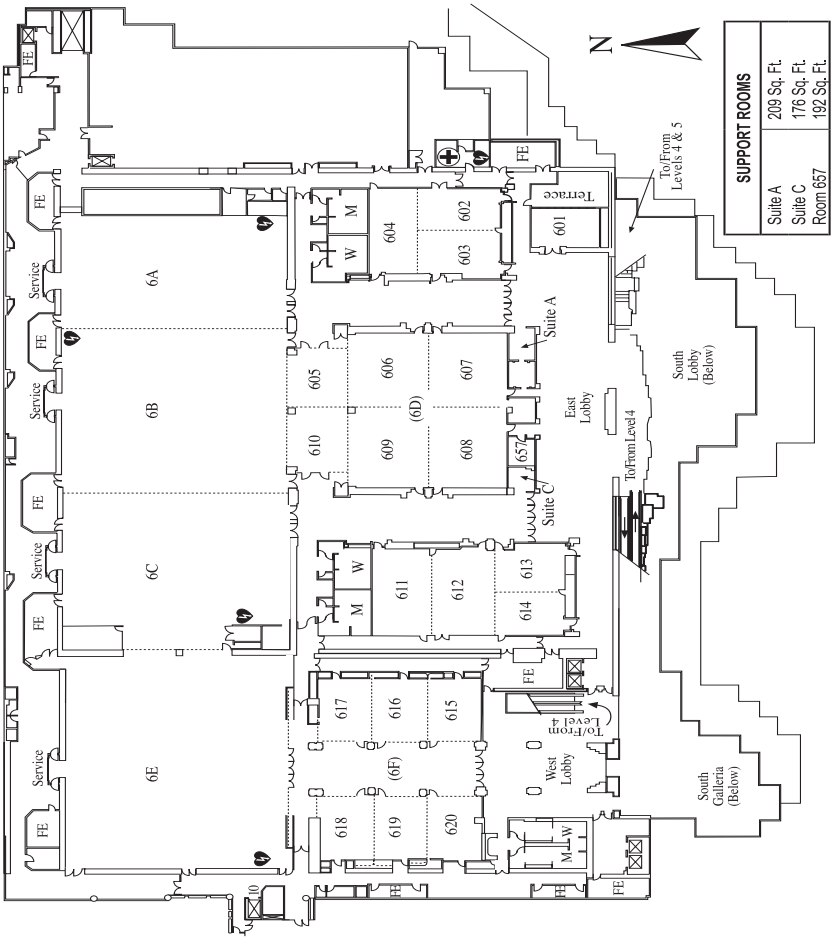
Level Three: Meeting Rooms



SUPPORT ROOM	
329	150 Sq. Ft.

CONVENTION CENTER MAPS (continued)

Level Six: Ballrooms & Meeting Rooms



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2013 RFIC Symposium
Seattle, Washington, USA
2–4 June 2013

PROGRAM