RFIC 2013

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Co-Chair: Lawrence Kushner, BAE Systems, and Bertan Bakkaloglu, Arizona State University

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Chair: Gernot Hueber, NXP Semiconductors — Co-Chair: Pedram Mohseni, Case Western Reserve University

Room 618-620, Time 08:00 - 09:40, Monday, 3 June 2013

RMO1C: Phase Noise Reduction Techniques

Chair: Timothy M. Hancock, MIT Lincoln Laboratory — Co-Chair: Kamran Entesari, Texas A&M University

Room 611-612, Time 08:00 - 09:40, Monday, 3 June 2013

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Chair: Francis Rotella, Peregrine Semiconductor — Co-Chair: Harish Krishnaswamy, Columbia University

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RMO2A: Low-Power Transceivers for Wireless Applications

Chair: Li-Wu Yang, Shanghai Jiao Tong University — Co-Chair: Jenshan Lin, University of Florida

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RMO2B : RF & mm-Wave Front-End Techniques

Chair: Osama Shana'a, MediaTek — Co-Chair: Marc Tiebout, Infineon Technologies

Room 615-617, Time 10:10 – 11:50, Monday, 3 June 2013

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- A High-Resolution Short-Range CMOS Impulse Radar for Human Walk Tracking

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Technische Universiteit Eindhoven, *The Netherlands*

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University of Michigan, *USA*

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University of Minnesota, *USA*

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- A 0.32nJ/bit Noncoherent UWB Impulse Radio Transceiver with Baseband Synchronization and a Fully Digital Transmitter

University of Southern California, *USA*

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Wireless Spectrum Challenges & Opportunities: Maximizing Assets for Growth

AUTHOR:
Neville Ray, *T-Mobile, USA*

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ABSTRACT:
In an industry needing to support phenomenal growth, spectrum is key. Networks and devices must support multiple technologies and frequency bands without sacrificing performance. The industry has to come together to provide innovative and cost-effective RFIC design that utilizes all available resources.

Smarter utilization of industry assets is essential, for example building small cell solutions (HetNets) that include tighter integration and interworking between cellular and WiFi. Since unlicensed spectrum is a great augment to carriers' licensed spectrum assets, it opens a myriad of opportunities for increasing network capacity. Better integration between WiFi and cellular would allow customers greater capacity and flexibility with data transmissions based on cost or desired quality level and network load. Therefore, RFIC innovation is necessary for future wireless systems.

Microwave Technologies: The First Century

AUTHOR:
Barrie Gilbert, *Analog Devices Inc., USA*

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ABSTRACT:
The talk describes the history of microwave technologies, reaching back to the late 1800s, a time of experimentation with spark-gaps and waveguides up to 60GHz. Marconi and Hertz also investigated this regime, but turned their attention to low frequencies. For decades crude galena rectifiers were used for detectors, setting the stage for the later development of semiconductor diodes. The triode tube was a great leap for radio, but not as a source of microwave power, due to its long transit times. The 1920 Barkhausen-Kurz oscillator made use of this transit time to generate frequencies up to 700MHz.

Once the idea of exploiting transit times was out of the box, the majority of microwave power sources for the next several decades were based on such methods and some invoked the use of crossed magnetic and electric fields. The cavity magnetron, today found in every home, was invented in 1937 by Boot and Randall at Birmingham University in England. It possessed the astonishing ability to instantly convert simple DC power into RF power in the centimetre range of wavelengths with hitherto unimaginable efficiency. It was followed by a rash of amazing electron tubes with mysterious names: the klystron, twystron, dematron, amplitron, and the scary-sounding carcinotron. Later semiconductor devices would generate their own list of odd abbreviated names: BARRIT, TED, IMPATT, TRAPATT and LSA.

The commercialization of radio communication systems has led to a greater emphasis on two imperatives: very high performance, and extremely low cost. Modern microwave technologies have moved into a new commodity phase, like plastics or steel. However, it is safe to say "You ain't seen nuthin' yet!"

A High-Resolution Short-Range CMOS Impulse Radar for Human Walk Tracking

AUTHORS:
Piljae Park, Sungdo Kim, Sungchul Woo, Cheonsoo Kim, *ETRI, Korea*

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ABSTRACT:
A single-chip impulse radar transceiver is presented. A high-resolution, enhanced SNR and controllability are achieved with a proposed architecture. By controlling timing between the transmit (TX) pulse and sampling clock of the receiver, echo pulses from targets are received and recovered. The TX pulse can adjust its spectrum occupancy by changing impulse shape. The 4-channel sampling receiver consists of a low noise amplifier, track and hold samplers, integrators, and a cascaded triple delay locked loop. The embedded control logic allows the radar to enhance the SNR of the received pulse using an averaging technique, and to operate at multiple reception modes.

The real-time radar system measurements show that echo pulses are recovered with ≥100-psec range resolution while consuming 80 mW from 1.2-V of V_{dd}. An indoor human walking trace is successfully recorded. The transceiver is fabricated in a 130-nm CMOS technology occupying chip area of 3.4 mm^2.

An All-Digital IR-UWB Transmitter with a Waveform-Synthesis Pulse Generator in 90nm CMOS for High-Density Brain Monitoring

AUTHORS:
Ali Ebrazeh, Pedram Mohseni, *Case Western Reserve University, USA*

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ABSTRACT:
This paper reports an all-digital impulse radio ultra wideband transmitter (IR-UWB TX) fabricated in 90-nm CMOS, which incorporates a waveform-synthesis pulse generator and a timing generator for OOK/PPM pulse modulation and scrambling. The UWB pulse generator includes ten identical taps, each comprising an impulse generator and an output driver. Upon triggering by the timing generator, these taps create a programmable number of individual lobes with 4b control over their duration and amplitude, which are then combined at a shared output node to generate the UWB pulse. With a high-performance receiver, the TX might be used for moderate-data-rate (<50Mbps), m-range telemetry, suitable for brain-behavior studies, with energy consumption in the range of 12 to 20pJ/pulse, and for high-data-rate (>100Mbps), cm-range telemetry, suitable for brain-machine interfaces, with energy consumption in the range of 3.6 to 6pJ/pulse from 1.2V.

A 0.32nJ/bit Noncoherent UWB Impulse Radio Transceiver with Baseband Synchronization and a Fully Digital Transmitter

AUTHORS:
Ashutosh Mehra [1], Martin Sturm [1], Dan Hedin [2], Ramesh Harjani [1]
[1] *University of Minnesota, USA* ; [2] *Advanced Medical Electronics, USA*

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ABSTRACT:
This paper presents a low-power noncoherent ultrawideband (UWB) impulse-radio (IR) transceiver operating at 5GHz in 0.13-μm CMOS. The super-regenerative amplifier (SRA) based energy-detection receiver utilizes early/late detection for a two-step baseband synchronization algorithm. A fully-digital transmitter generates a shaped output pulse of 1GHz 3-dB bandwidth. DLLs provide a PVT-tolerant time-step resolution of 1ns over the entire symbol period and regulate the pulse generator center frequency. Measured results show a receiver efficiency of 0.32nJ/bit at 20.8Mb/s and operation with inputs as low as -70dBm. The transmitter outputs -31dBm (0.88pJ/pulse at 1Mpulse/s) with a dynamic (energy) efficiency of 16pJ/pulse.

A 0.7V Intermittently Operating LNA with Optimal On-Time Controller for Pulse-Based Inductive-Coupling Transceiver

AUTHORS:
Teruo Jyo, Tadahiro Kuroda, Hiroki Ishikuro, *Keio University, Japan*

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ABSTRACT:
This paper presents a low-power LNA for a inductive-coupling transceiver. Intermittently operating technique to turn on LNA only at the moment when the pulse signal appears is used to reduce power consumption. To optimally control the On-time of LNA, pulse width detector based on self-oversampling TDC is used and compensate the PVT variations of On-time width and of pulse signal width. The fabricated test chip in 65nm CMOS occupies 0.06mm^2 and achieved the intermittently operating frequency at the range from 60 to 400Mbps. The power consumption is 0.42mW at 400Mbps and the supply voltage of 0.7V which corresponds to 37% power reduction from the power consumption without optimal On-Time Controller.

A Wideband Voltage-Biased LC Oscillator with Reduced Flicker Noise Up-Conversion

AUTHORS:
F. Pepe, A. Bonfanti, S. Levantino, C. Samori, A.L. Lacaita, *Politecnico di Milano, Italy*

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ABSTRACT:
The demand of voltage-controlled oscillators (VCOs) with a broad tuning range can lead to unacceptable degradation of the $1/f^3$ phase-noise component if traditional voltage-biased topologies are implemented. In this paper, a novel VCO architecture is proposed, where a segmented transconductor tailors the negative g_m depending on the operating range to ensure that flicker-noise up-conversion remains minimal. The implemented oscillator covers both 4G and WiMAX 2.5-GHz operation modes and achieves a 10-dB reduction of the $1/f^3$ phase noise without impairing the $1/f^2$ phase-noise performance.

A 220dB FOM, 1.9GHz Oscillator Using a Phase Noise Reduction Technique for High-Q Oscillators

AUTHORS:
Kannan Sankaragomathi [1], Lori Callaghan [2], Richard Ruby [2], Brian Otis [1]
[1]University of Washington, USA ; [2]Avago Technologies, USA

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ABSTRACT:
We present a technique to reduce the close-in phase noise of high-Q (FBAR/MEMS/crystal) oscillators. The proposed technique suppresses the up-conversion of 1/f noise via AM-PM conversion by the addition of a non-linear capacitor to the tank. The proposed AM-PM suppression technique has no additional power penalty and incurs a minimal area penalty. Measurements from multiple dies of a 1.9GHZ FBAR oscillator show ≥3.5dB reduction in close-in phase noise using the proposed technique. The FBAR oscillator achieves a measured phase noise of -88dBc/Hz @ 1kHz, -116dBc/Hz @10kHz, -146dBc/Hz @ 1MHz offsets. The oscillator with the proposed technique achieves a Figure of Merit (FOM) of 220dB, which is 5.5dB better than the FBAR oscillator with lowest close-in phase noise reported to date [1].

A Current-Reuse Class-C LC-VCO with an Adaptive Bias Scheme

AUTHORS:
Teerachot Siriburanon, Wei Deng, Kenichi Okada, Akira Matsuzawa, *Tokyo Institute of Technology, Japan*

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ABSTRACT:
This paper proposes a low-power current-reuse complementary differential LC-VCO which is composed of a pair of NMOS and PMOS transistors with an adaptive bias scheme for both transistors to ensure its robust startup and achieve maximum swing in Class-C operation. The proposed VCO has been implemented in a standard 0.18μm CMOS technology, which oscillates at the carrier frequency of 4.6 GHz. The measured phase noise is -139.5dBc/Hz at 10 MHz offset while drawing a current consumption of 1.6 mA from 1.5 V supply. The Figure of Merit is -189.1 dBc/Hz. To the author's best knowledge, this is the first class-C current-reuse VCO with an adaptive bias scheme.

A 0.5V, 2.41GHz, 196.3dBc/Hz FoM Differential Colpitts VCO with an Output Voltage Swing Exceeding Supply and Ground Potential Requiring No Additional Inductor

AUTHORS:
Joo-Myoung Kim, Seong Joong Kim, Seok-Kyun Han, Sang-Gug Lee, *KAIST, Korea*

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ABSTRACT:
A low-voltage differential Colpitts VCO that achieves an output voltage swing above the supply voltage and below the ground potential to improve the phase noise while requiring no additional inductor for a small chip area is proposed. Implemented in a 65nm CMOS process, the proposed VCO achieves the phase noise of -131.05dBc/Hz at an offset of 1MHz from an oscillation frequency of 2.41GHz and a FoM of 196.3dBc/Hz while dissipating 1.74mW from a 0.5V supply.

Ultra-Low Phase Noise 7.2–8.7GHz Clip-and-Restore Oscillator with 191dBc/Hz FoM

AUTHORS:
Masoud Babaie [1], Akshay Visweswaran [1], Zhuobiao He [2], Robert Bogdan Staszewski [1]
[1] *Technische Universiteit Delft, The Netherlands* ; [2] *HiSilicon, China*

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ABSTRACT:
In this paper we investigate benefits of a recently introduced clip-and-restore (C&R) oscillator for ultra-low phase noise RF applications and reconsider the original choices in light of further insight into the oscillator behavior. We also tackle undesired resonance frequencies and exploit them to facilitate clipping with proper choices of tuning capacitances. Based on the new theory, the proposed oscillator was implemented in 65-nm CMOS and verified to achieve 4 dB better phase noise and 1.8 dB better FoM than the original C&R oscillator, thus making it the lowest phase noise CMOS oscillator ever published. The measured phase noise is -145 dBc/Hz at a 3 MHz offset from a 4.2 GHz carrier. The resulting average FoM is 191 dBc/Hz and varies less than 2 dB across the tuning range. It covers the 7.2–8.7 GHz frequency band for a 19% tuning range, drawing 32 mA from a 1.3 V power supply.

HF Mismatch Characterization and Modeling of Bipolar Transistors for RFIC Design

AUTHORS:
Tzung-Yin Lee, Yuh-Yue Chen, *Skyworks Solutions Inc., USA*

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ABSTRACT:
This paper presents a methodology to characterize and model BJT's mismatch behavior for RFIC design. A measurement technique based on the conventional S-parameter measurement is developed to measure the mismatch behavior at high frequencies (HFs). First, besides the typical de-embedding, the bondpad mismatch is subtracted statistically from the capacitance mismatch measurement. Second, a semi-empirical methodology using physical parameters, such as window CD and vertical doping, is developed to model the measured AC mismatch behavior for transistors of different size. Finally, a systematic procedure is proposed to extract the mismatch parameters, which can be used in the SPICE Monte-Carlo mismatch simulation. The proposed mismatch modeling methodology is validated on an industrial 0.35μm RF BiCMOS process. The proposed model fits the mismatch characteristics of the key AC parameters, such as C_{BE}, C_{BC}, and f_T at different current densities. The model also scales well with geometry for the transistors with sizes useful for RFIC application.

CMOS RF Noise, Scaling, and Compact Modeling for RFIC Design

AUTHORS:
Angelos Antonopoulos [1], Matthias Bucher [1], Konstantinos Papathanasiou [1], Nikolaos Makris [1], Rupendra K. Sharma [1], Paulius Sakalas [2], Michael Schroter [2]
[1] *Technical University of Crete, Greece* ; [2] *Technische Universität Dresden, Germany*

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ABSTRACT:
This work presents an analysis of high frequency noise and linearity performance of a 90 nm CMOS process. Measurements are performed for a wide range of nominal gate lengths and bias points at high frequency. Modeling is based on the EKV3 compact model in Spectre RF circuit simulator from Cadence. The model shows correct scalability for noise and linearity accounting for short channel effects (SCEs), such as velocity saturation (VS) and channel length modulation (CLM). Results are presented versus a common measure of channel inversion level, named inversion coefficient. Optimum performance is shown to gradually shift from higher to lower levels of moderate inversion, when scaling from 240 nm to 100 nm. The same trend is observed from investigating the transconductance frequency product (TFP) of a common-source (CS) LNA for technology nodes ranging from 180 nm to 22 nm.

An Automatic Parameter Extraction and Scalable Modeling Method for Transformers in RF Circuit

AUTHORS:
Jian Yao, Zuochang Ye, Yan Wang, *Tsinghua University, China*

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ABSTRACT:
In this paper, an automatic parameter extraction and scalable modeling method for transformer with 2π-based equivalent circuit-topology is established for the first time. In contrast to traditional optimization extraction, the adaptive boundary compression technique, combining a new correlated parameter extraction method with the neighboring geometry parameters, is introduced. The method is validated by 42 industry transformers and both accuracy and scalability have been achieved.

A 12ps True-Time-Delay Phase Shifter with 6.6% Delay Variation at 20–40GHz

AUTHORS:
Qian Ma, Domine M.W. Leenaerts, R. Mahmoudi, *Technische Universiteit Eindhoven, The Netherlands*

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ABSTRACT:
A fully integrated 2-channel Ka-band True Time Delay (TTD) phase shifter with 12ps continuous changing delay time has been realized in a 0.25μm SiGe:C BiCMOS technology. A delay variation cancellation technique is proposed, resulting in less than 0.8ps delay variation over a 20–40GHz frequency span, meanwhile maintaining a constant input impedance. In the high (low) power mode, the measured input 1dB compression point and input IP3 are +9.7dBm (+3.6dBm) and +18dBm (+13dBm) at 30GHz with an averaged power consumption per channel of 145mW (33mW) for the same TTD performance. The size of the core phase shifter is less than 0.1mm^2.

A PLL-Based BFSK Transmitter with Reconfigurable and PVT-Tolerant Class-C PA for MedRadio & ISM (433MHz) Standards

AUTHORS:
Karthik Natarajan, Daibashish Gangopadhyay, David Allstot, *University of Washington, USA*

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ABSTRACT:
An RF transmitter that uses closed-loop PLL-based BFSK modulation and is reconfigurable for both the MedRadio (402–405MHz) and 433 MHz ISM bands is introduced. Innovations include the first reconfigurable class-C PA, the first class-C PA with automatic calibration against PVT variations, and a low-power NMOS delay-based ring-VCO PLL. Several performance records are achieved: (1) The PA realizes a peak efficiency of 47% in the high-power (ISM) (-2 dBm) mode and 43% (33%) in the MedRadio -12 dBm (-16 dBm backoff) modes. (2) The PLL dissipates only 72 μW with a phase noise of -111 dBc/Hz @ 1 MHz, and (3) the overall transmit efficiencies are 29% and 17% for the -12 dBm and -16 dBm backoff levels for the MedRadio band and 44% for the ISM (433 MHz) bands.

A Low Power Miniaturized 1.95mm^2 Fully Integrated Transceiver with fastPLL Mode for IEEE 802.15.4 / Bluetooth Smart and Proprietary 2.4GHz Applications

AUTHORS:
Franz Pengg, David Barras, Martin Kucera, Nicola Scolari, Alexandre Vouilloz, *CSEM, Switzerland*

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ABSTRACT:
This paper presents an ultra-low power miniaturized single chip transceiver operating in the ISM band at 2.4GHz. Targeting low power and minimum die size, while excluding RF-options and minimizing the count of external components for low-cost, asks for appropriate architectural choices to obtain high performance. Fast PLL locking and immediate RX-TX turnaround minimize the consumption overhead at wake-up and turnaround. With a die size of only 1.95mm^2 in a 90nm standard digital CMOS technology, the receiver achieves a sensitivity of -94.5dBm (1Mbps, BER 10E-3) while consuming only 7.1mA and the transmitter consumes 9.2mA for 0dBm output power. The base-band is compliant with the IEEE 802.15.4 standard, the Bluetooth Smart standard (former Bluetooth low energy BLE) and can be configured for proprietary standards at 2.4GHz, with data-rates up to 3Mbps.

A 1.9nJ/bit, 5Mbps Multi-Standard ISM Band Wireless Transmitter Using Fully Digital PLL

AUTHORS:
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[1] *Texas Instruments Incorporated, USA* ; [2] *NVIDIA Incorporated, USA*

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ABSTRACT:
This paper presents an energy efficient transmitter for multi-standard applications (IEEE802.15.4, BLE, 5Mbps) in ISM2.4GHz band. It incorporates a fully digital PLL with two point modulation to achieve up to 5Mbps data rate at 9.5mW power consumption (including all power management blocks) at 0dBm output power, leading to 1.9nJ/b efficiency. The proposed digital PLL uses a counter based area and power efficient re-circulating TDC, current reuse low area DCO using resistive tail, process compensated high speed divider, class-AB PA stages, and fully integrated on-chip LDOs. The entire transmitter occupies 0.35mm^2 Silicon area in a 65nm digital CMOS process.

A Sub-GHz Low-Power Wireless Sensor Node with Remote Power-Up Receiver

AUTHORS:
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ABSTRACT:
A fully integrated low-power sub-GHz sensor node is presented for wireless sensor networks (WSN). The sensor node features a sensor IC and a RF transceiver IC, vertically assembled in a single QFN package. A unique remote power-up scheme is configured to supply the power to a sensor node from power-down state. It features a technique of centralized remote power-up scheme combined with local broadcasting power-up sequence to achieve ultra-low standby current, fast power-up time, and extended coverage. It proposes a time division switch to separate power-up message from data information, both propagated at the same frequency band. The standby current in power-down state draws less than 450nA. The sensitivity of power-up receiver is -24dBm, while the sensitivity of data receiver is -103dBm. The Sensor and RF transceiver ICs were fabricated in 0.25μm CMOS and 0.18μm RF CMOS, respectively.

A Receiver with In-Band IIP_3>20dBm, Exploiting Cancelling of OpAmp Finite-Gain-Induced Distortion via Negative Conductance

AUTHORS:
Dlovan H. Mahrof, Eric A.M. Klumperink, Mark S. Oude Alink, Bram Nauta, *University of Twente, The Netherlands*

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ABSTRACT:
Highly linear CMOS radio receivers increasingly exploit linear RF V-I conversion and passive down-mixing, followed by an OpAmp based Transimpedance Amplifier at baseband. Due to the finite OpAmp gain in wideband receivers operating with large signals, virtual ground is imperfect, inducing distortion currents. We propose to apply a negative conductance to cancel this distortion. In an RF receiver, this increases In-Band IIP_3 from 9dBm to >20dBm, at the cost of 1.5dB extra NF and <10% power penalty. In 1MHz bandwidth, a Spurious-Free Dynamic Range of 85dB is achieved at <27mA up to 2GHz for 1.2V supply voltage.

A Current-Mode mm-Wave Direct-Conversion Receiver with 7.5GHz Bandwidth, 3.8dB Minimum Noise-Figure and +1dBm $P_{1dB,out}$ Linearity for High Data Rate Communications

AUTHORS:
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[1] University of California at Los Angeles, USA ; [2] Broadcom, USA ; [3] TSMC, Taiwan

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ABSTRACT:
A current-mode mm-wave direct-conversion receiver breaking trade-offs among bandwidth, NF and linearity is designed and realized in 65nm CMOS. The 60GHz receiver employs novel Frequency-staggered Series Resonance Common Source (FSRCS) stage to extend RF bandwidth with superior noise performance. The receiver's current-mode operation offers excellent out-of-band blocker tolerance and linearity. With on-chip quadrature LO generations, the fabricated receiver simultaneously achieves minimal noise figure of 3.8dB, RF bandwidth of 7.5GHz, output P1dB of 1dBm, maximum conversion gain of 32dB, and IRR of -35dB. The receiver is capable of tolerating out-of-channel blocker up to -9dBm at 3.5GHz away. It occupies silicon area of 1.3mm^2 and draws 25.5mA from 1V supply.

Co-Design of 60GHz Wideband Front-End IC with On-Chip Tx/Rx Switch Based on Passive Macro-Modeling

AUTHORS:
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ABSTRACT:
Co-design of 60GHz wideband front-end IC with on-chip Tx/Rx switch in 65nm CMOS is presented. Passive macro-modeling (pmm) is utilized to convert S-parameter files from passive component EM simulations to state-space models in circuit netlist format which could be used in commercial SPICE simulator for various analyses without convergence issues. The co-design of on-chip switch and LNA/PA could achieve wideband matching and reduce the effects of insertion loss of on-chip Tx/Rx switch. Combining with gain boosting technique in LNA design and lumped-component based design methodology, the implemented 60GHz front-end IC with on-chip Tx/Rx switch achieves 3dB gain bandwidth of 12GHz with maximum gain 17.8dB and minimum NF 5.6dB in Rx mode and 3dB gain bandwidth of 10GHz with saturated output power 5.6dBm in Tx mode, and only consumes 1.0mm×1.2mm die area (including pads).

A 0.18-μm CMOS Fully Integrated Antenna Pulse Transceiver with Leakage-Cancellation Technique for Wide-Band Microwave Range Sensing Radar

AUTHORS:
Nguyen Ngoc Mai Khanh, Kunihiro Asada, *University of Tokyo, Japan*

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ABSTRACT:
This paper presents a leakage cancellation technique for on-chip transceiver for range sensing radar. A 180-nm CMOS transceiver with on-chip antennas is implemented with a 9–11-GHz damping-pulse transmitter (Tx) and a receiver (Rx) including a mixer and a 3-stage low-noise amplifier (LNA). By adding a polarity-reversal switch to the receiver mixer, leakage, reflected signals, and traveling time of transmitted pulses can be measured. Another improvement is the design of the Rx's mixer and the 3-stage wide-band LNA to reduce on-chip DC blocking capacitors. Experimental results with/without reflector placed at several distances from the transceiver are performed to demonstrate the technique. Pulse traveling times are measured with 0.8 ns, 1 ns, and 1.25 ns for the distance of 10 cm, 14 cm, and 18 cm, respectively. Furthermore, reflected signals are measured separately from leakage in cases of different distances.

245GHz Subharmonic Receivers in SiGe

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ABSTRACT:
Two subharmonic receivers for 245 GHz spectroscopy sensor applications in the 245 GHz ISM band have been proposed. One receiver consists of an 2nd APDP (antiparallel diode pair) passive SHM (subharmonic mixer), a 120 GHz push-push VCO with 1/64 divider, and a 120 GHz PA (power amplifier). The other consists of a single-ended four-stage CB (common base) LNA, an 2nd APDP passive SHM, an IF amplifier, a 120 GHz push-push VCO with 1/64 divider, and a 120 GHz PA. The receivers are fabricated in a SiGe:C BiCMOS technology with f_T/f_{max}=300/500 GHz. The measured conversion gain are -17 dB rsp. 10.6 dB at 245 GHz with 3-dB bandwidths of 13 GHz rsp. 14 GHz, and the single-side band noise figure are 17 dB rsp. 20 dB; the two receivers dissipates a power of 213 mW and 312 mW, respectively.

A mm-Wave FMCW Radar Transmitter Based on a Multirate ADPLL

AUTHORS:
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[1] *Technische Universiteit Delft, The Netherlands* ; [2] *USTC, China*

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ABSTRACT:
We present a 60-GHz FMCW radar transmitter based on an all-digital phase-locked loop (ADPLL) with ultra-wide linear frequency modulation. Multirate, two-point modulation generates an ultra-linear programmable frequency ramp. A novel, closed-loop DCO gain linearization method employing 24kb of SRAM realizes a GHz-level triangular chirp with high sweep linearity, and enables hitless modulation through multiple DCO tuning banks. Measured frequency error (i.e., nonlinearity) in the FMCW ramp is only 117-kHz_{rms} for a 62-GHz carrier with 1.22-GHz bandwidth. The synthesizer is transformer-coupled to a 3-stage neutralized power amplifier that delivers +5 dBm to a 50-Ω load. Implemented in 65-nm CMOS, the transmitter prototype consumes 89 mW from a 1.2-V supply.

A 440-μW 60-GHz Injection-Locked Frequency Divider in 65nm CMOS

AUTHORS:
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PAGE 111 – 114

ABSTRACT:
An ultra-low-power millimeter-wave injection-locked frequency divider (ILFD) based on transformer-feedback and transformer-distribution technique is proposed to operate with a very small injection signal. The proposed ILFD measures a locking range from 60.9GHz to 64.7GHz with -7dBm input power while consuming 440μW, which features the minimum power consumption among all the reported V-band frequency dividers. An interesting injection-saturation phenomenon is also identified and verified by measurement results.

An Automatically Placed-and-Routed ADPLL for the MedRadio Band Using PWM to Enhance DCO Resolution

AUTHORS:
Muhammad Faisal, David D. Wentzloff, *University of Michigan, USA*

PAGE 115 – 118

ABSTRACT:
An all-digital phase-locked loop for the MedRadio bands is presented. This ring oscillator based ADPLL was entirely designed and placed-and-routed using digital design flows and was fabricated in a 65 nm CMOS process. Pulse width modulation of the DCO control signals is introduced as a technique to improve the resolution of the DCO to 59 kHz/LSB. This ADPLL operates as a subsampling integer-N frequency synthesizer from 400 to 460 MHz, and consumes 2.1 mA from a 1 V supply, with an rms jitter of 13.3 ps.

A 2.4-GHz Low Power High Performance Frequency Synthesizer Based on Current-Reuse VCO and Symmetric Charge Pump

AUTHORS:
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ABSTRACT:
This paper presents a low power high performance frequency synthesizer. Based on the current-reuse VCO architecture, the whole system power consumption is significantly saved with excellent phase noise performance. Imbalance amplitude problems caused by the unsymmetrical VCO are solved by the pre-tuning mechanism, which automatically chooses the correct frequency band for the certain frequency channel. Besides, the symmetric charge pump (CP) can minimize the current mismatches and phase offset. The frequency synthesizer is fully integrated in 130-nm CMOS technology consuming 5.8mW. Measurement results show performance of -130 dBc/Hz at 1MHz offset phase noise, 450 fs rms jitter. The reference spur is below -75 dB, and it operates successfully with 1 Mbps GFSK signals as the two-point modulated transmitter.

A 73.9–83.5GHz Synthesizer with -111dBc/Hz Phase Noise at 10MHz Offset in a 130nm SiGe BiCMOS Technology

AUTHORS:
J.-O. Plouchart, Mark Ferriss, Bodhisatwa Sadhu, Mihai Sanduleanu, Benjamin Parker, Scott Reynolds,
IBM, USA

PAGE 123 – 126

ABSTRACT:
A 73.9–83.5 GHz synthesizer is implemented in a 130nm SiGe BiCMOS technology. The measured phase noise at 10KHz and 10MHz offset of the 82.4GHz carrier are -88.5dBc/Hz and -111dBc/Hz respectively. Reference spurs are -67 dBc. The synthesizer integrates voltage regulators and power management for SoC applications; it consumes 0.51 W from 1.5 V and 2.7 V supplies, and occupies 0.85 mm × 2.9 mm.

A 60nm WiFi/BT/GPS/FM Combo Connectivity SOC with Integrated Power Amplifiers, Virtual SP3T Switch, and Merged WiFi-BT Transceiver

AUTHORS:
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[1] *MediaTek, Taiwan* ; [2] *MediaTek, USA*

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ABSTRACT:
A highly integrated WiFi/BT/FM/GPS connectivity combo SOC is implemented in a 60nm CMOS process. This work presents the proposed WiFi/BT merged RF transceiver, a virtual SP3T switch, and DPD algorithm to save chip area, reduce BOM and enhance performance simultaneously. The WiFi/BT/FM/GPS RF transceiver areas are 1.7/1.3/0.8/1.0mm^2, respectively. The measured WiFi 11g 54Mbps RX sensitivity is -78dBm and Pout is 20dBm with EVM of -28dB. The measured BT GMSK RX sensitivity is -94dBm and Pout is 10dBm. FM sensitivity is -110dBm and GPS cold/hot-start TTFF sensitivity is -148/-163dBm.

Novel Silicon-on-Insulator SP5T Switch-LNA Front-End IC Enabling Concurrent Dual-Band 256-QAM 802.11ac WLAN Radio Operations

AUTHORS:
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Skyworks Solutions Inc., USA

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ABSTRACT:
An innovative SOI SP5T switch-LNA integrated circuit is presented. The switch-LNA consists of a diplexer that provides out-of-band rejection and enables dual-band concurrent operation, a dual-band LNA with bypass attenuators, and three high linearity transmit paths. Tx paths feature 0.1 dB compression at > 33 dBm input power, with > 35 dB Tx to Rx isolation, and 0.8 and 1.2 dB insertion loss for low and high bands respectively. Receive paths feature 12 dB gain with 2.5–2.8 dB NF. Cascading the design with a dual-band WLAN PA, a complex dual-band front-end module can be easily constructed in a 3 × 4 mm package, which demonstrates transmit and receive LNA linearity with EVM < 2% at >16 dBm and > -5dBm output power respectively and compliant with the linearity requirements of the 802.11ac standard up to of 256-QAM 80 MHz operations.

A Digitally-Calibrated 20-Gb/s 60-GHz Direct-Conversion Transceiver in 65-nm CMOS

AUTHORS:
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PAGE 137 – 140

ABSTRACT:
This paper presents a digitally-calibrated 60-GHz direct-conversion transceiver. To improve the error vector magnitude (EVM) performance over the wide bandwidth, a digital calibration technique is applied. The 60-GHz transceiver implemented by 65nm CMOS achieves the maximum data rates of 20 Gb/s in 16QAM mode. The transmitter and receiver consume 351mW and 238mW from 1.2V supply, respectively. As a 60-GHz transceiver, the best Tx-to-Rx EVM performance of -26.2 dB is achieved for 16QAM 7Gb/s data rate.

A Low-Current Digitally Predistorted 3G-4G Transmitter in 40nm CMOS

AUTHORS:
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[1] *MediaTek, UK* ; [2] *MediaTek, Singapore* ; [3] *MediaTek, Taiwan*

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ABSTRACT:
To create a wide-band transmit path with high current efficiency a single-balanced passive modulator is combined with a class-B single-ended resonant driver. The linearity of such configuration is limited by a strong 3rd harmonic response of the modulator combined with a strong third-order intermodulation in the driver. A novel digital pre-distortion approach is presented to enable good linearity under these highly non-linear conditions. Implemented in 40nm CMOS, the modulator and driver combined consume only 45mW to deliver a +3dBm Release 99 WCDMA signal with 1.1% EVM, -54dBc ACLR and -160dBc/Hz noise in the RX band. The ACLR remains below -50dBc over temperature, frequency and TX-power without adjustment of the predistortion coefficients. The transmitter delivers +0dBm 10MHz LTE with -51dBc ACLR.

A Passive Mixer-First Receiver Front-End without External Components for Mobile TV Applications

AUTHORS:
Inyoung Choi, Bumman Kim, *POSTECH, Korea*

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ABSTRACT:
This paper describes a passive mixer-first receiver front-end (RFE) for mobile TV covering 100MHz to 800MHz without any external components. The proposed input matching technique with RC discharging circuit achieves a simple topology with a low noise. The out-of-band linearity is enhanced using the low pass filtering of sampling capacitor, delivering an outstanding out-of-band linearity. The out-of-band IIP3 and IIP2 are 7dBm and 36dBm, respectively at the maximum gain setting of 36dB. The third and fifth harmonic rejection ratios (HRR) are 49dB and 42dB, respectively. The power consumption is 23mW and the maximum NF is 3.6dB. The active area occupies 0.33mm^2 in 65nm CMOS technology.

A 2-D GRO Vernier Time-to-Digital Converter with Large Input Range and Small Latency

AUTHORS:
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ABSTRACT:
The proposed time-to-digital converter (TDC) arranges two Vernier gated-ring-oscillator (GRO) branches in a 2-dimension (2-D) fashion. All delay differences between X phases and Y phases can be used, rather than only the diagonal line. The large latency time inherited from Vernier structure is therefore dramatically reduced. The TDC is implemented in a 90nm CMOS process and consumes 1.8mA from 1.2V. The measured input range can safely cover a full period of a 50MHz sampling signal. With the same delay elements, the latency time is less than 1/6 of that needed in a standard Vernier TDC.

A 130nm CMOS Polar Quantizer for Cellular Applications

AUTHORS:
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University of California at Irvine, USA

PAGE 155 – 158

ABSTRACT:
A polar quantizer is presented for detection and quantization of modulated signals in cellular applications. It consists of amplitude and phase quantizers. A time-to-digital converter (TDC) is designed to measure and quantize the phase, while a typical ADC is used for amplitude quantization. Polar quantizer significantly reduces the sensitivity of the quantizer to amplitude resolution. The 10 bit polar quantizer fabricated in 130nm CMOS achieves 5.5dB of SQNR improvement compared to rectangular quantizer for signal bandwidths as high as 20MHz.

A 6GHz Input Bandwidth $2V_{pp\text{-}diff}$ Input Range 6.4 GS/s Track-and-Hold Circuit in 0.25μm BiCMOS

AUTHORS:
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[1] Universität Stuttgart, Germany ; [2] Cassidian, Germany

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ABSTRACT:
A 0.25 μm SiGe-BiCMOS 6.4 GS/s track-and-hold circuit with an input bandwidth exceeding 6 GHz and up to 2 $V_{pp\text{-}diff}$ input voltage range applies a hold-mode muted preamplifier that reduces signal feedthrough and improves linearity. The track-and-hold circuit provides more than 59 dBc hold-mode SFDR3 for 1.0 to 6.0 GHz $1V_{pp\text{-}diff}$ input signals at 6.4 GS/s, outperforming the best commercial THs operated at only 4 GS/s.

A 10-b, 300-MS/s Power DAC with 6-V_{pp} Differential Swing

AUTHORS:
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ABSTRACT:
A 10-bit digital-to-analog converter (DAC) is presented that delivers 6-V_{pp} into a 100-Ω differential load. The circuit is implemented in 45-nm CMOS SOI, which provides benefits for using a FET-stack current buffer. The measured DNL is better than 0.44 LSB. The DAC consumes 476 mW and achieves a peak SFDR of 54.4 dB and a minimum IM3 of -55.6 dBc. This DAC demonstrates the largest output swing and highest power efficiency for a high-resolution (>8b), high-speed (>100MS/s) DAC.

A 2×13-bit All-Digital I/Q RF-DAC in 65-nm CMOS

AUTHORS:
Morteza S. Alavi, George Voicu, Robert Bogdan Staszewski, Leo C.N. de Vreede, John R. Long,
Technische Universiteit Delft, The Netherlands

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ABSTRACT:
This paper presents a 2×13-bit I/Q RF-DAC-based all-digital modulator realized in 65 nm CMOS. The proposed quadrature up-converter uses a 25% duty-cycle clock to isolate the in-phase (I) and quadrature-phase (Q) modulating signals before combining. Using a 1.2 V supply and an on-chip power combiner, the modulator provides more than 21 dBm RF output power within a frequency range of 1.36 to 2.51 GHz. The peak RF output power, overall system and drain energy efficiencies of the modulator are 22.3 dBm, 31.5%, and 39.7%, respectively. Applying digital predistortion (DPD), 64 & 256 constellation points are measured with EVM better than -30 dB. The measured noise floor is below -160 dBc/Hz, with an IQ image rejection and LO leakage of -65 and -63 dBc, respectively. Its linearity has been evaluated with WCDMA modulation. Using DPD, the linearity improves by more than 15 dB.

Ultra-Low Voltage and Low Power UWB CMOS LNA Using Forward Body Biases

AUTHORS:
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PAGE 173 – 176

ABSTRACT:
An ultra-wideband (UWB) low noise amplifier (LNA) was designed and fabricated using 0.18μm 1.8V CMOS technology. The adoption of forward body biases (FBB) in a 3-stage distributed amplifier enables an aggressive scaling of the supply voltages and gate input voltage to 0.6V. The low voltage feature from FBB leads to more than 50% power consumption saving to 4.2mW. The measured power gain (S_{21}) is higher than 10dB in 3.1~8.1GHz and noise figure is 2.83~4.7 dB in the wideband of 2~10GHz. Superior linearity is achieved with IIP3 as high as 4.2dBm and 12.5dBm at 6.5GHz and 10GHz, respectively.

A DC-9.5GHz Noise-Canceling Distributed LNA in 65nm CMOS

AUTHORS:
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ABSTRACT:
A low noise amplifier is presented that uniquely achieves wide-band input matching and good low-frequency noise performance at the same time. Its topology is a hybrid of distributed amplifier and a common-source common-gate noise-canceling amplifier. The proof-of-principle prototype in 65nm CMOS operates from DC up to 9.5GHz with more than 12dB gain, achieves a minimum noise figure of 2.8dB, P_{1dB} of -7dBm, IIP_3 of +4dBm, consumes 18mW from a 1.4V power supply and occupies a total active area of 0.4mm^2.

A Highly Linear Low-Noise Amplifier Using a Wideband Linearization Technique with Tunable Multiple Gated Transistors

AUTHORS:
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ABSTRACT:
A wideband linearization technique using tunable multiple gated transistors (MGTRs) is proposed. Extra tunable input capacitors and the modified derivative superposition (DS) method are also adopted to increase the amplifier's linearity at RF. A low-noise amplifier (LNA) employing the proposed linearization technique has been developed with 0.18-μm CMOS process for various mobile TV standards in UHF band (470–862 MHz). The LNA achieves 19-dBm IIP_3, 16.5-dB gain, and 1.33-dB NF with 10.8-mW power consumption. Over the desired UHF band, the LNA increases the average IIP_3 obtained with off-state auxiliary transistor by 11.7 dBm.

A Highly Selective LNTA Capable of Large-Signal Handling for RF Receiver Front-Ends

AUTHORS:
M. Mehrpoo, Robert Bogdan Staszewski, *Technische Universiteit Delft, The Netherlands*

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ABSTRACT:
To achieve ultimately flexible multi-core radio operation, wide-band receiver RF front-ends must be robust against interference well in excess of the requirements usually specified by a radio standard. In this paper, a highly selective, very linear low-noise transconductance amplifier (LNTA) capable of large-signal handling for current-mode receiver (RX) front-ends is proposed and implemented in 65-nm CMOS. It is shown that by combining on-chip high-Q bandpass filters with a push/pull class-AB common-gate stage, a measured 1-dB desensitization point (B_{1dB}) and large-signal IIP3 of +8 dBm and +20 dBm, respectively, can be achieved. In addition, by applying a noise cancellation technique, via an auxiliary push/pull class-AB common-source stage, the proposed LNTA measures a moderate NF of 5.9 dB, which is a very competitive number for such high value of B_{1dB}. The circuit consumes 7.5 mA at 1.5 V.

A 62GHz Inductor-Peaked Rectifier with 7% Efficiency

AUTHORS:
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Technische Universiteit Eindhoven, The Netherlands A

PAGE 189 – 192

ABSTRACT:
This paper presents the first 62 GHz fully on-chip RF-DC rectifier in 65nm CMOS technology. The rectifier is the bottleneck in realizing on-chip wireless power receivers. In this paper, efficiency problems of the mm-wave rectifier are discussed and the inductor-peaked rectifier structure is proposed and realized. By using an inductor-peaked diode connected transistor, self-threshold voltage modulation, and an output filter, the measured rectifier reaches 7% efficiency with 1 mA current load. Compared to previous state-of-art 45 GHz rectifier with 1.2% efficiency [1], our solution achieves a higher efficiency at a higher frequency, providing a better solution for mm-wave wireless power receivers.

A 5.12–12.95GHz Triple-Resonance Low Phase Noise CMOS VCO for Software-Defined Radio Applications

AUTHORS:
M. Moslehi Bajestan, K. Entesari, *Texas A&M University, USA*

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ABSTRACT:
This paper presents a wide-tuning range Voltage-Controlled Oscillator (VCO) for software-defined radio (SDR) applications using a resonator with three potential oscillation modes. The implemented prototype in 0.18μm CMOS technology achieves a continuous tuning range of 86.7% from 5.12GHz to 12.95GHz while drawing 5 to 10mA current from 1-V supply. The measured phase noise at 1MHz offset from carrier frequencies of 5.9, 9.12 and 12.25GHz is -122.9, -117.1 and -110.5dBc/Hz, respectively. The VCO occupies a chip area of 0.33mm^2.

A -189dBc/Hz FOM_T Wide Tuning Range Ka-Band VCO Using Tunable Negative Capacitance and Inductance Redistribution

AUTHORS:
Qiyang Wu [1], Salma Elabd [1], Tony K. Quach [2], Aji Mattamana [2], Steve R. Dooley [2], Jamin McCue [1], Pompei L. Orlando [2], Gregory L. Creech [1], Waleed Khalil [1]
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ABSTRACT:
An ultra wideband LC voltage-controlled oscillator (LC-VCO) operating in the Ka-band with equally spaced sub-band coarse tuning characteristics is proposed and characterized. A tunable negative capacitance (TNC) circuit technique is used to cancel the fixed capacitance in the LC-tank to extend the tuning range (TR). A digitally-switched varactor coarse tuning structure with an inductance redistribution technique is utilized to reduce VCO gain (K_V) and retain uniform spacing between tuning curves. The proposed VCO structure and a baseline VCO are fabricated in a 130 nm CMOS process. Compared to the reference VCO, the proposed VCO achieves a 34% increase in TR with maximum K_V of 450 MHz/V. The measured worst-case phase noise is -100.1 dBc/Hz at 1 MHz offset across the TR from 30.5 GHz to 39.6 GHz. The power dissipation of the VCO core is 11 mW from a 1.2 V supply. The TNC-based VCO achieves a FOM_T of -189 dBc/Hz, which is the highest reported at the Ka-band.

A Dual-Band LO Generation System Using a 40GHz VCO with a Phase Noise of -106.8dBc/Hz at 1-MHz

AUTHORS:
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ABSTRACT:
This paper demonstrates a dual-band LO generation system using a low phase noise single-band 40GHz VCO as the signal source. The LO generation system has two outputs: single-band LO1 at 20GHz and dual-band LO2 switchable between 10GHz and 15GHz. Implemented in 0.25-μm SiGe:C BiCMOS, the VCO achieves a phase noise of -106.8dBc/Hz at 1-MHz offset from 40GHz with a frequency tuning range of 9.7%.

A 120GHz Quadrature Frequency Generator with 16.2GHz Tuning Range in 45nm CMOS

AUTHORS:
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PAGE 207 – 210

ABSTRACT:
This paper presents a new architecture for a 120GHz quadrature frequency generator with large tuning range and immunity against PA-VCO coupling. Combining the output signals of two independent oscillators, the pulling effect is removed and the oscillator can be integrated with a PA and an antenna on the same chip. This architecture also makes quadrature generation with large tuning range feasible at 120GHz. The chip is fabricated in a 45nm CMOS technology and shows a tuning range of 16.2GHz (13.5%), a phase noise of -112dBc/Hz @ 10MHz offset and a phase error of 5°.

An FM Demodulator Operating Across 2–10GHz IF

AUTHORS:
Akshay Visweswaran, John R. Long, Luca Galatro, Marco Spirito, Robert Bogdan Staszewski, *Technische Universiteit Delft, The Netherlands*

PAGE 213 – 216

ABSTRACT:
An FM demodulator operating across 8GHz IF bandwidth for application in low-power, wideband heterodyne receivers is presented. A 4-stage ring oscillator is frequency modulated by a wideband input. Locking to 1/4th the input frequency, it divides the FM deviation by four, thereby reducing the energy required for wideband demodulation to 0.75nJ/bit. Autocorrelation of the quadrature-phased outputs using a new low-power folded CMOS mixer is capable of detecting FM up to 400Mb/s over 2–10GHz IF. The inductorless 65nm CMOS prototype circuit occupies 0.17mm^2 and dissipates 3mW from 1.2V.

A 3.4mW 65nm CMOS 5th Order Programmable Active-RC Channel Select Filter for LTE Receivers

AUTHORS:
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ABSTRACT:
In this work a low power 5th order Chebyshev active-RC low pass filter that meets Rel-8 LTE receiver requirements has been designed with programmable bandwidth and overshoot. Designed for a homodyne LTE receiver, filter bandwidths from 700kHz to 10MHz are supported. The bandwidth of the operational amplifiers is improved using a novel phase enhancement technique. The filter was implemented in 65nm CMOS technology with a core area of 0.29mm^2. Its total current consumption is 2.83mA from a 1.2V supply. The measured input referred noise is 39nV/$\sqrt{Hz}$, the in-band IIP3 is 21.5dBm, at the band-edge the IIP3 is 20.7dBm, the out-of-band IIP3 is 20.6dBm, and the compression point is 0dBm.

A Low-Q Resonant Tank Phase Modulator for Outphasing Transmitters

AUTHORS:
Gilad Yahalom, Joel L. Dawson, *MIT, USA*

PAGE 221 – 224

ABSTRACT:
A new design concept is proposed for a phase modulator for outphasing transmitter architectures, utilizing the phase shifting capabilities of a resonant tank and the ability to separately control the circuit properties via its components. A prototype in 65-nm CMOS achieves 12 bits of resolution, with a fast settling time of less than five carrier cycles to within 1°. The circuit is also tested as a stand-alone transmitter showing an EVM of less than 5% for 8-PSK modulation at maximum data rate, meeting the FCC requirements for operation at the medical implant communication services (MICS) band.

A Linear-in-dB Analog Baseband Circuit for Low Power 60GHz Receiver in Standard 65nm CMOS

AUTHORS:
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[1] *Intel Corporation, USA* ; [2] *Intel Corporation, Israel*

PAGE 225 – 228

ABSTRACT:
This paper presents an analog baseband (ABB) circuit for low power 60 GHz wireless receiver in standard 65 nm CMOS. The proposed analog baseband system combines variable gain amplifiers (VGA) with a 3rd-order type II Chebyshev filter and provides linear steps as well as filter tuning range to achieve sufficient out-of-band rejection. The ABB demonstrates 2 dB gain step tuning range from 3–31 dB, 3-dB bandwidth of 980 MHz, OP1dB of 0dBm, and noise figure of 6 dB to 21 dB. The ABB consumes 48 mW at max gain setting and 32 mW at minimum gain setting from a 1.1 V supply. The entire ABB occupies an area of 1.1 mm^2 with active area of 0.2 mm^2.

A 100GHz Active-Varactor VCO and a Bi-Directionally Injection-Locked Loop in 65nm CMOS

AUTHORS:
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PAGE 231 – 234

ABSTRACT:
A 100GHz fundamental active-varactor VCO and a bi-directionally injection-locked loop are demonstrated in 65nm CMOS. Without using a conventional passive varactor, the proposed VCO achieves a tuning range of 5.2% at 100GHz and a phase noise of -112.1dBc/Hz at 10MHz offset. By utilizing the proposed transmission-line-based capacitive coupling, four oscillators are injection-locked properly and the loop creates eight phases of the carrier and 6dB(=10log4) of phase noise improvement, realizing a measured phase noise is -118.8dBc/Hz at 10MHz offset.

A Multichannel, Multicore mm-Wave Clustered VCO with Phase Noise, Tuning Range, and Lifetime Reliability Enhancements

AUTHORS:
Farid Shirinfar [1], Med Nariman [2], Tirdad Sowlati [2], Maryam Rofougaran [2], Reza Rofougaran [2], Sudhakar Pamarti [1]
[1] University of California at Los Angeles, USA ; [2] Broadcom, USA

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ABSTRACT:
Clustering and multi-core transformer coupling techniques are presented to improve phase noise, tuning range, and reliability of a mm-wave VCO. A proof-of-concept design targeting the WiGig protocol is shown. Each cluster of VCOs covers one channel resulting in better phase noise performance. Multicores of VCOs with uncorrelated noise are combined using transformers to further enhance phase noise and combat the voltage swing reliability issues. Furthermore, due to realization of multiple inductive elements in parallel instead of one small inductor, this approach bypasses Q-degradation of small inductors (<50pH). The VCO achieves a phase noise of -101.8dBc/Hz at 1MHz offset with over 12.6% tuning range (50.7GHz to 57.5GHz) and an FOM of -183dB/Hz.

A 105GHz VCO with 9.5% Tuning Range and 2.8mW Peak Output Power Using Coupled Colpitts Oscillators in 65nm Bulk CMOS

AUTHORS:
Muhammad Adnan, Ehsan Afshari, *Cornell University, USA*

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ABSTRACT:
In this work, a loop of unidirectionally coupled oscillators to demonstrate high tuning range and output power is proposed. To achieve large tuning range, two different tuning mechanisms are simultaneously exploited. First each core oscillator is tuned using a variable capacitor. Next, by controlling the phase/delay between the coupled oscillators, the entire loop dynamics and hence its frequency is tuned. In this paper, we analyze a loop of "n" coupled oscillators using Adler's equation and derive the expression for the maximum tuning range. The proposed system is designed and implemented using four coupled Colpitts VCOs in a 65nm bulk CMOS process. The VCO achieves continuous tuning range of 9.5% at the center frequency of 105GHz with the peak output power of 2.8mW. The circuit consumes 54mW from a 1.2V supply. To the best of our knowledge, this VCO has the highest output power and tuning range among all the CMOS oscillators at or above 100GHz.

Dual-Core High-Swing Class-C Oscillator with Ultra-Low Phase Noise

AUTHORS:
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PAGE 243 – 246

ABSTRACT:
We propose an ultra-low phase noise oscillator topology that works on the premise that coupling a second identical oscillator core would reduce the overall phase noise by 3 dB. For each core, a high-swing class-C oscillator is used to achieve the lowest phase noise. The realized oscillator is tunable from 4.07–4.91 GHz, drawing 39–59 mA from a 2.15 V power supply. The measured phase noise is -146.7 dBc/Hz and -163.1 dBc/Hz at 3 MHz and 20 MHz offset, respectively, from 4.07 GHz carrier. This is the lowest ever reported phase noise in bulk CMOS IC. This phase noise meets GSM900 normal basestation receiver and mobile station transmitter standards, which have the toughest phase noise requirements in cellular communications.

A 42 to 47-GHz, 8-bit I/Q Digital-to-RF Converter with 21-dBm P_{sat} and 16% PAE in 45-nm SOI CMOS

AUTHORS:
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[1]*University of California at San Diego, USA* ; [2]*Brown University, USA*

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ABSTRACT:
A novel stacked FET digital-to-RF converter is implemented in 45-nm SOI CMOS, which shares DC current through an I/Q digital-to-analog converter (DAC), I/Q mixer, and stacked-FET PA to provide high output power. The proposed architecture transmits at 1.25 Gbps for QPSK at 45GHz. This transmitter exhibits a 21.3-dBm saturated output power, while achieving a peak PAE of 16%. The circuit occupies $0.3mm^2$ including pads, while the PAE and P_{sat} remains above 13% and 18 dBm from 42 to 47 GHz.

A 32-Gbps 4×4 Passive Cross-Point Switch in 45-nm SOI CMOS

AUTHORS:
Donghyup Shin, Gabriel M. Rebeiz, *University of California at San Diego, USA*

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ABSTRACT:
This paper presents a passive 4×4 cross-point switch in 45-nm SOI CMOS technology for LVDS systems with near-zero power consumption. The CMOS switch dimensions and layout structures are optimized using full-wave electromagnetic simulations for the highest 3-dB bandwidth in order to maximize the data-rate for digital signal transmission. Also, a novel series switch is used between the cells to enhance the bandwidth. The 4×4 switch matrix results in a measured 3-dB bandwidth of ~ 20–25 GHz (depending on the path) and an isolation > 40 dB at 26.5 GHz. The group delay variation is < ±5 psec, and results in very low jitter as seen from eye measurements (< 1.3 psec). Good eye-openings are obtained at 26 Gbps and up to 31.5 Gbps. The design is readily scalable to an 8×8 cross-point switch matrix.

A 20Gb/s 136fJ/b 12.5Gb/s/μm On-Chip Link in 28nm CMOS

AUTHORS:
Meisam Honarvar Nazari, Azita Emami-Neyestanak, *California Institute of Technology, USA*

PAGE 257 – 260

ABSTRACT:
A high data rate, low power on-chip link in 28nm CMOS is presented. It features a double-sampling receiver with dynamic offset modulation and a capacitively-driven transmitter. The functionality of the link was validated using 4–7mm minimum-pitch on-chip wires. It achieves up to 20Gb/s of data rate (13.9Gb/s/μm) with BER$< 10^{-12}$. It has better than 136fJ/b of power efficiency at 10Gb/s. The total area of the transmitter and receiver is 1110μm^2.

A Wideband Injection Locking Scheme and Quadrature Phase Generation in 65nm CMOS

AUTHORS:
Mayank Raj, Azita Emami-Neyestanak, *California Institute of Technology, USA*

PAGE 261 – 264

ABSTRACT:
A novel technique for wideband injection locking in an LC oscillator is proposed. PLL and injection locking elements are combined symbiotically to achieve wide locking range while retaining the simplicity of the latter. This method doesn't require a phase frequency detector or a loop filter to achieve phase lock. 13.4GHz–17.2GHz locking range and an average jitter tracking bandwidth of up to 400 MHz was measured in a high-*Q* LC oscillator. This architecture is used to generate quadrature phases form a single clock without any frequency division, and to provide high frequency jitter filtering while retaining the low frequency correlated jitter essential for clock forwarded receivers.

Electronic Laser Phase Noise Reduction

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PAGE 265 – 268

ABSTRACT:
The first integrated wideband laser phase noise reduction scheme is presented where the laser phase noise is first detected using a photonic chip, processed using an electronic chip, and subtracted from the laser phase in a feed-forward manner. The proof-of-concept experiments on a commercially available 1553nm distributed feedback laser show linewidth reduction from 6MHz to 250kHz equivalent to 14dB phase noise improvement. The hybrid integration of the photonic and electronic chips enables dramatic power consumption and area reduction compared to bench-top designs. This feed-forward scheme performs wideband phase noise reduction independent of the light source and, as such, it is compatible with several types of lasers.

A 53-to-73GHz Power Amplifier with 74.5mW/μm^2 Output Power Density by 2D Differential Power Combining in 65nm CMOS

AUTHORS:
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ABSTRACT:
Towards wide bandwidth and high output power density for 60GHz PA design in 65nm CMOS, this paper introduces a 2D differential power combining network by metamaterial-based zero-phase-shifter. Simultaneous distributed amplification and power combining can be achieved with improved performances in both power density and bandwidth. The PA measurement results show 13.2 dB gain, 8.7% PAE, 13dBm P1dB, and 20GHz bandwidth (53 to 73GHz) within an area of 0.268mm^2.

Analysis, Design and Implementation of mm-Wave SiGe Stacked Class-E Power Amplifiers

AUTHORS:
Kunal Datta, Jonathan Roderick, Hossein Hashemi, *University of Southern California, USA*

PAGE 275 – 278

ABSTRACT:
Design equations and performance limits of stacked Class-E power amplifiers at mm-waves, including the limitations imposed by device parasitics, are presented in this paper. As a proof of concept of this parasitic aware mm-wave Class-E design methodology and to demonstrate the beyond BVCEO Class-E operation in a stacked architecture at mm-wave frequencies, a Q-band, single ended, two-stage, double-stacked, Class-E power amplifier is designed in a 0.13 μm SiGe HBT BiCMOS process. The measured performance of the fabricated chip show 23.4 dBm maximum output power at 34.9% peak power added efficiency (PAE), and 14.6 dB of power gain across 5 GHz centered around 41 GHz for a supply voltage of 4 V. The total chip area including the pads is 0.8 mm $\times$ 1.28 mm.

A Fully Integrated 22.6dBm mm-Wave PA in 40nm CMOS

AUTHORS:
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[1] *University of California at Los Angeles, USA* ; [2] *Broadcom, USA*

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ABSTRACT:
A fully integrated 60GHz CMOS PA with a P_{SAT} of 22.6dBm is presented. To our knowledge, this is the highest reported P_{SAT} at mm-waves in standard CMOS. To achieve a high power level, 32 differential PAs are combined through a network of transmission lines, Wilkinson combiners, and a multi-port argyle transformer. This method of combining minimizes loss while implementing a low impedance load (~12Ω) at the drains of each of the last stage PAs. Electromigration and other reliability issues are discussed.

Large-Scale Power-Combining and Linearization in Watt-Class mmWave CMOS Power Amplifiers

AUTHORS:
Ritesh Bhat, Anandaroop Chakrabarti, Harish Krishnaswamy, *Columbia University, USA*

PAGE 283 – 286

ABSTRACT:
Switching-class PAs employing device-stacking have been recently explored to meet the challenge of efficient power amplification at mmWave frequencies at moderate power levels of around 20dBm. In this paper, we propose the use of a single-step, large-scale (8-way), 75%-efficient lumped quarter-wave power combiner that is co-designed with stacked Class-E-like PA unit cells to enable a Q-band 45nm SOI CMOS PA with a peak P_{sat} of 27.2dBm (>0.5W), peak PAE of 10.7% and 1dB flatness in P_{sat} over nearly the entire Q-band (33–46GHz). This measured output power level is approximately 5× higher than prior reported mmWave silicon PAs. In order to support complex modulations with high average-efficiency, we also propose a novel linearizing architecture that combines large-scale power combining, supply-switching for efficiency under backoff and dynamic load modulation for linearization. A second fully-integrated 42.5GHz 45nm SOI CMOS PA is implemented based on this architecture and achieves 60% of the peak efficiency at 6dB back-off.

A 135–170GHz Power Amplifier in an Advanced SiGe HBT Technology

AUTHORS:
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ABSTRACT:
High-power, broadband power amplifiers (PA) operating in the D-band (110–170 GHz) are essential towards implementation of broadband frequency multiplier chains at sub-mmWave frequencies. In this paper we present the design of a 3-stage power amplifier (PA) with 3-dB bandwidth of 35 GHz (135–170 GHz) and implemented in 130 nm SiGe BiCMOS technology. A staggered tuning approach where the peak gain of the individual or group of individual stages are tuned at offset frequencies is used for broadband operation. In the 135–170 GHz, the small signal gain for the PA is 14–17 dB and the saturated output power (P_{sat}) varies from 5–8 dBm and the output referred 1 dB compression point (P_{1dB}) varies from 1–6 dBm over this frequency range. The nominal dc power consumption of this PA is 320 mW with peak PAE of 1.6%. To our best knowledge, this is the highest bandwidth reported for silicon PAs in the D band.

24GHz CMOS Transceiver with Novel T/R Switching Concept for Indoor Localization

AUTHORS:
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ABSTRACT:
This paper presents a 130 nm CMOS transceiver for 24 GHz wireless indoor localization. Due to a novel Rx/Tx switching concept RF-losses between receiver/transmitter and antenna could be reduced and the T/R isolation was drastically improved. The measured transceiver chip achieves an output power and noise figure of >5 dBm and <6 dB, respectively with 2 mm^2 total chip size. The complete transceiver consumes 16 mW in the Rx- and 26 mW in the Tx-mode. The RF-transceiver-chip was integrated with a DSP-unit and mounted on a PCB for wireless indoor localization demonstration. The measured results show a distance measurement precision in the cm-range.

A Low Power 60-GHz 2.2-Gbps UWB Transceiver with Integrated Antennas for Short Range Communications

AUTHORS:
Alexandre Siligaris, Fabrice Chaix, Michaël Pelissier, Vincent Puyal, José Zevallos, Laurent Dussopt, Pierre Vincent, *CEA-LETI, France*

PAGE 297 – 300

ABSTRACT:
A 60-GHz low power fully integrated transceiver including antennas, fabricated in CMOS 65nm SOI and packaged in low cost QFN is described. The circuit achieves 2 Gbps and 500 Mbps rates at 7.5 cm and 22.5 cm transmission ranges respectively. The transceiver energy efficiency is lower than 50 pJ/bit thanks to scalable power consumption using pulse generator and Super Regenerator Oscillator architecture.

A 283GHz Low Power Heterodyne Receiver with On-Chip Local Oscillator in 65nm CMOS Process

AUTHORS:
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ABSTRACT:
A Fully integrated 283 GHz heterodyne receiver in 65 nm CMOS process is presented in this paper. The circuit includes a resistive differential mixer, an intermediate frequency amplifier and a 282 GHz sub-harmonic injection locked oscillator. The on-chip oscillator generates a 94 GHz fundamental tone but exploits a 282 GHz third harmonic. An injection signal of 47 GHz (one sixth of the RF frequency) is used to lock the oscillator on a reference. The receiver measured conversion gain is -6 dB for a DC power consumption of 97.6 mW. Simulated noise figure is 38 dB. The chip size is 820 μm $\times$ 780 μm including matching networks and DC/RF pads.

A 240GHz Direct Conversion IQ Receiver in 0.13μm SiGe BiCMOS Technology

AUTHORS:
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[1] IHP, Germany ; [2] Technische Universität Dresden, Germany ; [3] Universität Paderborn, Germany

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ABSTRACT:
A 240 GHz direct conversion IQ receiver manufactured in 0.13μm SiGe BiCMOS technology with f_T/f_{max} of 300/500 GHz is presented. The receiver consists of a four stage LNA, an active power divider, an LO IQ generation network, and direct down-conversion fundamental mixers. The integrated IQ receiver yields a conversion gain of 18 dB, an 18 dB simulated DSB NF, and a 3 dB bandwidth of 25 GHz. The required 245 GHz LO power is in the order of - 10 dBm. The receiver exhibits an IQ amplitude and phase imbalance of 1 dB and 3° respectively. It draws 135 mA from the 3.5 V supply and 20 mA from 2 V.

A 240GHz Single-Chip Radar Transceiver in a SiGe Bipolar Technology with On-Chip Antennas and Ultra-Wide Tuning Range

AUTHORS:
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[1]Ruhr-Universität Bochum, Germany ; [2]Fraunhofer FHR, Germany ; [3]Infineon Technologies, Germany ; [4]KROHNE Messtechnik, Germany

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ABSTRACT:
This paper presents an ultra-wideband single-chip radar transceiver MMIC around 240 GHz in a SiGe:C bipolar laboratory technology with an f_T of 240 GHz and f_{max} of 380 GHz. The presented transceiver architecture consists of a fundamental 120 GHz VCO, two 240 GHz frequency doublers, a fundamental 240 GHz down-conversion mixer, a divide-by-four stage, a PLL-mixer and two on-chip patch antennas. The complete transceiver architecture is fully differential. The chip facilitates a -1 dBm peak output power (EIRP) at the transmit patch antenna and a tuning range of 61 GHz. The phase noise at 1 MHz offset is -84 dBc/Hz at 240 GHz (and better than -76 dBc/Hz over the full tuning range). The 240 GHz mixer offers a simulated noise figure below 17 dB, a simulated conversion gain of better than 5 dB, and an input referred compression point of -1.3 dBm. The results are achieved with a power consumption of 750 mW from a single 5 V supply.

A 0.5-to-3GHz Software-Defined Radio Receiver Using Sample Domain Signal Processing

AUTHORS:
Run Chen, Hossein Hashemi, *University of Southern California, USA*

PAGE 315 – 318

ABSTRACT:
A 0.5-to-3 GHz software-defined radio receiver leveraging Sampled Domain Signal Processing (SPSD) is demonstrated in a 65nm LP CMOS technology. The SDSP approach achieves band-pass filtering, harmonic rejection, and frequency translation simultaneously. Input impedance matching is achieved in an active translational loop that tracks the desired RF frequency. The chip includes a wideband frequency synthesizer, multi-phase non-overlapping clock generation circuitry, bandgap and power supply regulators. It achieves out-of-band IIP3 > 11.7 dBm, IIP2 > 58 dBm, NF = 5.5~8.8 dB, and uncalibrated 3rd and 5th order harmonic rejections exceeding 47 dB and 52 dB, respectively.

A 5–9-mW, 0.2–2.5-GHz CMOS Low-IF Receiver for Spectrum-Sensing Cognitive Radio Sensor Networks

AUTHORS:
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ABSTRACT:
A low-power, wideband CMOS receiver for spectrum-sensing cognitive radio sensor networks is presented. The low-IF receiver equipped with an inverter-based LNA-balun and I/Q sub-threshold rectifier enables low-power and high-speed spectrum sensing. For further extension to support higher data-rate radio systems, our local oscillator provides a frequency-dividing function when a low-phase-noise signal source is optionally used. A prototype chip fabricated in a 65-nm CMOS process can support a wide frequency range of 0.2–2.5 GHz with 43-dB maximum gain, 6-dB NF, and -9-dBm IIP3 and only occupies 0.6 mm^2 while consuming as low as 5–9 mW at a 0.6-V supply.

A 65nm CMOS High-IF Superheterodyne Receiver with a High-Q Complex BPF

AUTHORS:
Iman Madadi, Massoud Tohidian, Robert Bogdan Staszewski, *Technische Universiteit Delft, The Netherlands*

PAGE 323 – 326

ABSTRACT:
We propose a highly reconfigurable superheterodyne receiver that employs a 3rd-order complex IQ charge-sharing band-pass filter (BPF) for image rejection and 1st-order feedback based RF-BPF for channel selection filtering. The operating RF input frequency of the receiver is 500 MHz–1.2GHz with varying high-IF range of 33–80 MHz. All the gain stages are merely inverter-based g_m stages. The total gain of the receiver is 35 dB and in-band IIP3 at mid-gain is +10 dBm. The NF of the receiver is 6.7 dB, which is acceptable for the receiver without an LNA. The architecture is highly reconfigurable and follows the technology scaling. The RX occupies 0.47mm^2 of active area and consumes 24.5mA at 1.2V power supply.

A Multi-Path Multi-Rate CMOS Polar DPA for Wideband Multi-Standard RF Transmitters

AUTHORS:
Arnaud Werquin, Antoine Frappé, Andreas Kaiser, *IEMN, France*

PAGE 327 – 330

ABSTRACT:
A two-path digital power amplifier (DPA) in 1.2V 65nm CMOS is presented. This highly reconfigurable and frequency agile block is designed to be used as an envelope modulator in a wideband multi-standard polar transmitter. Each path is composed of a 12-bit DPA ensuring the modulation of the envelope of the RF signal. The DPAs are controlled by envelope code words (ECW) at different sample rates. This diversity strongly attenuates the images produced by the direct digital to RF conversion, avoiding passive filtering. The baseband sample rate conversion can easily be reconfigured. The proposed front-end can manage spurious emissions depending on the standard, the carrier frequency and the required power. The DPAs also integrate active input impedance compensation cells in order to limit the input impedance modulation when switching the DPA cells. The two-path DPA covers a 0.9–1.9 GHz bandwidth with 16.7dBm output 1dB compression point and 12.4% PAE. 64-QAM presents -28dB EVM while active area occupies $1 \times 0.25 mm^2$.

A Frequency-Agile RF Frontend for Multi-Band TDD Radios in 45nm SOI CMOS

AUTHORS:
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[1] *MIT, USA* ; [2] *MIT Lincoln Laboratory, USA*

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ABSTRACT:
A tunable and highly digital RF frontend for multi-band TDD radios is integrated in 45nm SOI CMOS. The PA absorbs the TX branch of the TX/RX switch with no added loss. Peak PA output power is 27.5±0.5dBm from 1.6 to 3.4GHz, with up to 30% total efficiency at 2V. For TDD LTE applications, better than -30dBc ACLR and -25dB EVM is measured with 16-QAM, 20MHz signals from 1.65 to 3.5GHz, with up to 16.5% average efficiency and 22.9dBm average power. The broadband LNA achieves $A_V > 14$dB, NF=4.3 ± 1.6dB and IIP3 > -7dBm from 1.6 to 3.4GHz while drawing just 6mA from 1V.

A Single Chip HBT Power Amplifier with Integrated Power Control

AUTHOR:
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PAGE 337 – 340

ABSTRACT:
The GSM power amplifier market continues to drive towards low cost and small size, but remains reluctant to compromise on performance. Current generation PA products utilize InGaP HBT to deliver RF performance and integrate bias and control on a supporting silicon die. This approach is common amongst many PA manufacturers with the exception of CMOS PA [1] solutions. This paper describes a solution using an HBT BiFET [2] technology to integrate both the precision control function and power amplifier onto a common die. The resulting solution opens opportunity for industry leading size and performance at no additional cost or RF performance penalty.

A Novel Load Insensitive RF Power Amplifier Using a Load Mismatch Detection and Curing Technique

AUTHORS:
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[1]Hanyang University, Korea ; [2]Avago Technologies, Korea

PAGE 341 – 344

ABSTRACT:
This paper proposes a new load insensitive RF power amplifier (PA) for mobile handsets using a load mismatch detection and curing technique. The PA controls a tunable output matching network (TOMN) adaptively based on the information of a mismatched load, thereby enhancing PA performances dramatically at a mismatched load without substantial performance degradation at a matched load. A load mismatch detector and TOMN can simply be implemented by using 0.18-μm silicon on insulator (SOI) FET that are integrated with 2-μm InGaP/GaAs HBT PA MMIC into a single module. To verify the idea, the PA module has been designed and implemented especially for a linearity enhancement under load mismatch condition. With WCDMA R'99 signal at 1.95 GHz, the measured results showed that ACLR at output power of 28.25 dBm was improved by as much as 13.7 dB on the worst ACLR-load angle compared to a conventional PA. In this way, the proposed load insensitive PA can keep ACLR under -37 dBc all over the load angle at 2.5:1 voltage standing wave ratio (VSWR).

A WLAN RF CMOS PA with Adaptive Power Cells

AUTHORS:
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ABSTRACT:
A CMOS linear PA for IEEE 802.11 b/g applications is implemented in a 0.13 μm process including all matching networks. An adaptive power cell (APC) scheme is proposed to achieve high linear output power and efficiency and applied to the PA, which delivers the output power of 20.5(19.5) dBm with the PAE of 20.2(17.5)% for an 802.11g modulated signal with the EVMs at -25(-28) dB.

A Ka-Band Doherty Power Amplifier with 25.1dBm Output Power, 38% Peak PAE and 27% Back-Off PAE

AUTHORS:
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ABSTRACT:
We present the design and development of the first fully integrated, two stage Doherty power amplifier (DPA) in the Ka-Band. The DPA is fabricated in a 0.15-μm GaAs pseudomorphic high electron mobility transistor (pHEMT) process. At 26.4 GHz, the amplifier achieves measured small signal gain of 10.3 dB, output power at 1-dB compression point (P_{1dB}) of 25.1 dBm, peak power added efficiency (PAE) of 38%, and PAE of 27% at 6 dB back-off power. To the best of the author's knowledge, this Doherty circuit is the first fully integrated millimeter-wave amplifier that achieves the highest power and a recorded 27% PAE at 6-dB back-off and each unit amplifier has 2 stages.

High Efficiency GaN Switching Converter IC with Bootstrap Driver for Envelope Tracking Applications

AUTHORS:
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ABSTRACT:
In this paper, we report a DC/DC converter based on GaN HEMT's with a switching frequency of 200 MHz that can be used to generate envelope-modulated power supply voltages for use in envelope tracking power amplifiers. The converter consists of switching circuits using 0.25-μm GaN HEMTs, inductor, and low pass filter, and can provide output voltages above 28V. An integrated bootstrap driver of the switching circuits is employed in order to reduce DC power consumption of the driver stage. Generation of envelope power supply voltages for 20 MHz LTE signals was demonstrated using 200 MHz switching rates with efficiency of 73% (including dissipation in final and driver stages). The chip size is 1075×990 um^2.

A 45GHz CMOS Transmitter SoC with Digitally-Assisted Power Amplifiers for 64QAM Efficiency Improvement

AUTHORS:
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ABSTRACT:
A 45GHz 64QAM system-on-chip (SoC) CMOS transmitter with digitally-assisted power amplifiers (DAPA) is presented. The SoC includes a 7M gate ASIC with 9b reconfigurable symbol mapping, 8X upsampling, 161tap pulse shape filtering, IQ imbalance correction and DAPA envelope/time estimation. The ASIC feeds two 10b IQ current-steering DACs and active IQ modulator. A unique transformer splitting up converter drives eight parallel combined DAPAs. The chip is packaged in aluminum housing with WR22 outputs. A 64QAM signal achieves 1.8% EVM with 33dBc ACPR at 45GHz. The data rate is 450Mbps and the integrated output power exceeds -10dBm.

A 163–180GHz 2×2 Amplifier-Doubler Array with Peak EIRP of +5dBm

AUTHORS:
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PAGE 363 – 366

ABSTRACT:
This paper presents a 2×2 amplifier-multiplier array with on-chip antennas at 163–180 GHz in 45 nm CMOS SOI technology. The measured EIRP is > 2 dBm at 165–175 GHz with a peak value of 5 dBm at 170 GHz meeting the stringiest metal-density rules for antennas. The amplifier-multiplier architecture is scalable to N×M arrays for high EIRP and transmit power.

A Self-Steering I/Q Receiver Array in 45-nm CMOS SOI

AUTHORS:
Arpit K. Gupta, James F. Buckwalter, *University of California at San Diego, USA*

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ABSTRACT:
A novel I/Q receiver array is demonstrated that adapts phase shifts in each receive channel to point a receive beam toward an incident RF signal. The measured array operates at 8.1 GHz and covers steering angles of +/-35 degrees for a four element array. Additionally, the receiver incorporates an I/Q down-converter and demodulates 64-QAM with EVM less than 4%. The chip is fabricated in 45 nm CMOS SOI process and occupies an area of 3.45mm^2 while consuming 143 mW dc power.

75–85GHz Flip-Chip Phased Array RFIC with Simultaneous 8-Transmit and 8-Receive Paths for Automotive Radar Applications

AUTHORS:
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PAGE 371 – 374

ABSTRACT:
This paper presents the first simultaneous 8-transmit and 8-receive paths 75–85 GHz phased array RFIC for FMCW automotive radars. The receive path has two separate I/Q mixers each connected to 4-element phased arrays for RF and digital beamforming. The chip also contains a build-in-self-test system (BIST) for the transmit and receive paths. Measurements on a flip-chip prototype show a gain >24 dB at 77 GHz, -25 dB coupling between adjacent channels in the transmit and receive paths (<-45 dB between non-adjacent channels), and <-50 dB coupling between the transmit and receive portions of the chip.

A Fully-Integrated Dual-Polarization 16-Element W-Band Phased-Array Transceiver in SiGe BiCMOS

AUTHORS:
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PAGE 375 – 378

ABSTRACT:
This paper presents a multi-function, dual-polarization phased array transceiver supporting both radar and communication applications at W-band. 32 receive elements and 16 transmit elements with dual outputs are integrated to support 16 dual polarized antennas in a package. The IC further includes two independent 16:1 combining networks, two receiver down-conversion chains, an up-conversion chain, a 40GHz PLL, an 80GHz frequency doubler, extensive digital control circuitry, and on-chip IF/LO combining/distribution circuitry to enable scalability to arrays at the board level. The fully-integrated transceiver is fabricated in the IBM SiGe BiCMOS 0.13μm process, occupies an area of 6.6$\times$6.7mm^2, and operates from 2.7V (analog/RF) and 1.5V (digital) supplies. Multiple operating modes are supported including the simultaneous reception of two polarizations with a 10GHz IF output, transmission in either polarization from an IF input, or single-polarization transmission/reception from/to I&Q base-band signals (2.5W RX, 2.9W TX). Measurement results show 8dB receiver NF and 2dBm transmitter output power per element at 94GHz in both polarizations.

A 130nm SiGe BiCMOS Technology for mm-Wave Applications Featuring HBT with f_T/f_{MAX} of 260/320GHz

AUTHORS:
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PAGE 381 – 384

ABSTRACT:
A manufacturable 130nm SiGe BiCMOS RF technology for high-performance mm-wave analog applications having a high-speed SiGe Heterojunction Bipolar Transistor (HBT) integrated into a full-featured RFCMOS is presented. The technology features a high performance (HP) SiGe HBT with f_T/f_{MAX} of 260/320 GHz, a high breakdown (HB) HBT with BV_{CEO} of 3.5V, 130nm RF CMOS, and a full suite of passive devices. Specific device results pertaining to this BiCMOS8XP technology are discussed in this paper.

Power Handling Capability of an SOI RF Switch

AUTHORS:
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PAGE 385 – 388

ABSTRACT:
In this study, we define and investigate the maximum power handling capability (Pmax) in an SOI RF shunt branch switch. One of the critical factor in the Pmax is the non-uniform voltage division across an OFF shunt branch. In this study we provide a simple analytical method to determine the stack voltage imbalance. The Pmax is characterized as a function of various parameters, such as, switch stack height, channel length, Gate and Body bias, and process parameters. Overall, we find that the Pmax can be improved by reducing stack imbalance as well as device leakage currents, namely, GIDL.

Nano Switching Crossbar Array ESD Protection Structures

AUTHORS:
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PAGE 389 – 392

ABSTRACT:
We report a new nano-switching ESD protection mechanism and dual-polarity $Cu/Si_xO_yN_z/W$ nano crossbar array ESD structures. Experiments show full ESD protection featuring fast response of 100pS, ultra low leakage of <2pA and ESD protection of >9A. New dispersed local ESD tunneling model and CMOS integration are reported.

Reconfigurable Sensors for Extraction of Dielectric Material and Liquid Properties

AUTHORS:
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[1] *NXP Semiconductors, France* ; [2] *Université de Toulouse, France*

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ABSTRACT:
This paper proposes an analysis and modeling of a reconfigurable sensor for the non-destructive remote extraction and monitoring of dielectric material and liquid properties, towards substance identification or distribution cartography.

A Sticking-Free and High-Quality Factor MEMS Variable Capacitor with Metal-Insulator-Metal Dots as Dielectric Layer

AUTHORS:
Fumihiko Nakazawa, Takeaki Shimanouchi, Takashi Katsuki, Osamu Toyoda, Satoshi Ueda, *ASET, Japan*

PAGE 397 – 400

ABSTRACT:
This paper describes a novel design of a MEMS variable capacitor with high operating reliability and high quality factor. Metal-Insulator-Metal (MIM) dots between a fixed electrode and a movable electrode in a variable capacitor is proposed. A Fabricated MEMS capacitor was operated one billion or more times without sticking. It demonstrated a high quality factor of 200 at 0.5 pF. It was experimentally confirmed that MIM dots effectively achieve a sticking-free and high-quality-factor MEMS variable capacitor.

A 71GHz RF Energy Harvesting Tag with 8% Efficiency for Wireless Temperature Sensors in 65nm CMOS

AUTHORS:
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Arthur van Roermund, Peter Baltus, *Technische Universiteit Eindhoven, The Netherlands*

PAGE 403 – 406

ABSTRACT:
This paper presents the first monolithically integrated RF-power harvesting 71 GHz wireless temperature sensor node in 65nm CMOS technology, containing a monopole antenna, a 71 GHz RF power harvesting unit with storage capacitor array, an End-of-Burst monitor, a temperature sensor and an ultra-low-power transmitter at 79 GHz. At 71 GHz, the RF to DC converter achieves a power conversion efficiency of 8% for 5 dBm input power.

A Compact Millimeter-Wave Energy Transmission System for Wireless Applications

AUTHORS:
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PAGE 407 – 410

ABSTRACT:
A compact energy transmission system in 40nm standard CMOS is presented. The system consists of a 60GHz VCO followed by a quad-core power amplifier as transmitter and an RF-to-DC converter as receiver. The total power delivered by the quad-core PA to its four 50Ω loads is 24.6dBm. The receiver is a complementary cross-coupled rectifier with a measured efficiency of 28% while supplying 1mA of current. The system can support amplitude and frequency modulations and beam-forming capabilities for wireless applications with minimal front-end complexities.

A 0.5GHz–1.5GHz Order Scalable Harmonic Rejection Mixer

AUTHORS:
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PAGE 411 – 414

ABSTRACT:
In this paper, a harmonic rejection mixer architecture capable of operating for a wide range of LO frequencies is demonstrated. The mixer can be configured to suppress any particular harmonic of the LO or multiple harmonics simultaneously. The level of suppression of each harmonic is controlled by a set of independent gain and phase tuning parameters. Feasibility of extension of this concept to higher order harmonics is also demonstrated.

A proof-of-principle prototype has been designed and fabricated in a 45nm SOI technology. Experimental results demonstrate an operation range of 0.5GHz to 1.5GHz for the LO frequency while offering harmonic rejection better than 55dB for the 3rd harmonic and 58dB for the 5th harmonic across LO frequencies. The mixer consumes 17mW of power from a 1V power supply while occupying an area of 0.352mm^2.

V-Band Dual-Conversion Down-Converter with Low-Doped N-Well Schottky Diode in 0.18μm CMOS Process

AUTHORS:
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[1] National Chiao Tung University, Taiwan ; [2] National Nano Device Laboratories, Taiwan ; [3] University of California at Los Angeles, USA

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ABSTRACT:
In this paper, a V-band dual-conversion down-converter with a silicon-based Schottky diode using low-doped N-well for DC and RF characteristics optimization is demonstrated in standard 0.18 μm CMOS technology. A triple-balanced subharmonic Schottky diode microwave mixer and a double-balanced resistive analog mixer are employed as the first conversion mixer and the second conversion mixer, respectively. As a result, the conversion gain is about -1 dB in the range of 45~64 GHz. The noise figure is about 20 dB, IP_{1dB} is about -5 dBm and IIP3 is about 5 dBm. The total power consumption is 92.4 mW at 2.5 V supply voltage.

A Fully Digital PWM-Based 1 to 3GHz Multistandard Transmitter in 40-nm CMOS

AUTHORS:
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PAGE 419 – 422

ABSTRACT:
A fully digital 1 to 3 GHz multimode transmitter is presented which contains two RF modulators: One uses baseband (BB) PWM, while the other uses RF PWM. RF PWM produces less harmonics, while BB PWM has a higher dynamic range (DR) and consumes less power. The BB PWM system satisfies the WLAN EVM limit over the whole frequency range. The RF PWM system achieves sufficient EVM for standards such as EDGE and WCDMA. Both systems support the use of multiple PAs to extend the DR using multilevel PWM.

An UWB CMOS Impulse Radar

AUTHORS:
Chenliang Du, Hossein Hashemi, *University of Southern California, USA*

PAGE 423 – 426

ABSTRACT:
This paper presents an integrated UWB short-range impulse radar implemented in a 130 nm CMOS process. The transmitter can digitally generate various waveforms with up to 10 GHz bandwidth at 5 dBm peak power. The receiver utilizes a time interleaved scheme to support a 20 GS/s effective sampling rate. Sample-domain averaging of multiple identical received waveforms reduces the required digitization rate and corresponding power consumption. Sampling clocks for the time interleaved samplers are generated using independent delay locked loops that are locked to the same reference. Measurement results of the individual blocks as well as the entire system are presented.

Simultaneous Linearity and Efficiency Enhancement of a Digitally-Assisted GaN Power Amplifier for 64-QAM

AUTHORS:
Monte Watanabe, Rob Snyder, Tim LaRocca, *Northrop Grumman, USA*

PAGE 427 – 430

ABSTRACT:
The first dynamic 4-bit, digitally-assisted GaN high power amplifier (DAPA) system transmitting 7.68-Msymbol/s with 64-QAM modulation is presented. An FPGA is programmed to generate the pulse-shaped 64-QAM signal, perform envelope estimation, and time-align the RF and digital control signals arriving at the DAPA. A high-speed, level-shifting circuit converts the FPGA's low-voltage differential signaling (LVDS) DAPA control signals into single-ended logic levels required for the depletion-mode GaN HEMT DAPA auxiliary cells. Measured results show 9.6% DC power savings, 23% improved PAE, and 23% higher output power at 4% EVM_{RMS} compared to the static PA configuration.

A Low-Noise FBAR-CMOS Frequency/Phase Discriminator for Phase Noise Measurement and Cancellation

AUTHORS:
Alireza Imani, Hossein Hashemi, *University of Southern California, USA*

PAGE 431 – 434

ABSTRACT:
A sensitive low-noise frequency/phase discriminator and its applications in phase noise measurement and phase noise cancellation are presented. The discriminator uses a high quality factor thin Film Bulk Acoustic Resonator (FBAR) in a notch filter configuration with common-mode traps to reduce the low-frequency noise up-conversion. The performance of the notch filter, the discriminator transfer function, output noise, and phase noise floor are measured and compared with simulations. A feed-back feed-forward phase noise cancellation scheme is proposed based on the frequency/phase discriminator. Two chips were fabricated in 0.13 μm CMOS technology integrating the discriminator and the phase noise cancellation schemes, respectively. The 1.5 GHz discriminator shows phase noise floor of -128 dBc/Hz at 20 kHz, -142 dBc/Hz at 100 kHz, -162 dBc/Hz at 1 MHz and -166 dBc/Hz at 4 MHz, while consuming 26 mW of power. The measured phase noise of the feedback cancellation circuitry reaches the phase noise floor of the discriminator, verifying the proposed concepts.

A 36GHz/mW Single-Phase Prescaler Using Implication Logic in 0.13μm CMOS

AUTHORS:
Elkim Roa, Wu-Hsin Chen, Byunghoo Jung, *Purdue University, USA*

PAGE 435 – 438

ABSTRACT:
This paper presents a non-Boolean digital logic technique used in the design of a high-speed and low-power frequency prescaler. Maximum achievable frequency input of prescalers is limited by the number of devices connected in cascade to the high-speed signal path. In this work, a reduced number of devices is obtained in the prescaler by realizing implication logic operators with a single-phase digital-based flip-flop. The prescaler is implemented in 0.13μm CMOS with a 1.2V supply. A measured efficiency of 36GHz per mW is achieved which represents 3X power consumption reduction compared to prior art in the same technology node, and the highest efficiency reported.

A Sub-1mW 5.5-GHz PLL with Digitally-Calibrated ILFD and Linearized Varactor for Low Supply Voltage Operation

AUTHORS:
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PAGE 439 – 442

ABSTRACT:
This paper proposes an ultra-low-power 5.5-GHz PLL which employs a divide-by-4 injection-locked frequency divider (ILFD) and linearity-compensated varactor for low supply voltage operation. The digital calibration circuit is introduced to control the ILFD frequency automatically. The proposed varactor, which applies a forward-body-bias (FBB) technique, is employed for linear-frequency-tuning under the power supply of 0.5V.

The proposed PLL was fabricated in 65nm CMOS. With a 34.3-MHz reference, it shows a 1-MHz-offset phase noise of -106 dBc/Hz, a reference spur level lower than -65 dBc, and the total power consumption of 950 μW at 5.5 GHz.

Effect of Drift Region Resistance on Temperature Characteristics of RF Power LDMOS Transistors

AUTHORS:
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[1]*National Nano Device Laboratories, Taiwan* ; [2]*National Taipei University of Technology, Taiwan*

PAGE 443 – 446

ABSTRACT:
In this work, we investigated the effects of drift region resistance on the temperature behaviors of RF power LDMOS transistors. Devices with various implant doses in the drift region were fabricated. Owing to the quasi-saturation effect, the transconductances at high gate voltages are less dependent on the temperature for low-drift-dose device. In addition, the maximum oscillation frequency exhibits different temperature coefficients for devices with different drift doses. We derived an expression of unilateral power gain with 4^{th}-order frequency term, and found that the drift resistance has a large influence on the device temperature characteristics at high frequencies.

A -78dBm Sensitivity Super-Regenerative Receiver at 96GHz with Quench-Controlled Metamaterial Oscillator in 65nm CMOS

AUTHORS:
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PAGE 447 – 450

ABSTRACT:
One high-sensitivity CMOS super-regenerative receiver is demonstrated for 96GHz mm-wave imaging based on high-Q metamaterial oscillator. Compared to traditional LC-tank based oscillator, the metamaterial oscillator is developed by folded-differential transmission-line loaded complementary split-ring resonator (FDTL-CSRR). With formed sharp stop-band, standing-wave is established with high EM-energy storage at mm-wave region for high-Q oscillatory amplification. As such, one high-sensitivity 96 GHz super-regenerative receiver is realized in 65nm CMOS with measurement results of: -78 dBm sensitivity, 0.67 $fW/Hz^{0.5}$ NEP, 8.5 dB NF, 2.8mW power consumption and 0.014 mm^2 core area.

A T-DMB Mobile TV SoC Tuner with Compact Size, Low Power and BoM in 65nm CMOS

AUTHORS:
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[1] I&C Technology Inc., Korea ; [2] Qualcomm, Korea ; [3] Samsung, Korea

PAGE 451 – 454

ABSTRACT:
This paper presents a direct conversion Korean standard T-DMB SoC tuner using a 65nm low power CMOS technology with the best feature of size, power and BoM ever reported. A digital F/E enhanced function is implemented to reduce analog signal processing empowered by oversampled A/D converter, digital channel selection filter and lots of digital calibration blocks. And the designed LNA excludes all required inductors. Thus high voltage gain and low current consumption are achieved due to their high Q factor. A single-to-differential signaling down-conversion mixer is also announced which has well balanced output characteristic. A DC/DC converter is adopted as well for the further low power consuming. The tunable clock frequency scheme of DC/DC buck converter can prevent a degradation of sensitivity performances which is planed value to escape the channel center frequency. This reported SoC tuner consumes only 28mA at maximum gain mode. And -103.5dBm of sensitivity and 48dBc of N±1 adjacent-channel selectivity are achieved also with only 5 external LC components. This SoC occupies $2.5 \times 2.5 mm^2$ die and WLCSP chip size.

A Highly-Linear CMOS RF Programmable-Gain Driver Amplifier with a Digital-Step Differential Attenuator for RF Transmitters

AUTHORS:
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PAGE 455 – 458

ABSTRACT:
This paper presents a CMOS RF programmable-gain driver amplifier (RF PGDA) for wireless transmitters. Digital-step differential attenuators precede a programmable-gain amplifier in order to enhance the dynamic range and to save power consumption, especially at low gain region. The RF PGDA fabricated in 0.13-μm CMOS technology with a 1.2 V supply voltage achieves a dynamic range of 49 dB with a step error of less than 0.5 dB and highly-linearized output satisfying the WCDMA/LTE specifications.

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