# A 0.32nJ/bit Noncoherent UWB Impulse Radio Transceiver with Baseband Synchronization and a Fully Digital Transmitter

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***Abstract* — This paper presents a low-power noncoherent ultrawideband (UWB) impulse-radio (IR) transceiver operating at 5GHz in 0.13-$\mu$m CMOS. The super-regenerative amplifier (SRA) based energy-detection receiver utilizes early/late detection for a two-step baseband synchronization algorithm. A fully-digital transmitter generates a shaped output pulse of 1GHz 3-dB bandwidth. DLLs provide a PVT-tolerant time-step resolution of 1ns over the entire symbol period and regulate the pulse generator center frequency. Measured results show a receiver efficiency of 0.32nJ/bit at 20.8Mb/s and operation with inputs as low as −70dBm. The transmitter outputs −31dBm (0.88pJ/pulse at 1Mpulse/s) with a dynamic (energy) efficiency of 16pJ/pulse.**

***Index Terms* — UWB, UWB-IR, Hearing aid, Impulse-radio, SRA, Super-regenerative amplifier, synchronization, low-power, transceiver**

## I. Introduction and Motivation

Recent developments in personal area networks and biomedical devices have enabled the integration of short range communication into low cost personal health care solutions. A target application where such integration proves beneficial is wireless hearing aids. Wireless hearing aids with integrated transceivers can serve multiple radio links such as ear-to-ear, ear-to-consumer device, and between the ear and a distant base station [1]. A small form factor coupled with low power and low cost is essential for an integrated solution. The FCC UWB standard allows a maximum of -41.3dBm/MHz power spectral density [2] which makes it an extremely viable choice for such transceivers. Transceivers for wireless hearing aid have been implemented using either a narrowband [3] or using carrier based UWB [1]. In this work we present a carrierless UWB-IR based transceiver for wireless hearing aid applications.

A carrier based transceiver scheme requires mixers and frequency synthesizers to frequency translate the signals. Auto-correlation techniques for reception can eliminate the frequency synthesizers but the mixers remain. These increase the area and power consumption of the implementations. A carrierless UWB-IR scheme allows for transmission of data in bursts (energy impulses) giving the circuit adequate sleep time during transmissions, hence lowering the power consumption and increasing the battery life. UWB-IR systems are time-based, i.e. detect sequences in time, hence timing synchronization between Tx and Rx is critical for demodulation.

The rest of the paper is organized as follows. Section II discusses the proposed transceiver architecture. Section III focuses on circuit implementation details. Section IV discusses testing and measurement results followed by conclusions.

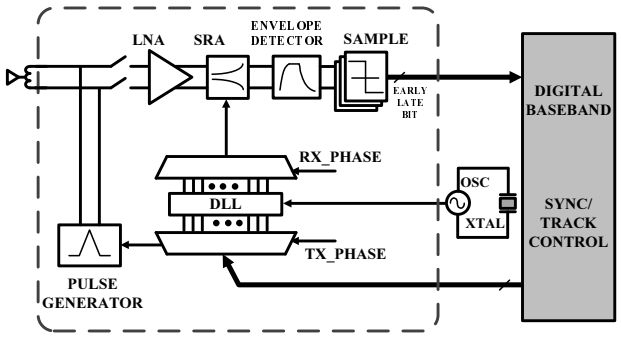


Fig. 1. Noncoherent UWB-IR Transceiver Architecture

## II. Transceiver Architecture

The block diagram for the proposed UWB-IR based transceiver is shown in Fig. 1. The system is designed for a 100Ω differential antenna and contains a pulse-generation based transmitter, a receiver supporting phase and frequency synchronization, a digital baseband, and a synchronization and tracking control block. A DLL provides a PVT tolerant time step resolution of 1ns and regulates the pulse generator center frequency. The antenna is shared between transmit and receive. The transmit output is always connected because it is in high impedance state when not transmitting. A switch is used to connect the receiver to the antenna while receiving. The following subsections discuss the transmit, receive and synchronization architecture in detail.

### *A. Transmitter*

A fully digital carrier less transmitter consisting of a pulse generator (PG) is proposed as shown in Fig. 2. The PG implements a piece-wise linear approximation of the an FCC [2] compliant pulse shape. This allows for a simple implementation leading to the omission of high-order on-chip bandpass filter, hence saving chip real estate and cost.

### *B. Receiver*

The receiver has an on-chip transformer preceding the LNA, which is followed by a super-regenerative amplifier (SRA), envelope detector, sample-and-holds, and a bank of comparators as shown in Fig. 3.

The energy detection based receiver determines the presence of a pulse by the amount of energy captured within a specific period, which we call the pulse detection window (PDW). The on-chip transformer is used for LNA input matching and filtering. The LNA amplifies the signal from the antenna, while presenting matched impedance to the input. The SRA provides an energy efficient way

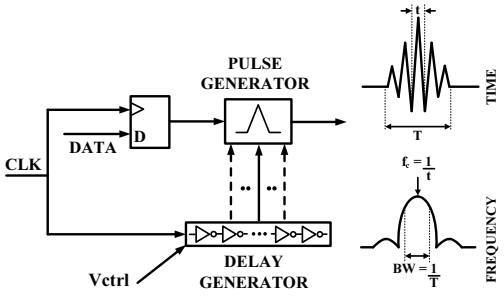


Fig. 2. Transmitter block diagram

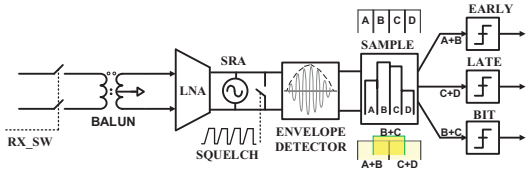


Fig. 3. Receiver block diagram

of signal detection. If a signal is present within the the PDW the SRA oscillates and the oscillation is detected by an envelope detector. A sample-and-hold allows the integration of the envelope detector's output within the PDW. Comparators then give digital outputs.

### C. Synchronization

For synchronization four fully programmable[1], equal sized, PDWs are used to locate and capture the data. Four windows A, B, C and D are combined using the logic shown in Fig. 3to generate the early, bit and late signals. The data is located by traversing the entire clock period through PDW resizing and delaying/advancing the entire windowing sequence in steps of 1ns, obtained using the DLL. A larger PDW leads to higher power dissipation in the receiver whereas a smaller window might result in erroneous detection due to incomplete SRA startup. An optimal PDW is decided by the signal energy level and the adjustable SRA bias current. Fig. 8 shows the width control on PDWs, with full power SRA to ensure startup.

## III. Circuit Details

The receiver is shown in Fig. 4. An on-chip transformer interfaces the differential input to the LNA serving the dual purpose of filtering and transforming the 100Ω differential antenna impedance to a 150Ω differential LNA input impedance. Series switches isolate the transformer and the receiver from the output path to minimize transmitter loading and LNA input saturation. The transmitter is shown in Fig. 5. The transmitter, receiver and the synchronization blocks are described next.

### A. Transmitter

*1) DLL:* The timing generation block is driven by a low power crystal oscillator with precise frequency control. It performs fine-phase control of timing signals used by transceiver blocks. The delay-locked loop (DLL) consists of a voltage-controlled delay line (VCDL), a phase

[1]Duration between PDWs and their width independently adjustable

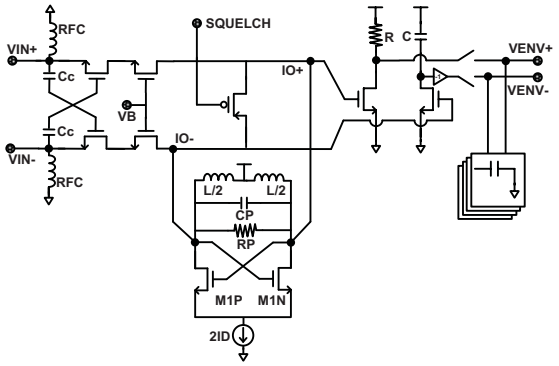


Fig. 4. Receiver front-end schematic

detector (PD), and a charge-pump (CP). The clock phases are selected by selecting signals from within the VCDL using a multiplexer. The phases of these signals are equally spaced within the total delay of the complete VCDL. The output clock is used as the timing reference for the pulse generator during transmission (another DLL in the receiver is used to control PDW). The resolution of the DLL in the transmitter is 100ps (and the receiver is 1ns). Since only nano-second timing accuracy is important, jitter is not a big concern in a non-coherent energy detection receiver.

*2) Pulse Generator:* The pulse generator uses static digital CMOS logic elements limiting power consumption to pulse transitions. A piecewise linear approximation of the desired pulse is generated by clock timing (to switch between up and down directions) and driver weighting (to change the charging/discharging strength) as shown in Fig. 5. A differential implementation is used to have more control of the output waveform. The output can be placed in a high-impedance state, removing the need for a T/R switch during reception. Timing is generated from the DLL to accomodate PVT.

### B. Receiver

*1) LNA:* A gain-boosted common-gate LNA [4] provides a wideband match and directly stimulates the SRA's inductive tank. The LNA gain is limited due to the high input impedance selected for lower power in combination with the de-Q'ing of the SRA's tank for wideband sensitivity. Cascoding provides isolation from signal leakage back towards the antenna.

*2) SRA:* The SRA consists of a cross-coupled NMOS pair, a de-Q'ed inductor tank, and a tank-shorting squelch switch. A squelch generation circuit controls the switch to form distinct time windows where the receiver is sensitive. The startup time of the SRA is influenced by the received signal energy during the operating windows. The oscillation is then quenched so that another detection interval can begin. The process is shown as an inset in Fig. 3. The receiver schematics are shown in Fig. 4.

*3) Receiver Backend:* A bank of four sample-and-holds record the envelope detector output at the end of each squelch window. The four sample-and-held values are averaged onto a capacitor to provide a running threshold voltage for comparing with the center two windows to determine if the a bit was received. Clocked comparators

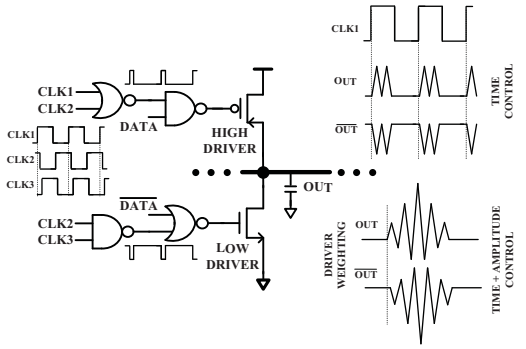


Fig. 5. Pulse generator timing, schematic, and output waveform

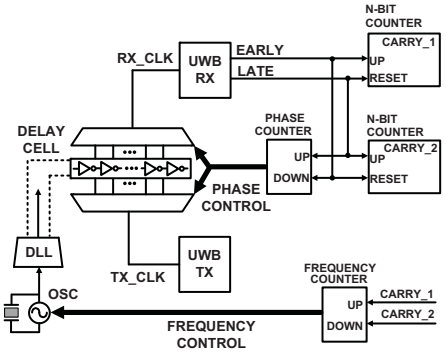


Fig. 6. Synchronization algorithm diagram

are used to generate early, late, and bit digital baseband indicator outputs.

### C. Synchronization Algorithm

The necessary clock frequency and phase adjustments can be controlled by a digital synchronization control using counters as shown in Fig. 6. Synchronization is achieved using the early/late impulse detection timing queues from the receiver. The phase is adjusted by selecting a different tap of the multiplexer. The N-bit counters are used for phase control unless they overflow in which case frequency control is initiated through the frequency counter. Frequency corrections are made every 2N consecutive early/late signals, taking care of the progressive phase mismatch. Tracking capability is acheived since early/late data continues through signal reception.

## IV. Measurements

The prototype design was implemented in IBM's $0.13\mu$m CMOS process. The chip occupies an active area of $0.67\text{mm}^2$ including probe pads. The chip micrograph is shown in Fig. 7.

To test the transmitter, an external clock of 50kHz is provided to the DLL. The data rate is set to 1Mb/s. The transmitter output pulse was captured using a 12GHz oscilloscope (Agilent DSO81204A) as shown in Fig. 9. Fig. 10, shows the measured output spectrum of the pulse. The expected output with modeled off-chip antenna response and matching network (including package bond wires) is also shown. It can be seen that the pulse is FCC compliant, centered at 5GHz, and has a 3dB bandwidth of 1GHz.

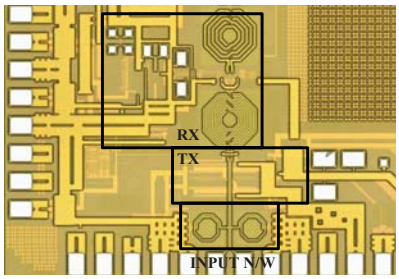


Fig. 7. Die photo

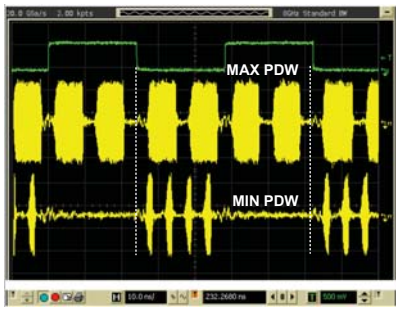


Fig. 8. Superimposed plot of forced SRA startup showing 4 consecutives windows of maximum and minimum size

In this prototype testing, the transmitter and the receiver were tested separately. In order to test the receiver, the transmitted pulse waveform is captured and used as an input data file to an arbitrary waveform generator (Tektronix AWG-7122C). The AWG is used to create pulse patterns, including modulation and phase shifts, for receiver testing. Receiver operation was evaluated over an input range of $-30$dBm (full power TX output) to approximately $-70$dBm using attenuators. Internal SRA operation was observed using a high-impedance probe. Receiver baseband digital outputs were monitored using a mixed-signal oscilloscope (Aglient MSO7104B). The receiver phase synchronization timing selection was performed manually depending on the test case and AWG waveforms.

Fig. 11 shows the demodulated output (red waveform) for an OOK input (green waveform). The figure also shows the modulated input pulse stream that was generated using the AWG (violet waveform). A repetitive (10110) pulse stream is used for this purpose. The corresponding SRA output is shown in yellow. The bottom part of the figure shows the demodulated output over a longer time period. The input power is set to -30dBm for this measurement. To measure the receiver sensitivity, the same test is performed again using a -70dBm input signal with successful demodulation.

An algorithmic implementation of the synchronization procedure is performed manually as shown in Fig. 12. In absence of synchronization, none of the PDWs show SRA oscillations. Using the DLL control, the data was located by traversing through the clock period by changing the phase of the receiver clock. In the first step, a strong startup is obtained in the fourth PDW (Late), indicating of lagging receiver clock with respect to data. Hence, in the subsequent steps the clock phase is advanced to align data to the central PDWs (PDWs 2 and 3) by moving 1ns in

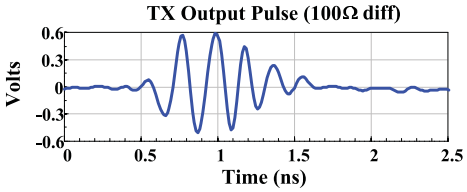


Fig. 9. Measured transmitter pulse through package and PCB

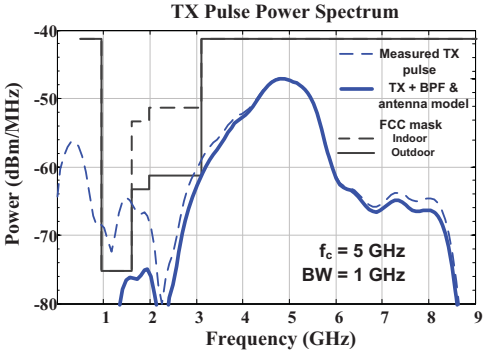


Fig. 10. Measured transmitter output spectrum including antenna and matching network model with FCC mask

each step. After alignment, a very strong startup is obtained in the second PDW (bit). The proposed synchronization algorithm lends itself well to automation and has been verified manually (Fig. 12).

Transceiver performance, as well as comparison with prior art, is summarized in Table I. As compared to [5] [6] (fabricated in lower technology nodes) we acheive comparable RX FOM with higher data rate and better TX power. While [7] has better sensitivity, the design is not fully integrated and has a higher RX FOM.

## V. Conclusions

This paper presents a carrier-less UWB-IR based transceiver for wireless hearing aid applications. The SRA based energy-detection receiver utilizes early/late detection for a two-step baseband synchronization. Simple digital circuits are used to implement the baseband blocks. The

TABLE I
Comparison with other UWB-IR designs

| | | **This work** | [5] | [6] | [7] |
|---|---|---|---|---|---|
| Modulation | | OOK | OOK | OOK | PPM |
| Synchonization | | **Yes** | **Yes** | **Yes** | No |
| Technology | nm | 130 | 65 | 90 | 90 |
| **RECEIVER** | | | | | |
| PRF | MHz | **20.8** | 2 | 0.15 | 16.7 |
| Power | mW | 6.6 | 0.75 | 0.052 | 35.8 |
| RX FOM | nJ/bit | **0.32** | 0.375 | 0.4 | 2.5* |
| Sensitivity | dBm | $\approx -70$ | $-76.5$ | $-86$ | $-99$* |
| **TRANSMITTER** | | | | | |
| Output Swing | $V_{pp}$ | **1.1** | – | 0.6 | – |
| Active Energy | pJ/bit | **16**† | – | 59 | – |

* 0.85nJ/bit at 0.5V with $-84$dBm sensitivity
† Dynamic power at 1Mpulses/s

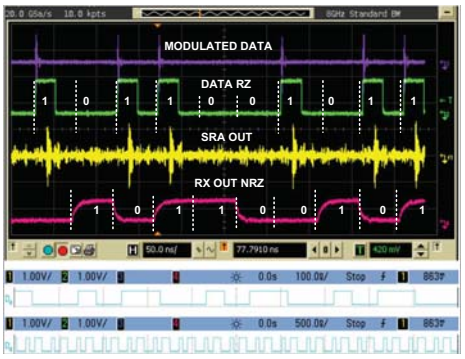


Fig. 11. Measurement of OOK input pulses and data, followed by synchronized SRA response and received data

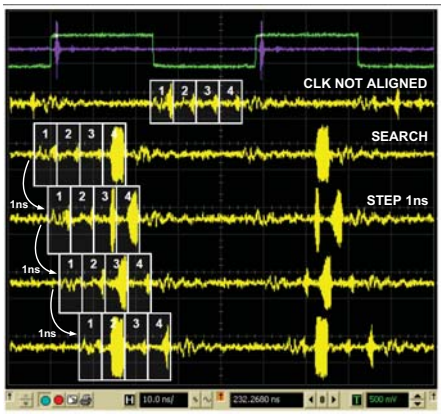


Fig. 12. Synchronization algorithm (with manual control)

fully-digital transmitter generates a shaped output pulse of 1GHz 3-dB bandwidth. Measured results show a receiver efficiency of 0.32nJ/bit at 20.8Mb/s and operation with inputs as low as $-70$dBm. The transmitter outputs $-31$dBm (0.88pJ/pulse at 1Mpulse/s) with a dynamic (energy) efficiency of 16pJ/pulse. A constant time step resolution of 1ns in the face of PVT variations is achieved.

## VI. Acknowledgments

We thank Integrand Software, Inc. for use of EMX®.

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