An UWB CMOS Impulse Radar

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***Abstract*—This paper presents an integrated UWB short-range impulse radar implemented in a 130 nm CMOS process. The transmitter can digitally generate various waveforms with up to 10 GHz bandwidth at 5 dBm peak power. The receiver utilizes a time interleaved scheme to support a 20 GS/s effective sampling rate. Sample-domain averaging of multiple identical received waveforms reduces the required digitization rate and corresponding power consumption. Sampling clocks for the time interleaved samplers are generated using independent delay locked loops that are locked to the same reference. Measurement results of the individual blocks as well as the entire system are presented.**

***Index Terms*—UWB, radar, time-interleaved sampling, delay locked loop.**

I. Introduction

Due to the depth resolution and the penetration capability, an Ultra Wide-Band (UWB) impulse radar provides a promising solution for several non line-of-sight sensing applications, including non-contact vital sign detection and through-the-wall imaging [3]. CMOS implementation enables further integration of the radar front-end with Digital Signal Processing (DSP) circuitry that can run various radar detection algorithms.

The optimum detector in any communication or radar system is a matched filter. Also known as a correlator, the matched filter can be realized in the analog or digital domain. In virtually all narrowband systems, the matched filter is realized in the digital domain due to the flexibility and scaling advantages of digital processors. In wideband and UWB systems, analog matched filters or correlators are often used due to the large power consumption of Analog-to-Digital Converters (ADC) and high-speed digital processors [4]. In a radar, the received waveform can vary considerably from the transmit waveform due to the effect of antennas and the reflecting objects. Therefore, the optimum template waveform, needed in the matched filter or correlator, is not necessarily known in advance of even fixed. Generating arbitrary UWB template waveforms and performing analog correlation requires power-hungry Direct Digital Synthesizers (DDS). In radars, in order to increase the Signal-to-Noise Ratio (SNR), oftentimes, the same waveform is transmitted multiple times to enable coherent addition at the receiver [5]. So long as the environment and reflecting objects remain stationary within the time that multiple waveforms are transmitted, all received waveforms are identical and can be added coherently. The "information rate" after the coherent addition of received waveforms is considerably reduced compared with the raw received waveform. This observation leads to an alternative radar architecture with lower power consumption where coherent addition of multiple received waveforms is done in the (analog) sampled domain prior to digitization [2]. The scheme recovers the exact received waveform, hence, enabling flexible and dynamic correlation schemes in the digital domain.

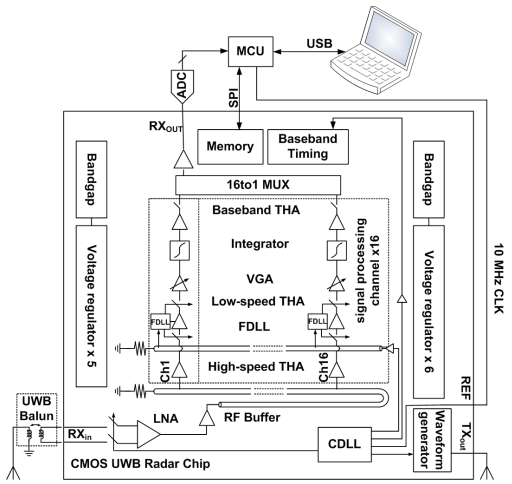

Fig. 1. Radar architecture block diagram.

In this paper, a completely new radar transceiver following the general scheme of [2] is presented. The main advantages of this scheme over [2] are (1) transmission-line based UWB received signal distribution to multiple time-interleaved samplers, (2) independent sampling clock generators for the time-interleaved samplers, (3) on-chip analog DC offset-cancellation blocks, (4) Power-Voltage-Supply (PVT) independent biasing, low-noise regulators, and Electro-Static Discharge (ESD) protection circuitry for all RF/Digital pads, and (5) standard Serial Peripheral Interface (SPI).

The paper structure is as follows. Section II covers the radar specifications and the transceiver architecture. Section III shows the key circuit building blocks and their corresponding performances. Section IV presents the measurement results, and Section V concludes the paper.

Parameter	Specification
Maximum range, R	15 m
Depth resolution, ΔR	1 cm
Reflector effective back-scattered cross-section, σ_{bs}	0.5x0.5 m^2
Effective receiving antenna area, A_e	3.5x3.5 cm^2
Transmitting antenna gain, A_G	1.5
Maximum transmitted power per pulse, P_{TX}	10 dBm
Input-referred noise bandwidth, BW	10 GHz
Required SNR at radar output	20 dB

TABLE I
REPRESENTATIVE
RADAR SPECIFICATIONS

Parameter	Specification
Transmitter	
Pulse repetition frequency, PRF	10 MHz
Maximum transmitted power per pulse, P_{TX}	10 dBm
Maximum transmitted pulse bandwidth, BW_{TX}	5 GHz
Receiver	
Equivalent sampling rate, f_s	20 GSa/s
Noise figure, NF	7 dB
Maximum DC offset at receiver output	0.4 V
Timing Circuitry	
Coarse range bin size, R_{CRB}	12 cm
Number of pulse averages	10^2-10^5

TABLE II
REPRESENTATIVE
CIRCUIT
SPECIFICATIONS

II. RADAR SPECIFICATIONS AND ARCHITECTURE

The envisioned chip-scaled radar should be flexible enough to cover a variety of indoor and outdoor applications. The probability of detection, directly related to received SNR, can be extracted from the radar equation [5]. Table I shows one example of the specifications that can be met with the presented chip-scaled radar having corresponding settings of Table II. The peak transmit power is set to be compliant with the FCC standard. The Pulse Repetition Frequency (PRF), number of averaged waveforms (in the receiver), and the transmit waveform bandwidth are all programmable.

The complete radar consists of an UWB CMOS transceiver, low-frequency ADC, a Micro-Controller Unit (MCU), and a pair of UWB transmit/receive antennas (Fig. 1). The chip can be interfaced with a PC or an FGPA through the MCU. The UWB CMOS transceiver includes a digital UWB waveform generator for the transmitter, a 16-time-interleaved UWB receiver, and a T/R switch. The received waveform is amplified in a noise-cancelling UWB differential Low Noise Amplifier (LNA). One key challenge in time-interleaved architectures is the realization of a low-power input signal distribution to all the interleaved paths. Specifically, driving a large aggregate capacitance, while maintaining the bandwidth requirement, often leads to power hungry driving buffers. In this implementation, the received and amplified waveform is fed to the time interleaved channels through a quasi-distributed transmission line that is periodically loaded with the input capacitance of each channel. Similar to the distributed amplifier concept, this leads to lower power consumption for the same bandwidth and gain. Each of the 16 time-interleaved channels consists of a high-speed Track-and-Hold Amplifier (THA) driven by a localized clock generated in a 16-cell Fine Delay Locked Loop (FDLL), a low-speed THA, a Variable Gain Amplifier (VGA), an Integrator, and a baseband THA. The sampling instant and the gain of each channel can be independently set through the corresponding FDLL and VGA. This flexibility enables correction capability for mismatches in the signal or clock paths. The delay resolution of the FDLL is 50 ps corresponding to 20 GS/s effective sampling rate. One key feature of this architecture is sample-domain received signal integration prior to digitization. As mentioned before, this reduces the power consumption of the baseband ADC, while preserving the exact shape of the received waveform (time stretched).

The fine DLLs are all locked to a single reference generated in a coarse DLL (CDLL) whose job is to set a specific range bin by compensating for the round-trip delay between the radar and the intended target. The delay resolution of the 128-cell CDLL is 780 ps corresponding to 11.72 cm range bin. The reference signal for the CDLL is set by a signal generated in the MCU - the PRF is set by this signal.

The chip runs from a single 2.5 V supply, and includes several 2.5 V - 1.5 V voltage regulators to separate the supply of aggressor (*e.g.*, clock) and victim (*e.g.*, LNA) blocks, and to ease the power distribution. All pads include ESD protection and clamp circuitries. The chip can be programmed through an SPI with an 184-byte on-chip memory map. The entire receive path is differential - an off-chip balun is used to interface with a single-ended antenna. The transmitter is single-ended. In addition to the gain and timing settings, all bias currents throughout the radar transceiver chip are programmable via the SPI interface.

III. CIRCUIT BLOCKS

A. Receiver front-end

The receiver differential pad is interfaced with the LNA through an UWB switch to isolate the receiver from the strong signal that is directly coupled from the transmit to the receive antenna. This switch must turn on/off within a few nanoseconds so that the nearby reflections are not missed. Spiral inductors used before and after the switch enhance the bandwidth. The differential LNA is a regulated cascode with noise cancellation (Fig. 2) with a simulated gain of 15 dB, Noise Figure (NF) of 7 dB, and -3dB bandwidth of 0.1-6.5 GHz. An open-drain differential pair follows the LNA and drives an on-chip quasi-distributed transmission line. The transmission lines is a differential micro-strip that is periodically loaded with the time-interleaved high-speed samplers. The 30 fF differential input capacitance of each high-speed sampler combined with the equivalent $L = 80\ pH$ and $C = 30\ fF$ of the micro-strip sections determine the characteristic impedance to be 37 Ω and cut-off frequency to be 72 GHz in differential mode. The high-speed THAs (Fig. 3)

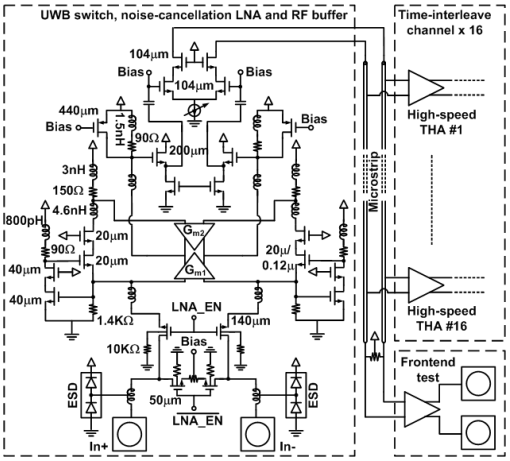

Fig. 2. Receiver frontend schematic. All transistors have minimum channel length

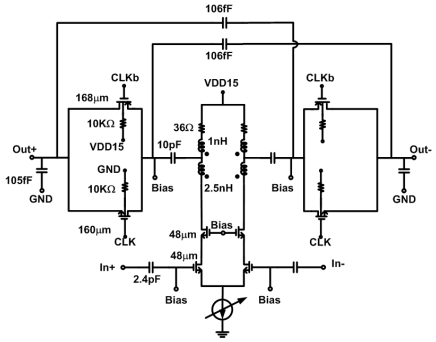

Fig. 3. High-speed THA schematic. All transistors have minimum channel length

are differential pairs with transformer-based T-coil shunt peaking at their outputs.

B. Receiver back-end

Receiver back-band (Fig. 4) consists of 16 channels, performing gain control and averaging for the output of each high-speed THAs. The sampled signal by the THA is fed to a VGA through a slow THA (note the sampled signal after the high-speed THA is slow). The VGA consists of two resistive feedback op-amp stages preceded and followed by passive mixers for chopper DC cancellation. The VGA gain range covers 0 to 40 dB in 1.5 dB steps enabling received signal strength control as well as channel-to-channel gain mismatch compensation. A following integrator is an active RC structure with internal offset cancellation circuitry. Integration time is digitally programmable. The output of 16 channels, now low-frequency (DC) signals, are interfaced with outside through a 16-1 analog multiplexer.

C. Timing circuitry

The time-interleaved clock generation and distribution scheme is shown in Fig. 5: all 16 fine DLLs, physically laid

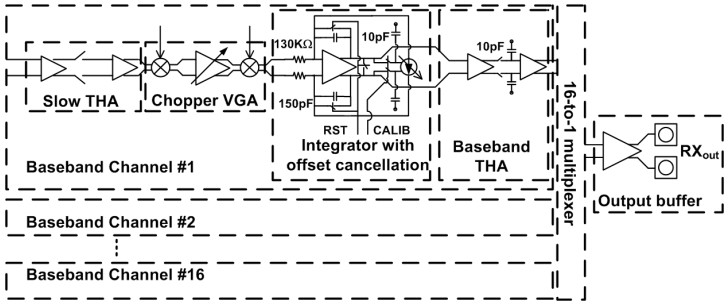

Fig. 4. Receiver back-band schematic.

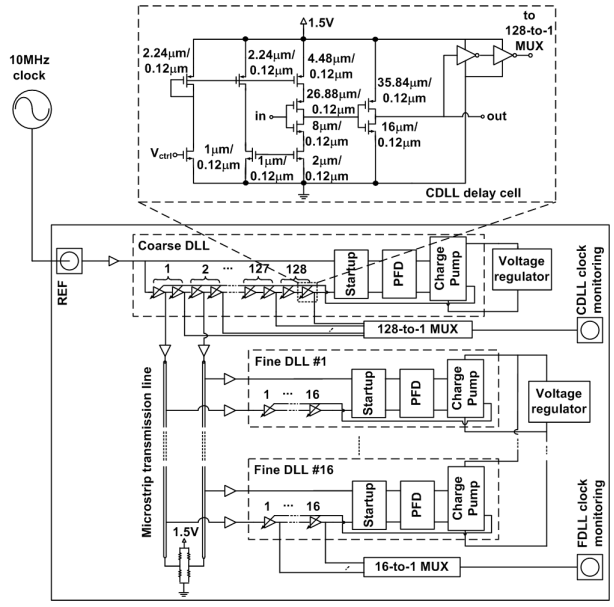

Fig. 5. Timing circuitry signal generation and distribution.

out close to the corresponding time-interleaved channel, lock to the coarse DLL and independently generate 16 clock phases between the first and second phases of coarse DLL. The two references to each fine DLL are distributed by two transmission lines terminated to their characteristic impedance. The electrical length of these transmission lines mimics that of the RF signal distribution line to the time interleaved channels, so that the signal and sampling clock arrive almost simultaneously. Independent generation of sampling clocks for the time interleaved channels enables correcting for timing mismatches. Moreover, the power consumption of DLLs, mostly digital circuitry, reduces with technology scaling.

D. Transmitter

The transmitter creates UWB waveforms similar to the scheme reported in [2], and it triggered by the timing circuitry fed from the CDLL.

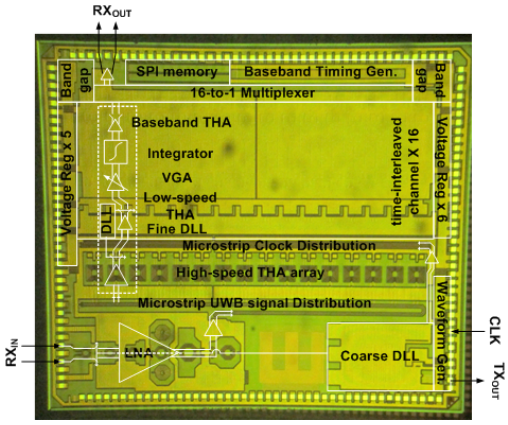

Fig. 6. Chip die photo.

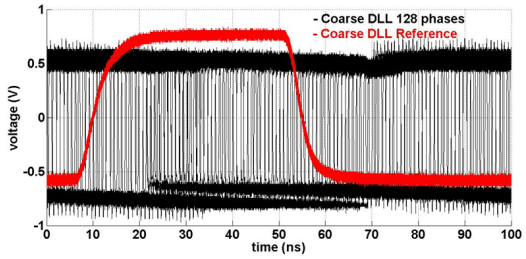

Fig. 7. Measured coarse DLL 128 phases and coarse DLL reference.

IV. Measurement Results

The radar transceiver chip is implemented in the IBM 8RF-DM process (Fig. 6). The $4.4 \times 5.1\ mm^2$ chip is packaged in a 56-pin QFN and placed on a custom Printed Circuit Board (PCB) that includes the low-speed ADC, MCU, and other interface components. All reported measurements include the effects of package and board.

The measured signals from all the 128 cells of the coarse DLL and the 16 cells of the fine DLLs are shown in Fig. 7 and 8, respectively. From measurements, the rms delay variation over different cells of the coarse and fine DLL are $45\ ps$ and $7\ ps$, respectively. As mentioned before, a key advantage of localized generation of sampling clocks is the ability to correct for channel to channel mismatches.

In order to demonstrate the system functionality as a radar, loop-back measurements through a fixed length of external cable between the transmitter and receiver are conducted. The output waveforms for different integration times are shown in Fig. 9 demonstrating generation and detection of UWB waveforms.

V. Conclusion

A short-range chip-scaled UWB impulse radar is reported. Main features of the CMOS radar chip include direct sampling of the UWB waveform in a time-interleaved approach, sampled-domain received signal integration, local generation of sampling clock signals, and on-chip DC offset cancellation circuities. Measurement results demonstrate the functionality of the radar and presented concepts.

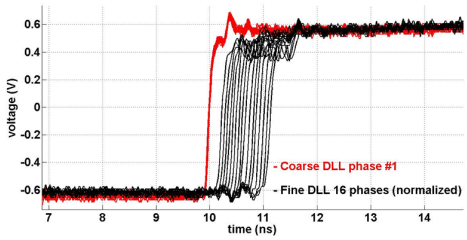

Fig. 8. Measured fine DLL 16 phases and fine DLL reference.

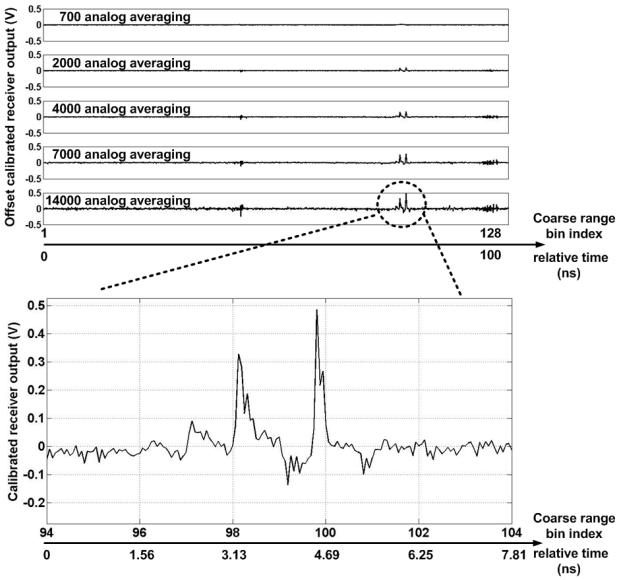

Fig. 9. Loopback measurement with different averaging setting.

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