A 2×13-bit All-Digital I/Q RF-DAC in 65-nm CMOS

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***Abstract* — This paper presents a 2×13-bit I/Q RF-DAC-based all-digital modulator realized in 65 nm CMOS. The proposed quadrature up-converter uses a 25% duty-cycle clock to isolate the in-phase (I) and quadrature-phase (Q) modulating signals before combining. Using a 1.2 V supply and an on-chip power combiner, the modulator provides more than 21 dBm RF output power within a frequency range of 1.36 to 2.51 GHz. The peak RF output power, overall system and drain energy efficiencies of the modulator are 22.3 dBm, 31.5%, and 39.7%, respectively. Applying digital predistortion (DPD), 64 & 256 constellation points are measured with EVM better than -30 dB. The measured noise floor is below -160 dBc/Hz, with an IQ image rejection and LO leakage of -65 and -63 dBc, respectively. Its linearity has been evaluated with WCDMA modulation. Using DPD, the linearity improves by more than 15 dB.**

I. Introduction

In recent years, intensive research has been directed towards digitizing RF transmitters. The modulator is the key building block of such transmitters and can be implemented as either polar [1] [2] or Cartesian (I/Q) [3]–[6] topology, with varying levels of digitization. For wider modulation bandwidths, due to their direct summation of the I and Q signals and the avoidance of bandwidth expansion, I/Q modulators prove to be a better choice than their polar counterparts [6]. An all-digital orthogonal I/Q modulator concept was first proposed in [6], where a 2×3-bit static I and Q implementation could reach a maximum RF output power of 12.6 dBm. The effective baseband code resolution is an important parameter for RF-DAC-based modulators, as it directly impacts the achievable dynamic range, linearity, error vector magnitude (EVM) and noise floor. In this work we demonstrate a new design of an all-digital 2×13-bit I/Q modulator that can provide output power beyond 20 dBm. Due to its high efficiency, bandwidth, functionality, and resolution, while requiring small chip area, the proposed solution is a very promising candidate for future multi-mode/multi-band transmitters.

II. RF Digital-to-Analog Converter

Fig. 1 shows the concept of the differential orthogonal digital I/Q modulator [6]. The digital in-phase (I_{BB}) and quadrature-phase (Q_{BB}) baseband signals are upsampled and interpolated to obtain high sampling-rate digital signals I_{BB-up} and Q_{BB-up}. This upsampling process ensures that the spectral images will be attenuated and located far away from the carrier such that they can be

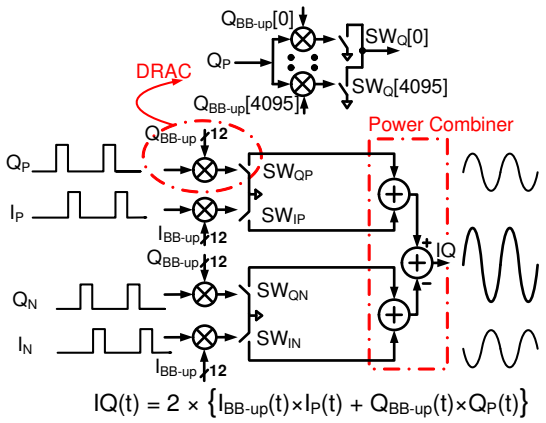

Fig. 1. The differential, orthogonal digital I/Q modulator model.

easily filtered out by circuit parasitics. Next, I_{BB-up} and Q_{BB-up} are applied to a pair of digital-to-RF-amplitude converters (DRACs), comprising implicit mixers and switch-array banks, which enable the direct conversion of the upsampled digital baseband signals to their continuous-time RF counterpart. Using a differential power combiner, the conversion of the upconverted digital signals into a "high power" RF output signal is done in an energy efficient manner. In fact, this approach represents an RF-DAC. The I/Q summation must be done orthogonally, otherwise EVM, bit-error rate and spectral regrowth will arise. To avoid this problem, quadrature differential clock signals (I_P, I_N, Q_P, Q_N) with a duty-cycle of 25% are used to guarantee isolation, thus avoiding any interaction between the in-phase and quadrature-phase paths. In addition, by swapping between I_P/I_N or Q_P/Q_N, the sign bits of the baseband data can be effectively changed and, therefore, the entire 4-quadrant constellation diagram can be covered.

III. Digital I/Q Modulator Design

Based on the digital I/Q concept above, a 2×13-bit all-digital I/Q modulator is implemented (see Fig. 2). The $4f_0$ single-ended off-chip clock, where f_0 is the carrier frequency, is applied to an on-chip balun to convert the single-ended clock to differential signals. The differential clock is applied to cascaded divide-by-two circuits to generate the desired carrier at f_0. In contrast to [6], the sign-bit circuit, implemented as a multiplexer with input control signals $I_{BB-up}[12]$ and $Q_{BB-up}[12]$, is now

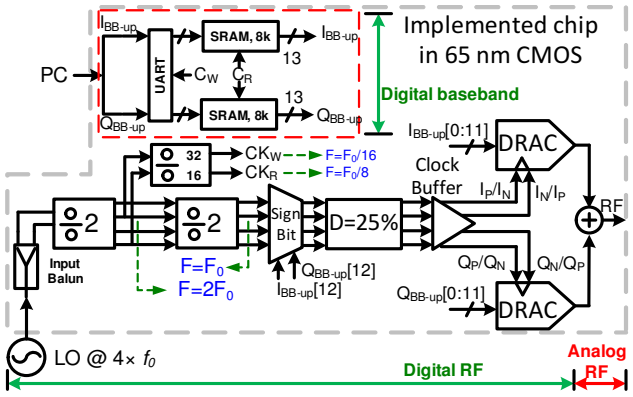

Fig. 2. Block diagram of the 2×13-bit all-digital I/Q modulator.

located between the second divider and the 25% duty-cycle generator to achieve faster rise and fall times. A simple logic AND operation is used to generate the 25% duty-cycle quadrature clocks [5]. As noted, the targeted modulator is a 2×13-bit RF-DAC whose upsampled I_{BB-up} and Q_{BB-up} inputs are binary coded. They must be converted to a thermometer code representation in order to avoid non-monotonic behavior and mid-code transition glitches. Use of a pure thermometer code, however, would increase the chip area, complexity of the encoders, and power consumption. Thus, a segmented approach is adopted. Based on extensive system level simulations, the segmentation is chosen such that 8 bits are used for the MSB and 4 bits for the LSB. Therefore, the DRAC implementation comprises 256 MSB and 16 LSB units. The design of such a complex RF-DAC requires several schematic and layout iterations. The 256 MSB units are further split into two sections, each with 128 MSB units. The main clock tree is placed in the middle, as shown in Fig. 3(a). Moreover, the 128 MSB units of each part are arranged in 8 rows and 16 columns (i.e., 8×16). The LSB part occupies only one row (1×16) at the bottom right of the matrix. Based on this arrangement, two 3-to-7 and three 4-to-15 binary-to-thermometer encoders are used in total.

The MSB DRAC unit is shown in Fig. 3(b). It consists of four equal, well-matched circuit sections, each with their own data and clock inputs. The quadrature differential input clocks are I_P, Q_P, I_N and Q_N, while the data input signals are R_I, C_I, R_Q, and C_Q. Each section has two parts: The pure digital logic part consists of decoding logic (AND-OR) and a flip-flop for timing synchronization. The digital-to-RF conversion part consists of a clocked cascode switch that yields the up-converting mixer operation. In addition, the use of a cascode transistor (M_2, M_4, M_6, M_8) alleviates the reliability issue related to the high voltage swing that appears on the output nodes ($Drain^+$, $Drain^-$). The use of the cascode configuration increases the output impedance and results in better isolation be-

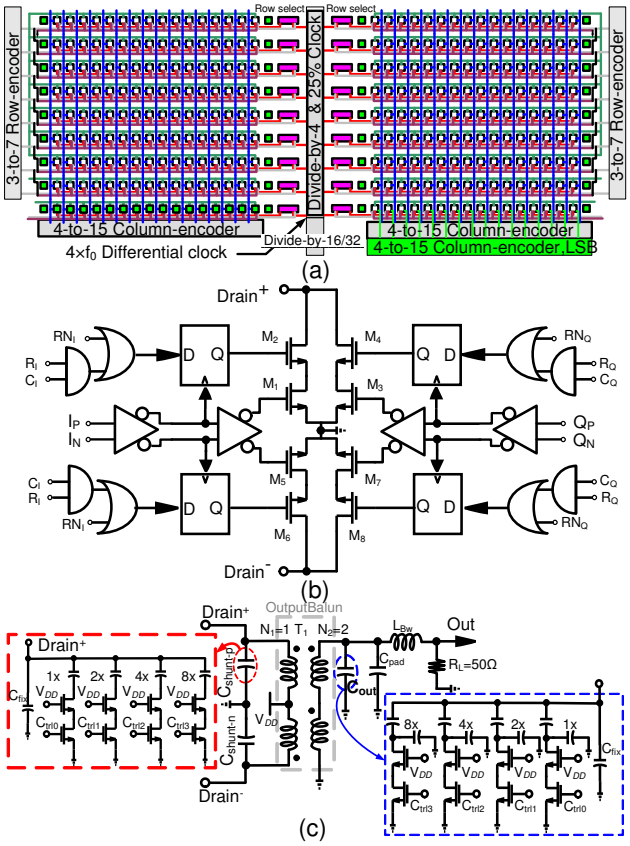

Fig. 3. (a) 2×12-bit DRAC floor plan, (b) DRAC unit cell, (c) power combining network.

tween the I and Q paths. The overall quadrature mixer is formed by electrically combining the outputs of two individual upconverter mixers that are driven by quadrature input clocks (the upside M_1–M_4 and downside M_5–M_8 upconverter mixer pairs in Fig. 3(b)). As a result, the entire RF-DAC is now created by simply connecting together the corresponding drain nodes of each DRAC unit cell.

The power combining network is an important part of the digital modulator as it determines its output power, efficiency, and quadrature accuracy. It consists of a balun (T_1), input shunt capacitors (C_{shunt}), and output capacitors (C_{out}) [6]. The balun de-couples the drain DC condition from the load and converts the differential signal to a single-ended output. Furthermore, the balun provides a DC bias path for the DRAC transistor switches and transforms the 50 Ω load to the desired impedance at the drain nodes of the DRAC. The targeted output power for this design is more than 22 dBm. Based on the design procedure in [6], the balun size is chosen to be 450×450 μm^2 with 1:2 turns ratio. The balun must handle high currents of up to 360 mA. To do so, it uses three parallel traces in the primary winding that are inter-digitated with the secondary winding to satisfy electromagnetic rules of the

technology [2]. The shunt input and output capacitances of the transformer balun are used to fine tune the amplitude and phase relationship of the I/Q modulator for the desired frequency. For this purpose, two 4-bit binary-weighted capacitor banks are added at the primary and secondary sides (Fig. 3(c)). Since the entire design is done using 1.2 V standard thin-oxide transistors, the voltage swings at the transformer connections are too high to be handled by a single transistor. Consequently, cascode switches are used. Moreover, the voltage swing at the secondary side can be as high as 4 V. Therefore, series-capacitors are incorporated to reduce the cascode drain node swing to at most 2 V (Fig. 3(c)).

IV. Measurement Results

The proposed 2×13-bit all-digital I/Q RF-DAC-based modulator is fabricated in 65 nm CMOS technology. Fig. 4 shows the chip micrograph. The total chip area is 1.27×2 mm^2 with the core of the digital I/Q modulator occupying 0.6×1 mm^2. All pads, including the RF input clock and RF output (both single-ended), are wire-bonded. For the measurements, the I_{BB-up} and Q_{BB-up} are loaded via a Universal Asynchronous Receiver/Transmitter (UART) into two SRAM memories, which are synchronized by CK_R, i.e., an on-chip clock operating at 1/8 of carrier frequency (see Fig. 2). The resulting sampling and synchronization operations represent a zero-order-hold (ZOH) that acts like a sinc-filter with its corresponding zeros located at multiples of CK_R. As such, the spectral images are notched by the ZOH operation. Experimental verification shows that, without using any correction for the PCB and SMA connector losses, the peak overall system efficiency ($\eta_{tot} = P_{RFout}/P_{DCtotal}$) occurs at 1.98 GHz and reaches 31.5% with the related output power and drain efficiency of 22.3 dBm and 39.7%, respectively.

Although the IQ modulator works properly from 60 MHz to 3.5 GHz, the best performance is achieved for operating frequencies in the range of 1.36 to 2.51 GHz, where measurements show an output power and overall system efficiency of more than 21 dBm and 21%, respectively (see Fig. 5). For this measurement, the carrier frequency is swept from 1.35 to 2.63 GHz in steps of 2 MHz. These results underscore the wide-band operation of the realized on-chip output balun.

The modulator phase noise is measured for various carrier frequencies between 1.5 to 2.5 GHz and the noise floor is found to be better than -160 dBc/Hz. Fig. 6(a) shows the modulator phase noise at the frequency of 2.4 GHz. As can be noted, at 60 MHz frequency offset, the phase noise is -158 dBc/Hz with an associated RF output power of 21.54 dBm. The figure also shows two "spurs" at 300 MHz and 600 MHz, which are actually the spectral replicas discussed earlier. Here the ZOH filter operation

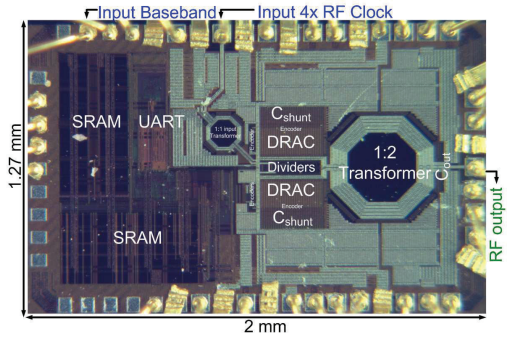

Fig. 4. Micrograph of the 2×13-bit all-digital I/Q RF-DAC.

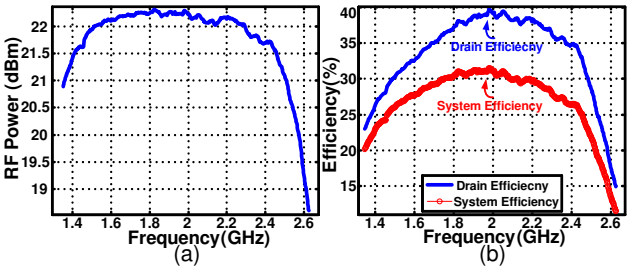

Fig. 5. (a) RF output power, (b) efficiency of digital modulator.

ensures that these spur levels are below -70 dBc. The I_{BB} and Q_{BB} input baseband codes are individually swept from code -4095 to +4095 and the output power with the related voltage/phase is captured (see Fig. 6(b) and Fig. 7(a)). As expected, at lower codes (center of the curve of Fig. 6(b)) the output voltage changes linearly with respect to the input code. In contrast, at higher codes the curve starts to saturate, which indicates the AM-AM compression. Moreover, based on Fig. 7(a), changing I_{BB} or Q_{BB} alone, not only changes the amplitude but also the output phase, which reveals the AM-PM nonlinearity of the RF-DAC. By applying both AM-AM and AM-PM predistortion (but no memory correction), the constellation mapping of I/Q symbols are measured for 64 and 256-point (Fig. 7(b)) and the related EVM is better than -30 dB. Dynamic measurements have also been performed. Firstly, LO leakage and IQ image suppression are examined.

For this experiment, the LO frequency is set to 2.1 GHz and the frequency of I_{BB} and Q_{BB} is about 2.05 MHz. Even without applying any I/Q calibration, the LO leakage and image signals are -62 and -51 dBc, respectively, at the corresponding output power of 20.03 dBm. As such, these numbers are sufficient to meet the specifications of most communication standards. The low image level indicates the excellent I and Q path matching. Moreover, the use of a divide-by-four circuit instead of a divide-by-two approach proves also beneficial in improving the

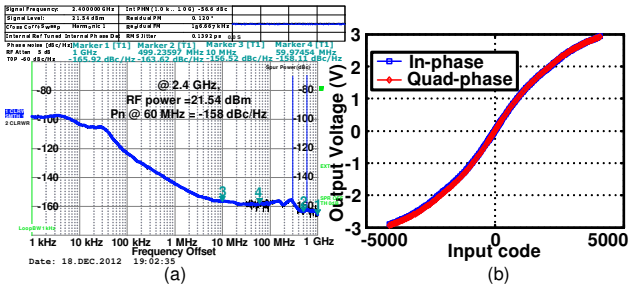

Fig. 6. (a) Phase noise at 2.4 GHz, (b) output versus input code.

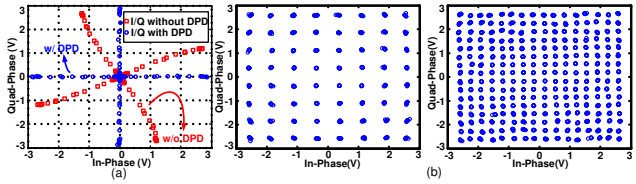

Fig. 7. (a) AM-AM/AM-PM profile, (b) constellation diagram.

quadrature operation. By applying simple I/Q calibration, the image signal can be further reduced by another 14 dB (Fig. 8(a)). The linearity of the IQ modulator is evaluated using WCDMA modulation. For this purpose, the baseband I/Q WCDMA signals are loaded into the SRAM memories. Without further action, the resulting upconverted WCDMA signal suffers from compression at the higher output levels (see Fig. 8(b)). Based on Fig. 7(a), the digital input code was predistorted (AM-AM/AM-PM) using a simple lookup table and applied as the input baseband signals. Fig. 8(b) compares the RF output signal without and with this simple DPD. Accordingly, DPD reduces the emission into the adjacent channel by more than 15 dB. Table I summarizes the measurement results and compares against the recent publications. The proposed RF-DAC has the best resolution, noise floor, efficiency, and RF output power.

V. Conclusion

In this work, a high-resolution, 2×13-bit RF-DAC-based all-digital I/Q modulator is presented. It uses 25% quadrature differential clocks to directly upconvert the upsampled I/Q baseband signals to their RF continuous-time representation. Digital-switch banks are connected to an on-chip low-loss power combining transformer network to produce 22 dBm peak output power, with 31% total system efficiency within 1.36—2.51 GHz frequency range. EVM for 64 and 256-point constellations is found to be better than -30 dB. These numbers indicate that this new concept is a viable option for the next generation of multi-band/multi-standard transmitters. The realized demonstrator can act as an energy-efficient RF-DAC in a stand-alone digital transmitter directly (e.g., for WLAN) or as a pre-driver for high-power basestation PAs.

TABLE I
Comparison Summary of I/Q Modulators

Ref	Process (nm)	Noise (dBc/Hz)	RF Power (dBm)	Resol. (bit)	Eff. (%)	EVM (dB)
[3]	130	-146	-2	10	0.04	-34
[4]	65	N/A	2.6	11	1.18	-32.4
[5]	45	-158	1	12	4.2	-34
[6]	65	-148	12.6	3	20	-28.6
This work	65	-163	22.3	13	31 $^{*}\eta_{tot}$	-30

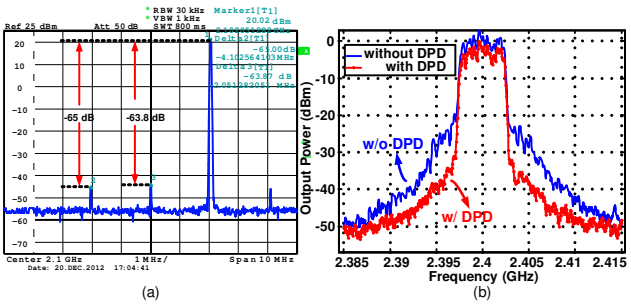

Fig. 8. (a) Image rejection and LO leakage with simple calibration, (b) WCDMA spectrum, without and with simple AM-AM/AM-PM predistortion.

Acknowledgment

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