A Frequency-Agile RF Frontend for Multi-Band TDD Radios in 45nm SOI CMOS

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***Abstract* — A tunable and highly digital RF frontend for multi-band TDD radios is integrated in 45nm SOI CMOS. The PA absorbs the TX branch of the TX/RX switch with no added loss. Peak PA output power is 27.5±0.5dBm from 1.6 to 3.4GHz, with up to 30% total efficiency at 2V. For TDD LTE applications, better than -30dBc ACLR and -25dB EVM is measured with 16-QAM, 20MHz signals from 1.65 to 3.5GHz, with up to 16.5% average efficiency and 22.9dBm average power. The broadband LNA achieves A_V > 14dB, NF=4.3 ± 1.6dB and IIP3 > -7dBm from 1.6 to 3.4GHz while drawing just 6mA from 1V.**

***Index Terms* — 4G wireless communication, low-noise amplifiers, power amplifiers, silicon on insulator technology, software radio, time division multiplexing, wireless LAN.**

I. Introduction

Radios for future mobile devices will need to support a large number of wireless standards, spread over a wide range of frequency bands. In the past, Time Division Duplexing (TDD) has been prevalent for connectivity (WLAN etc.), while Frequency Division Duplexing (FDD) has been primarily used for cellular applications. With the ongoing adoption of LTE, there is a trend of convergence. The current LTE specification [1] lists 44 bands (12 TDD and 32 FDD) for worldwide operation, ranging in frequency from 0.7 to 3.8GHz. Further, wireless connectivity through WLAN, Bluetooth etc. also requires TDD operation in various bands from 2.4 to 5.9GHz. To meet the stringent cost and form-factor requirements posed by the mobile market, it is imperative that multi-standard, reconfigurable architectures be developed for both TDD and FDD schemes.

Fig. 1(a) exemplifies a state-of-the-art multi-band mobile TDD radio. It consists of a software-defined CMOS transceiver (i.e. baseband and up/down-conversion circuitry) such as those recently reported [2], in conjunction with the RF frontend which usually employs some redundancy to cover all required frequency bands. Typically, multiple narrowband PAs [3] and LNAs are designed and switched in and out depending on the desired operating frequency. The need for PA and LNA redundancy arises from the narrowband behavior inherent in resonant RF circuits. Further, as high-power PAs and

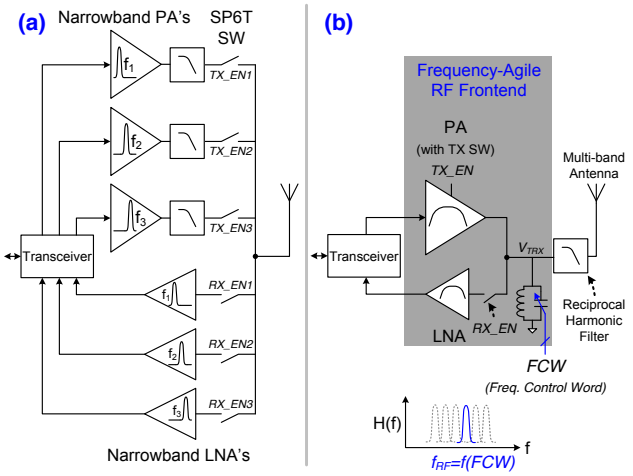


Fig. 1. (a) Conventional multi-band TDD radio (b) Proposed frequency-agile solution to eliminate RF frontend redundancy

RF switches are challenging to implement in silicon, such implementations often combine heterogeneous device technologies like CMOS, SiGe and GaAs. Clearly, this is not a cost- or area-optimal architecture for future devices.

In contrast, the proposed frequency-agile RF frontend architecture shown in Fig. 1(b) consists of a single PA, LNA and RF switch. The frequency response of the frontend can be digitally tuned over a wide frequency range (f_{low} to f_{high}) exceeding one octave. A single-chip all-silicon solution is targeted. The architecture follows a maximally-digital design philosophy, wherein both the LNA and PA unit cells utilize broadband topologies inspired by the CMOS inverter. As a result, key performance parameters like PA efficiency and frequency tuning range directly benefit from CMOS scaling. In addition, by exploiting the inherent tri-state/turn-off feature of the PA core, the need for an explicit TX branch RF switch is obviated, eliminating ~1dB loss in the TX RF path. The principal challenge of implementing a tunable RF frontend architecture compatible with high PA output power (P_{OUT}) in a highly scaled CMOS process is tolerance for high RF voltages, up to $16V_{PP}$ at the 50Ω matched I/O port V_{TRX} at 28dBm P_{OUT}. The proposed

architecture addresses this by (a) Isolating the PA core from V_{TRX} through aggressive power combining (b) Employing aggressive device stacking in the RF switch and tunable matching network with floating-body SOI transistors.

At system-level, off-chip low-pass filters are usually required at the PA outputs to attenuate odd harmonics (even harmonics are attenuated by differential design). For this design covering one octave, the 3rd harmonic of f_{low} (= $3f_{low}$) is still much higher than f_{high} (= $2f_{low}$), which indicates that a reciprocal (bidirectional) low-pass filter with $f_{high} < f_{cutoff} < 3f_{low}$ can be used here.

II. TX Architecture

The TX section is shown in Fig. 2.

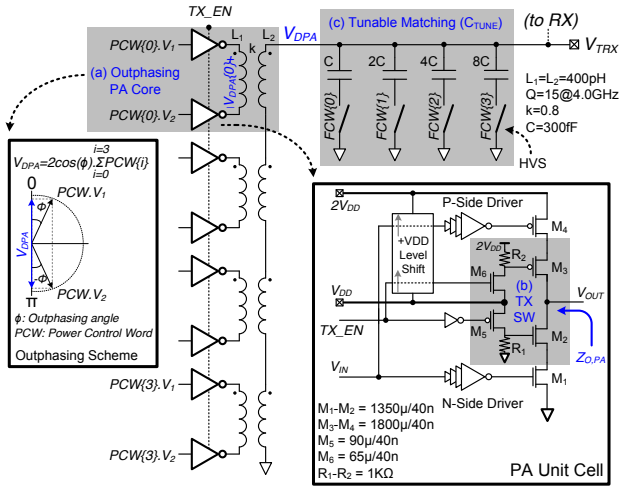


Fig. 2. TX architecture

The design builds upon prior work on the Class-D outphasing PA architecture [4]-[5]. In this work, the PA unit cell and matching network have been modified to enable lossless TX switching and frequency-agile operation respectively.

A. Outphasing Class-D PA Core

The PA unit cell employs a stacked Class-D topology to enable rail-to-rail (0 to $2V_{DD}$) RF switching at V_{OUT}. Only thin-gate transistors are used, with nominal V_{DD} = 1V. A DC level-shifted replica of the RF input V_{IN} feeds the P-side driver logic, which operates between V_{DD} and $2V_{DD}$. Since Class-D unit cells are relatively tolerant of reactive loads, two PA unit cells are arranged in an outphasing configuration with a non-isolating transformer to form the outphasing PA core, capable of achieving high efficiency in linear operation. To achieve high P_{OUT}, transformer based power combining with 4 cores is employed.

B. Embedded TX Switch

In the PA unit cell, transistors M_2 and M_3 serve a dual purpose. In TX mode (TX_EN = 1), both M_2 and M_3 are turned on through M_5 and M_6 and prevent switching devices M_1 and M_4 from seeing drain voltages in excess of V_{DD}, ensuring device reliability. In RX mode (TX_EN = 0), M_2 and M_3 function as the TX branch switch by turning off through large pull-down and pull-up resistors R_1 and R_2. The off-state PA presents an output impedance dominated by device parasitics at V_{OUT}. Parasitic capacitances are sufficiently small in this process to be considered an open circuit at frequencies of interest. The incoming RX signal at V_{TRX} sees a resonant LC tank in parallel with the RX section, so the in-band component propagates to the RX signal path. Therefore, the proposed PA unit cell essentially absorbs the TX branch switch, without additional loss.

C. Tunable Matching Network

Optimal PA impedance transformation is achieved through transformer turns-ratio and series combining. The LC resonance frequency at which it occurs is set by a digitally programmable capacitor (C_{TUNE}), controlled by a 4b Frequency Control Word (FCW). 28dBm peak P_{OUT} corresponds to $16V_{pp}$ at 50Ω port V_{TRX}, which must be tolerated by some of the capacitor switches that are in the off/open state. This High Voltage Switch (HVS) design is also used in the RX switch, and detailed in Section III.

III. RX Architecture

Fig. 3 illustrates the RX section, which consists of the RX switch and the LNA.

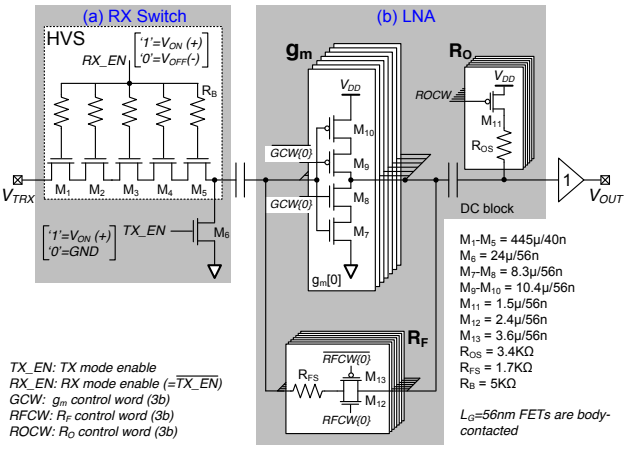


Fig. 3. RX architecture

A. RX Switch

The RX switch employs a series-shunt topology to maximize TX/RX isolation [6]. The series path uses a High Voltage Switch (HVS) with N stacked floating-body SOI NFETs.

The TX mode (TX_EN = 1, RX_EN = 0) corresponds to series-off shunt-on configuration. The LNA input is grounded, and isolated from the high voltage swing at V_{TRX} by the off HVS. In the HVS, large gate resistors are effectively open circuit at RF. The voltage stress is equally shared by a stack of 2N parasitic capacitors in series. The RX_EN signal uses a -ve logic-0 voltage V_{OFF} such that $[V_{TH} > V_{OFF}+V_{TRX(ampl.)}/2N]$, ensuring that the RF signal does not turn the stack on. Simultaneously satisfying $[BV_{OX} > |V_{OFF}|+V_{TRX(ampl.)}/2N]$ avoids oxide breakdown. Design choice of N = 5, V_{OFF} = -1.4V satisfies both conditions with some margin, while $V_{ON} = V_{DD} = 1V$.

The RX mode (TX_EN = 0, RX_EN = 1) corresponds to series-on shunt-off configuration. The RX signal passes through the on HVS device stack to the LNA.

B. Gain and Power Scalable LNA

The LNA design also follows a maximally-digital design approach. A CMOS inverter based g_m cell is employed with resistive output load ($R_{OUT} = R_O||r_{on}||r_{op}$) and shunt feedback ($R_F$) for low voltage, broadband operation. The complimentary topology reuses current, effectively doubling g_m/I_{ds} to reduce power. N/PFET g_m superposition and a nearly rail-rail output swing offer improved linearity at $V_{DD} = 1V$. For system flexibility, the LNA design also incorporates 10dB of digital gain control. The g_m cell has 7 slices that can be selectively turned off with 3b g_m control word GCW. R_F and R_O are also tunable through 3b words RFCW and ROCW respectively. For maximum gain $[A_V \approx -g_m(R_{OUT}||R_F)]$, both g_m and R_F are set to maximum while R_O is open ($R_{OUT} \approx r_{on}||r_{op}$). To reduce gain (and power) g_m, R_F and R_O are all scaled appropriately to maintain 50Ω input match $[Z_{IN} = (R_F+R_{OUT})/(1+g_mR_{OUT})]$ at lower gain.

IV. Physical Design

The prototype has been integrated in a 1V 45nm SOI CMOS process with 11 metal layers. The die micrograph is shown in Fig. 7. The RF frontend occupies an active area of only 1.5mm×1.4mm, no larger than a single CMOS PA with comparable P_{OUT} [3][5]. Custom flip-chip packaging is used for superior RF performance. Transformers are designed with the aid of 2.5D EM simulation. Since the digital stackup in this process offers

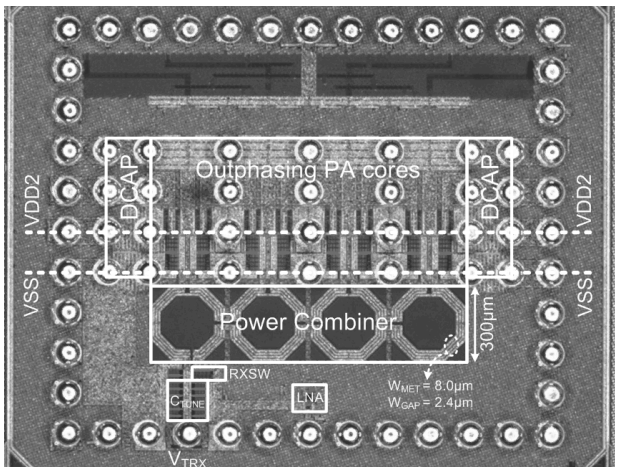


Fig. 4. Die micrograph

no ultra-thick metal, 3 top metals are used in parallel to form a low resistance, composite RF conductor. Primary and secondary inductors are composed of two windings each, interleaved to enhance the coupling, while meeting maximum metal width DRC and electro-migration limits simultaneously. To maintain supply integrity in the presence of current transients, 400pF of decoupling capacitance (DCAP) has been integrated on-chip. Further, the supply (V_{DD2}) and ground (V_{SS}) buses utilize multiple distributed bumps to reduce parasitic supply inductance.

V. Measurements

Fig. 5 shows TX mode PA measurements under single-tone drive. No off-chip filters are used. At each frequency, the FCW is optimized to maximize P_{SAT}. Nearly constant P_{SAT} of 27.5±0.5dBm is measured from 1.6 to 3.4GHz. Total efficiency (= P_{RF}/P_{DC}, including all 6 driver stages) is

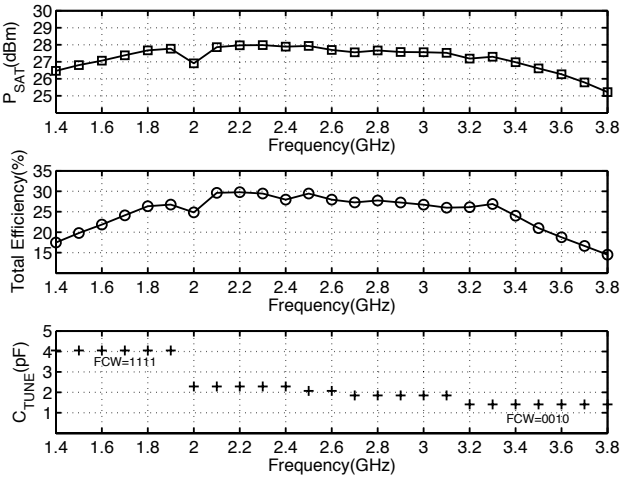
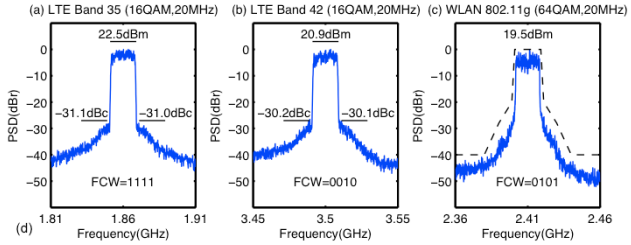


Fig. 5. PA measurements

as high as 30% at 2.3GHz. The dip at 2GHz is due to an undesired resonance on the RF input trace. Embedded TX switching makes this solution competitive with standalone PAs with ~1dB/1.25× higher P_{OUT} /efficiency.

Fig. 6 summarizes linear PA performance in outphasing mode. Tests are performed with 16-QAM, 20MHz BW, 6.2dB PAPR signals in several LTE bands from 1.65 to 3.5GHz. To benchmark intrinsic linearity, no predistortion is applied. Again, for each band, the optimal FCW is used. ACLR is measured with channel BW and offsets for E-UTRA and UTRA scenarios [1]. Average efficiency is as high as 16.5% at 1.72GHz with 22.9dBm P_{OUT} and -28dB EVM. ACLR is better than -30dBc from 1.65 to 3.5GHz. This frequency range covers 11 (out of 12) TDD LTE bands. Further tests with 802.11g (20MHz, 64-QAM) signals at 2.41GHz show that the PA also meets the WLAN mask at 19.5dBm P_{OUT} and -25.4dB EVM.



Freq. (GHz)	LTE TDD Band#	LTE FDD[1] Band#	FCW	P_{AVE} (dBm)	Ave. Eff.(%)	EUTRA ACLR (dBc)	UTRA ACLR1 (dBc)	UTRA ACLR2 (dBc)	EVM (dB)
1.65		24	1111	22.7	16.0	-31.3	-34.9	-37.4	-27.9
1.72		3,4,10	1111	22.9	16.5	-31.2	-34.2	-37	-28.1
1.86 (a)	35	2,25	1111	22.5	15.8	-31.1	-37.2	-39.3	-27.3
2.31	40		0110	21.9	13.0	-31.1	-33.4	-36	-26.2
2.56		7	0101	21.6	12.8	-30.1	-35.3	-36.2	-25.8
2.65	38,41		0101	21.8	12.5	-30.6	-35.7	-36.6	-26
3.50 (b)	42		0010	20.9	9.2	-30.1	-33.6	-35.6	-27.5

[1]*FDD bands shown only to highlight broadband PA response. FDD frontend would require different system-level implementation*

Fig. 6. PA measurements in linear outphasing mode

Parameter	Francois et al., TMTT 2012	[5] Tai et al., JSSC 2012	[4] Xu et al., JSSC 2011	Kousai et al., ISSCC 2010	This Work
CMOS Process	90nm	45nm	32nm	130nm	45nm SOI
Center Freq. (GHz)	0.93	2.40	2.40	1.80	Tunable
1dB BW (GHz)	**0.3[1]**	**1.0[1]**	**0.8[1]**	**1.2**	**1.8**
P_{SAT} (dBm) / Peak Eff. (%)	29.4 / 25.8	31.5 / 27.0	25.3 / 35.0	31.3 / 42.0	28.0 / 30.0[2]
Waveform BW/Mod/PAPR	10M/16QAM/6.9dB	20M/64QAM/6.0dB	20M/64QAM/5.8dB	10M/16QAM/8.5dB	20M/16QAM/6.2dB
Linear Test Range (GHz)	**0.93 only**	**2.40 only**	**2.40 only**	**1.75-1.95**	**1.65-3.50**
Ave. P_{OUT} (dBm) / Eff. (%)	25.9 / 17.0	24.8 / 16	19.6 / 21.8	25.0 / 20.0	22.9 /16.5[3]
EVM (dB)	-25.0	-25.0	-25.0	-26.0	-28.1
Predistortion	Yes	Yes	No	Yes	No

[1] Estimated from graph | [2] Best single tone performance (2.31GHz) | [3] Best linear performance (1.72GHz)

Table. 1. PA performance comparison with recent publications

Fig. 7 shows RX mode LNA measurements. A_V > 14dB, NF = 4.3±1.6dB and IIP3 > -7dBm (20MHz tone spacing) are measured from 1.6 to 3.4GHz with only 6mA current drawn from V_{DD} = 1V. For this measurement, FCW is

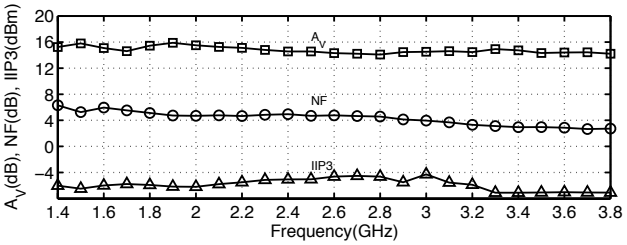


Fig. 7. LNA measurements

tuned to obtain the best A_V over frequency like the PA measurement. RX branch switch loss was also individually measured with a test structure to be ~2dB.

VI. Conclusion

A frequency-agile RF frontend for TDD radios, which is fully integrated in 45nm SOI CMOS technology has been reported in this work. With the large number of frequency bands required for ubiquitous coverage and connectivity, reconfigurable RF frontends such as the one reported will serve as critical building blocks to reduce the form-factor, complexity and cost of future mobile radios. Further research into tunable duplexers and filters is needed to enable even more ambitious and universal (TDD+FDD) radio solutions covering multiple octaves.

Acknowledgement

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