A 1.9nJ/bit, 5Mbps Multi-Standard ISM Band Wireless Transmitter Using Fully Digital PLL

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***ABSTRACT* — This paper presents an energy efficient transmitter for multi-standard applications (IEEE802.15.4, BLE, 5Mbps) in ISM2.4GHz band. It incorporates a fully digital PLL with two point modulation to achieve upto 5Mbps data rate at 9.5mW power consumption (including all power management blocks) at 0dBm output power, leading to 1.9nJ/b efficiency. The proposed digital PLL uses a counter based area and power efficient re-circulating TDC, current reuse low area DCO using resistive tail, process compensated high speed divider, class-AB PA stages, and fully integrated on-chip LDOs. The entire transmitter occupies 0.35mm^2 Silicon area in a 65nm digital CMOS process.**

***Index Terms* — multi-standard transmitter, high data rate loop modulator, ultra low energy, digital PLL, low area.**

I. Introduction

Ultra low power and energy efficient radio transceivers have found widespread use for wireless sensors, medical and other emerging applications [1-4]. This paper presents an energy efficient, multi-standard transmitter operating in ISM 2.4GHz band using fully digital PLL (DPLL) architecture. The transmitter meets the system requirements of IEEE802.15.4, Bluetooth low energy (BLE), enhanced data rate mode with data rates of 250kbps, 1Mbps, 5Mbps respectively. Two point modulation using DPLL provides two principal benefits for phase/frequency modulations: (a) Provision of completely matched digital injection capable of supporting data rates beyond the PLL's loop bandwidth without any complicated calibration loop, (b) Lower area, finer TDC resolution, design ease and scalability, that scale directly with technology node. However, these advantages of digital PLL are somewhat undermined by their high power consumption even at scaled CMOS nodes, along with the presence of spurious tones due to higher switching activities. These deficiencies of reported DPLLs in open literature have presented significant difficulty for their use in low power, low energy systems. In this paper, we present techniques to achieve a low power DPLL based digitally-intensive transmitter in 65nm standard CMOS technology that uses current-reuse DCO, dynamic logic based divider, counter based time to digital converter (TDC) and class-AB PA, consuming total power of 9.5mW leading to a best in class energy efficiency of 1.9nJ/bit with DPLL consuming only 0.22mm^2 Silicon area.

II. Low Energy Digital PLL

The proposed DPLL architecture is illustrated in Fig. 1. Unlike [5], the proposed DPLL divides down the higher frequency F_{REF} to F_R, lowering the dynamic power consumption and reducing F_{REF} spurs at the expense of higher in-band noise from TDC. The Digitally Controlled Oscillator (DCO) operates at 4.8GHz followed by divide by 2 to obtain 2.4GHz RF signal for TX and RX. The output pulses at 2.4GHz are accumulated in a counter, which consists of two parts: A binary counter that generates the integer part and the TDC that generates the fractional part. At any given instant the TDC output represents the time elapsed from the last DCO edge as a fraction of the DCO period.

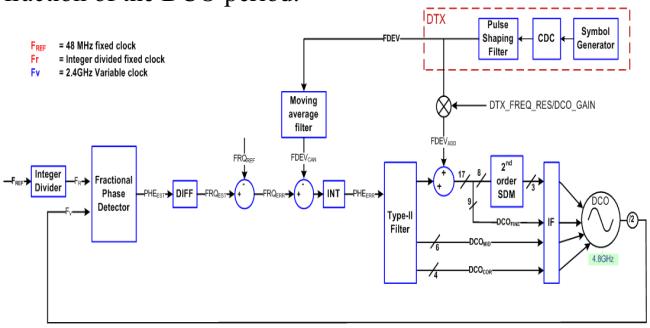


Fig. 1. Toplevel architecture of the proposed DPLL

Fig. 2 shows details of a digital phase detector that provides estimated phase of F_R w.r.t. DCO clock (F_V) and is sampled at every F_R edge. The estimated phase is differentiated to get estimated frequency, which is directly subtracted from reference frequency and also from the modulated data of the cancellation path. This frequency domain operation provides a power efficient implementation of two-point modulation by saving an accumulator. The resulting frequency error is integrated to obtain the phase error, which is processed through a type-II digital filter. The filter output is added to the modulated data of the addition path to generate the final fine code. To increase the resolution of DCO cap array, the fine code is further split into integer and fractional parts, where fractional part is processed through 2^{nd} order $\Delta\Sigma$ modulator. The integer fine code controls DCO fine cap array, while $\Delta\Sigma$ output controls 3-caps of the bank.

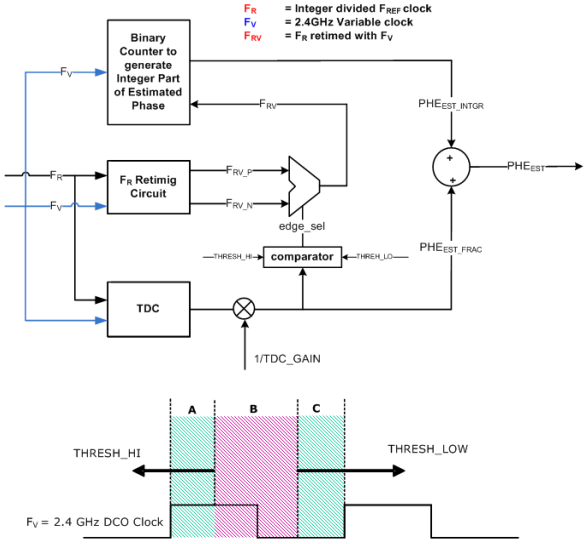


Fig. 2. Block diagram of proposed cyclic TDC and threshold detection

However, this implementation poses a practical problem. As the F_V and F_R have a fractional ratio, the DCO and F_R edges cross each other periodically. Whenever this occurs, there is a probability that the DCO integral count is changing, while it is being sampled, leading to meta-stability, and hence an error of ±1 in the estimated DCO phase. This problem is solved by synchronizing F_R to both the rising and the falling edges of the DCO output and then using the safer of the two. The safer edge is detected with the use of TDC output as illustrated in Fig. 2. Here the fractional DCO count from the TDC is compared with two thresholds. If the count is within windows A or C, the F_R edge is close to the DCO rising edge and thus F_R synchronized with the DCO falling edge is used to sample estimated phase. On the other hand if the fractional count is within window B, F_R synchronized with the DCO rising edge is selected. This dual-edge detection scheme facilitates the use of an area and power efficient re-circulating TDC instead of a power hungry linear TDC, used in [6].

The digital MODEM implements phase/frequency modulation schemes, and provides a maximum symbol rate of 2Mcps, 1Msps, 2Msps for IEEE802.15.4 using OQPSK, BLE using GFSK, and 5Mbps modes using 8CPM modulation. Implementation of 5Mbps data rate is achieved by coding 2.5 bits in each symbol and each of the symbols is mapped to any of the 8 levels, using a constant phase modulation (CPM) as described in [7]. Fig. 3 illustrates the modulator block diagram. The bits are converted from serial to parallel at the input of the modulator. Groups of 5 bits are then fed into the FEC stage, which in turn produces 2 symbols for each of the incoming 5 bits. The FEC stage outputs two 8-ary symbols to the shaping stage. A partial response shape is used to smoothen symbol transitions without introducing excessive ISI.

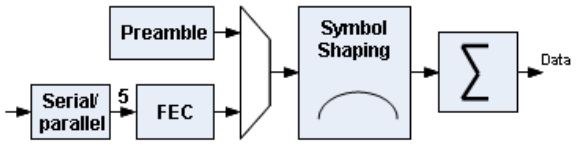


Fig. 3. Block diagram of high data rate MODEM and symbol mapper

III. Low Energy Analog Circuits

The core of the DPLL consists of a current reuse, self biased direct cross-coupled NP-core based L/C oscillator with digitally controlled resistive tail to provide 4.8Ghz operating frequency and shown in Fig 4.

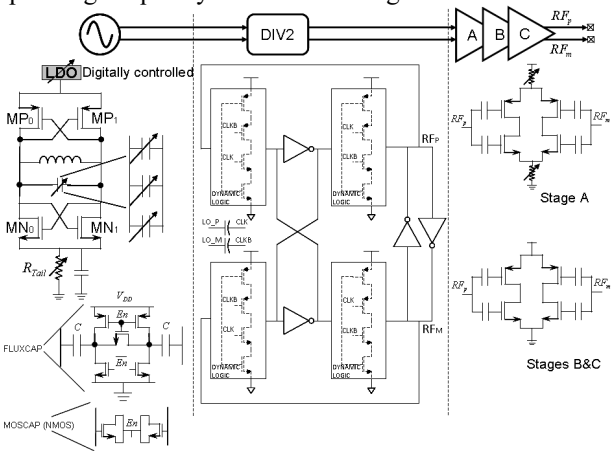


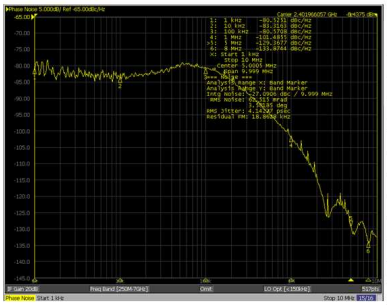
Fig. 4. Circuit description for DCO, DIV2 and PA stages

This oscillator approaches to the voltage limited region of the phase noise quite fast, and is an attractive choice for low energy systems. Use of a resistive tail significantly reduces flicker noise contribution from current source that is used in conventional L/C oscillator design. Current sources implemented using transistors consume large channel length to reduce flicker noise, and the mirroring transistor consumes additional DC current, which can be a significant fraction of the core oscillator current. In addition, continuously running analog amplitude control loop in conventional architectures consume current and introduces noise, leading to degradation of dynamic range per unit power consumption. In contrast, resistive tail provides low power, low area and flicker-noise free current source. The passive resonator tank has been implemented using a fully symmetric inductor utilizing thick top CU layer along with Aluminum routing layer to achieve a differential Q factor ~15 at 4.8Ghz. The frequency tuning is performed w.r.t. three capacitive banks: (a) coarse array, (b) mid array, and (c) fine array. Coarse array is implemented by metal-metal comb capacitors with PMOS pullup while the mid array and fine array unit elements are implemented using regular NMOS transistors. The fine array elements are the smallest in the capacitor bank, and are switched during modulation. To ensure a good EVM of the transmitter signal, the fine-array has been implemented using thermometer coded elements and achieves <3.5% linearity while providing 180kHz/LSB steps @ 2.4GHz, leading to 700Hz frequency resolution (with 3 $\Delta\Sigma$ modulator bits). The DCO consumes ~700uA current from 1.3V supply.

The LO operates at 2X the required frequency of 4.8 GHz to increase passive quality factor and mitigate LO pulling. To remain within power budget, this mandates the need for an extremely low-power divider that generates the /2 signal while taking in a low-swing (~750mVpp) input from the LO. The divider is implemented using dynamic-logic which consumes lower area (and lower routing parasitics) compared to CML dividers, and consists of 2-phase TX and 4-phase RX buffers that consumes ~725uA, from a 1.3V supply. The divider employs adaptive biasing of the LO switching devices on the divider close to threshold (Vt). A fixed trickle current into a diode-connected replica device is used to generate the bias that automatically adapts to process and temperature variation. Loading on the divider has been optimized by providing approximately equal loading in RX/TX modes and providing power-efficient buffer-distribution system. Power consumption is also optimized by limiting the signal swing within rails while relaxing the rise-fall times from the TX buffer. Fig. 4 illustrates the circuit details of divider. The transmitter utilizes a 3 stage class AB style power amplifier to provide -20dBm to +5dBm output power.

IV. Measurement Results

Fig. 5 summarizes the measured results of the DPLL. The DPLL provides very low level of spurious signals without needing special isolation from additional masks such as deep NWELL. All the local LDOs are implemented fully on-chip. Compared to the open literature, these results present a significant improvement in energy consumption compared to state-of-the-art DPLLs and even some analog PLLs in scaled CMOS nodes.



	Parameters
Power	3.96 mW
DPLL Area	0.22 mm² in 65nm
Phase noise	-83 dBc/Hz @ 10kHz -80 dBc/Hz @ 100kHz -101 dBc/Hz @ 1MHz -134 dBc/Hz @ 10MHz
LBW	100kHz
Jitter	4.2pS
Spurs	< -70 dBc

Block	Power in mW (Current)
XOSC	0.49 (375uA,1.3V)
DCO	0.91 (700uA,1.3V)
DIV2	0.94 (725uA, 1.3V)
DIG LOOP	1.5 (1200uA, 1.25V)
TDC	0.12 (100uA, 1.25V)
Total DPLL	3.96
PA	5.54 (4465uA, 1.3V)
Total TX	9.5
Data rate	5.0 Mbps
Energy	1.9 nJ/b

Fig.5. Measurement results of DPLL

Fig. 6 details the measurement results of the proposed multi-standard transmitter. In all cases, the transmitter meets the spectral mask and modulation requirements as defined by the regulation body and the communication standards, and provides clear eye opening.

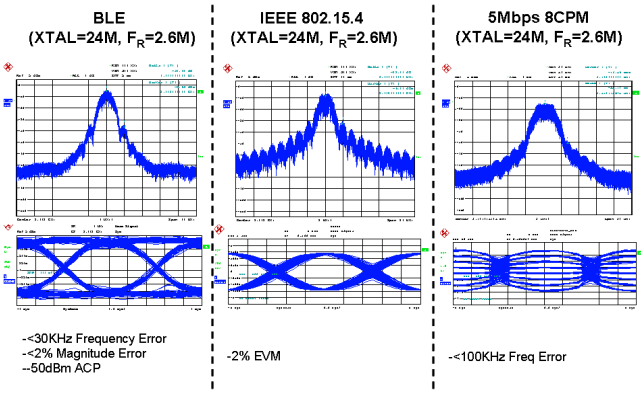


Fig. 6. Measurement results of multi-standard digital transmitter

Fig. 7 provides the performance comparison with recent state-of-the-art reports for low energy radios. Successful use of the low power techniques in the DPLL results in lowest energy consumption compared to the recently reported solutions that are even using analog type PLL. The use of DPLL based transmitter also favors highest data rate modulation compared to the reports in open literature.

	This work	[1]	[2]	[3]	[4]
Supported MODEM	**IEEE802.15.4 (a) BLE (b) 5Mbps 8CPM (c)**	IEEE802.15.4 (a) IEEE802.15.4g (b) BLE (c) IEEE802.15.6(d)	IEEE802.15.4	IEEE802.15.4	BLE
Data rate & modulation	**2Mcps HS-OQPSK 1Mbps GFSK 5Mbps 8CPM**	2Mcps HS-OQPSK 200kbps GFSK 1Mbps GFSK 600ksps pi/2 DQPSK	2Mcps HS-OQPSK	2Mcps HS-OQPSK	1Mbps GFSK
Technology	**65nm**	90nm	180nm	180nm	N.A.
Architecture	**Digital PLL, 2 point modulation**	Analog PLL, 2 point modulation	Analog PLL, 2 point modulation	Analog PLL	N.A.
Max Pout	**+5dBm**	-1dBm	+3dBm	+3dBm	0dBm
TX EVM/ FSK error	**2.0% for (a) 30kHz for (b)**	2.3% for (a) <4.8% for (b) 2.8% for (c) 7.6% for (d)	8%	2%	N.A.
Power consumption	**PLL: 3.96 mW PA : 5.54 mW Total: 9.5 mW @Pout =0dBm**	PLL: 1.1mW PA: 3.2 mW Total: 5.4mW @Pout =-1dBm	PLL: 11.8mW PA: 10.1 mW Total: 28.2mW @Pout=+3dBm	PLL: 13.3mW PA: 16.3 mW Total: 32.4mW @Pout=+3dBm	PLL: 11.3mW PA: 8.0 mW Total: 21.0mW @Pout=0dBm
Energy effifiency	**1.9nJ/b (@ 5Mbps)**	2.7nJ/b (@ 2Mcps)	14.1nJ/b	16.2nJ/b	21.0nJ/b

Fig. 7. Performance comparison with state-of-the-art

Fig. 8 shows the die micrograph of the DPLL based transmitter in 65nm CMOS. The core area of the transmitter is 0.35mm^2, including power management and crystal oscillator, which is the lowest compared to the recently reported solutions, favored by the DPLL based implementation.

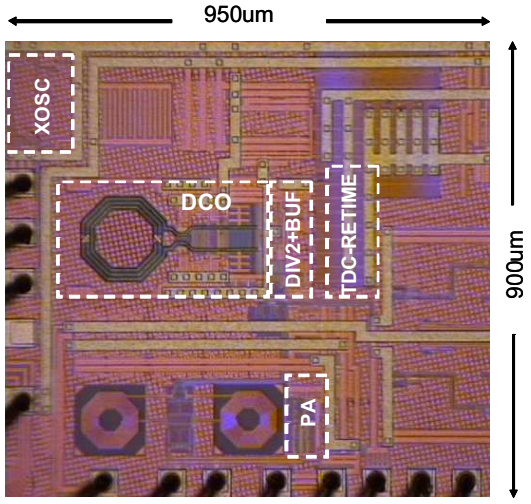


Fig. 8. Die photograph of the low energy transmitter

VI. Conclusions

In summary, we've presented a multi-standard (BLE, ZigBee and 5Mbps proprietary), low energy consumption transmitter using digital PLL (DPLL) based architecture. Various circuit/system techniques have been used to significantly reduce current consumption of the fundamental DPLL architecture while improving performance at no analog mask adder. The entire transmitter consumes 9.5mW power, operates upto 5Mbps, leading to 1.9nJ/b efficiency, and occupies 0.35mm^2 Silicon area. To the best of our knowledge from the recent reports in open literature, the proposed transmitter provides lowest energy, highest data rate for short range ISM transmitter, and occupies lowest Silicon area for a multi-standard application.

Acknowledgement

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