A wideband voltage-biased LC oscillator with reduced flicker noise up-conversion

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***Abstract*—The demand of voltage-controlled oscillators (VCOs) with a broad tuning range can lead to unacceptable degradation of the $1/f^3$ phase-noise component if traditional voltage-biased topologies are implemented. In this paper, a novel VCO architecture is proposed, where a segmented transconductor tailors the negative g_m depending on the operating range to ensure that flicker-noise up-conversion remains minimal. The implemented oscillator covers both 4G and WiMAX 2.5-GHz operation modes and achieves a 10-dB reduction of the $1/f^3$ phase noise without impairing the $1/f^2$ phase-noise performance.**

***Index Terms*—Voltage-controlled oscillator (VCO), flicker noise, phase noise, AM-to-PM conversion**

I. Introduction

The recent trend in wireless communications to integrate various standards on a single chip [1],[2] demands the use of a wideband voltage-controlled oscillator (VCO). The approach to this integration is to implement RF functions in CMOS technology. Unfortunately, this choice usually fails to comply with tight phase-noise requirements due to: 1) poor quality factor of monolithic inductors and 2) higher flicker noise corner-frequency in CMOS compared to other technologies. The latter issue drastically limits the achievable performance when the integral phase noise of local oscillator (LO) must be kept low. Such a case is met in WiMAX operation mode implementing Orthogonal Frequency-Division Multiplexing (OFDM) where the PLL output phase jitter results into inter-carrier interference. In scaled CMOS technologies, the output phase jitter can be largely dominated by the $1/f^3$ phase noise of the VCO arising from the up-conversion of flicker noise into phase noise. In [3], a detailed analysis of flicker noise up-conversion mechanisms was carried out for the voltage-biased oscillator topology. Basing on those theoretical results, in this paper we present the design of a novel VCO topology aiming at minimizing $1/f^3$ phase noise over the broad tuning range of 1.6-2.6 GHz. With respect to the well-known current-biased differential topology, the circuit does not feature a bias current generator, thus removing dominant contributions to both $1/f^2$ and $1/f^3$ phase noise [4]. The paper describes the novel VCO, implemented in a 65-nm CMOS technology, together with the results of the experimental characterization that successfully confirm the theoretical insight and the modeling predictions.

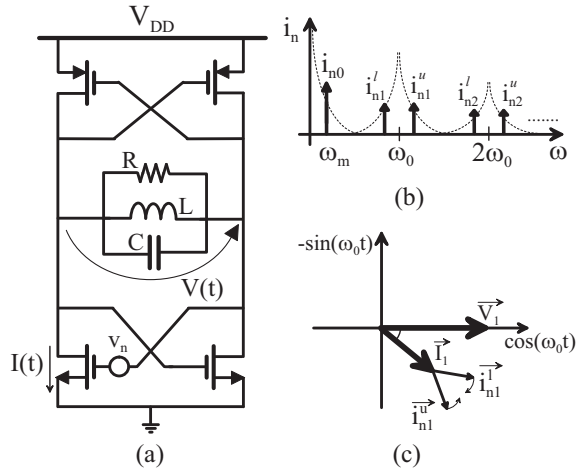

Fig. 1. (a) Traditional voltage-biased topology; (b) Up-converted flicker-noise tones; (c) Phasor plot of the first harmonics of the oscillator output voltage and current.

II. $1/f^3$ phase noise in voltage-biased oscillators

The traditional voltage-biased oscillator is depicted in Fig. 1(a), where a gate-referred flicker noise source is also shown. In [3] it has been pointed out that the $1/f^3$ phase noise in this topology increases by increasing the excess gain G_X=g_mR, where g_m is the overall small-signal transconductance of the negative-resistance element and R is the equivalent parallel loss resistance of the LC tank. In particular, due to the large signal time-variant regime of the oscillator a single tone of the gate-referred flicker noise translates into a set of correlated current tones around each harmonic of the fundamental frequency, as depicted in Fig. 1(b). Being the impulse sensitivity function almost sinusoidal [5],[6],[7] only the noise tones i^u_{n1} and i^l_{n1} around the fundamental harmonic contribute to phase noise. The resultant of $\overrightarrow{i^u_{n1}}$ and $\overrightarrow{i^l_{n1}}$ is in phase with the first harmonic I_1 of the transistor current, which lags with respect to the output voltage V_1 due to the Groszkowski effect [8], as shown in Fig. 1(c). As a result, i^u_{n1} and i^l_{n1} modulate the first harmonic of the output voltage both in amplitude and phase. Hence, two mechanisms are involved, namely a direct injection into the LC tank of phase modulation (PM) current components (*direct*

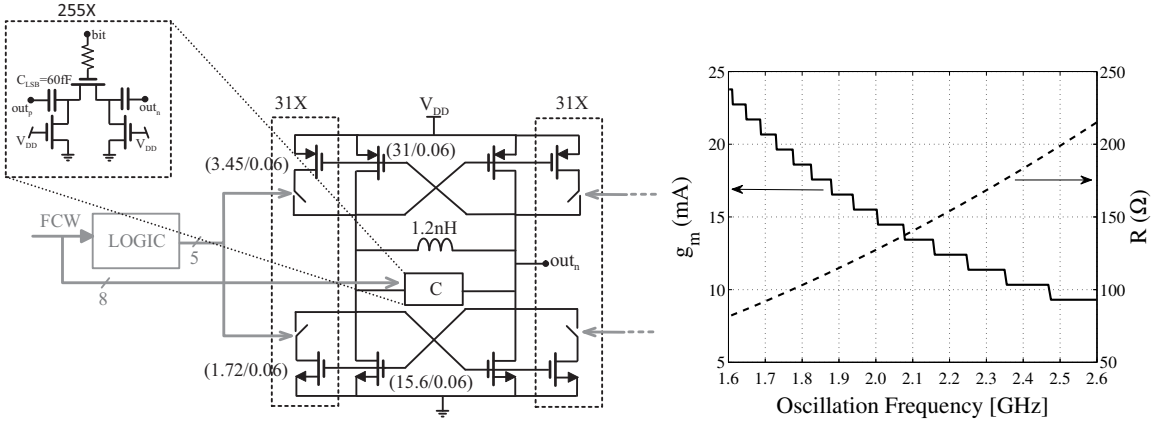

Fig. 2. (a) Schematic of the fabricated oscillator implementing the proposed topology; (b) Equivalent parallel loss resistance R and optimum value of small-signal transconductance g_m as functions of the oscillation frequency.

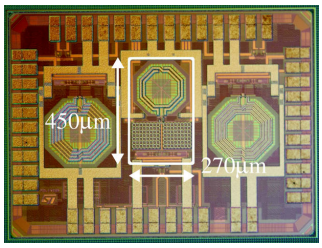

Fig. 3. Die photograph.

Groszkowski contribution) and an AM-to-PM conversion effect via a modulation of the harmonic content of the output voltage (*incremental Groszkowski contribution*). Both mechanisms are emphasized as the the excess gain is raised since the oscillator non-linearity is increased. According to eq. (51) in [3], the $1/f^3$ phase noise is proportional to:

$$SSCR(\omega_m) \propto \frac{\left(G_X^2-1\right)^2 \omega_0}{V_1 Q^3 C}, \qquad (1)$$

where ω_0 is the oscillation angular frequency, V_1 the oscillation amplitude, Q and C the tank quality factor and capacitance, respectively.

III. The Proposed Topology

The result pointed out in Section II suggests that the oscillator design should be accomplished by limiting the excess gain value. However, in practical applications this requirement is conflicting with the increasing tuning range width. Since frequency tuning is implemented by changing the value of a tunable capacitor, the equivalent parallel loss resistance of the tank R does not remain constant. If the tank losses are determined by the inductor series resistance, r_s, it is $R \cong \frac{(\omega_0 L)^2}{r_s}$.

In the traditional voltage-biased topology, the small-signal transconductance g_m is therefore chosen to guarantee a reliable oscillation start-up, i.e. $G_X \cong 2$, at the minimum frequency, where the equivalent parallel loss resistance is the lowest. As a consequence, by increasing the oscillation frequency the excess gain increases, thus degrading the $1/f^3$ phase-noise performance. To avoid this trend, a mechanism is therefore needed to adjust the g_m value to the corresponding R value, thus keeping G_X approximately equal to 2 over the whole tuning range. To this aim, Fig. 2(a) shows a novel voltage-biased topology where the transconductor is split into a main part that provides the minimum g_m value required at the maximum frequency and a set of 31 cells, digitally-controlled by a transconductance control word (TCW). This signal can be set externally or by a digital circuit to track the tank capacitance. The tank capacitance consists on 255 MIM (metal-insulator-metal) capacitor-based cells connected as shown in Fig. 2(a) and controlled by a frequency-control word (FCW). This 8-bit digital word is used to switch-on the capacitive cells needed to synthesize the required oscillation frequency, thus FCW=0 and FCW=255 correspond to the maximum and the minimum oscillation frequency, respectively. A fine tuning of the oscillation frequency is obtained by using a pair of accumulation-PMOS varactors with a sensitivity k_{VCO} lower than 8 MHz/V. Such a small tuning gain has been chosen not to further worsen the AM-to-PM conversion mechanism.

The FCW range (0:255) has been divided into 16 equally-spaced intervals. While in the first interval (0:15) only the transconductor core is active, in each of the following intervals an additional g_m-cell is turned on to compensate the decrease of the parallel resistance. The cells have been sized in order to keep the excess gain

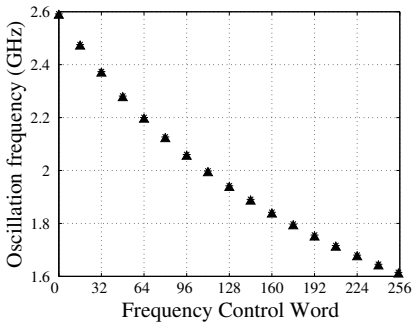

Fig. 4. Measured oscillation frequency of two VCO samples.

approximately constant and equal to 2 as the frequency spans along the tuning range. A larger number of cells have been integrated either to verify the theory on a broad interval of the excess gain values and to eventually compensate a lower quality factor of the inductor at the maximum frequency.

Fig. 2(b) shows the overall transconductor g_m together with the estimated values of the equivalent parallel loss resistance as functions of the oscillation frequency. The g_mR-product is always in the range 1.9-2.1 assuring a reliable and fast oscillation start-up and, in the meantime, a low flicker-noise up-conversion.

The switches connecting the transconductance cells to the rest of the circuit are placed in series to the drain of the transistors. To ensure a low series resistance along the whole oscillation period, they have been implemented by using pass-transistors. Their noise contribution is expected to be negligible since their MOSFETs work either in deep triode or in off region.

IV. Measurement results

The proposed topology has been integrated in a 1.2-V 65-nm CMOS technology. The microphotograph of the oscillator die is shown in Fig. 3. The VCO covers the 1.6-2.6 GHz band and the measured oscillation frequency as a function of the FCW is reported in Fig. 4. Phase-noise measurements have been performed by using an Anritsu MS2690A signal analyzer running the phase-noise measurement option while the circuit has been powered by a battery. The $1/f^3$ phase noise has been quoted as single sideband-to-carrier ratio at 1-kHz frequency offset. The measurements have been carried out in two different operative conditions:

1) by keeping on all the transconductance cells, thus guaranteeing the oscillation start-up over the whole tuning range (g_m max.);
2) by changing the number of active transconductance cells according to the FCW (g_m opt.).

These two conditions correspond to set the TCW as in Fig. 5. Note that in the latter case, for FCW=0 the number of the transconductance cells on is not 0, which would correspond to leave active only the core transconductor. In fact, the inductor quality factor has been estimated to be approximately 6 at 2.6 GHz, instead of about 10.5 as predicted from post-layout simulations, thus the condition $G_X \cong 2$ is reached only turning on 11 g_m-cells.

The measured $1/f^3$ phase noise on two oscillator samples is shown in Fig. 6. As predicted, by following the traditional design the $1/f^3$ phase noise rapidly rises as the oscillation frequency is increased due to the growing excess gain. Instead, the segmented topology reduces the flicker noise up-conversion over the whole tuning range and by almost 10 dB at the highest oscillation frequency (FCW=0). A residual increase of the $1/f^3$ noise may be still noticed as the oscillation frequency increases due to the decreasing value of the tank capacitance.

Fig. 6 also shows the comparison with SpectreRF simulation results. A good agreement is achieved by assuming a tank quality factor equal to 6. For comparison, the projected performances achievable by a tank with the nominal Q of 10 are also shown.

Fig. 7 shows the measured phase noise spectra at FCW=0 for different excess gain values turning on an increasing number of g_m-cells. The measured SSCR at 1-kHz frequency offset as function of the TCW for two values of FCW is plotted in the inset. Once the FCW is set, as the TCW is increased the transconductance of the active element and thus the oscillator excess gain increase, leading to a rapid growing of the $1/f^3$ phase noise.

As far as the $1/f^2$ phase noise is concerned, Fig. 8 plots the measurement results performed in the same two conditions described before. An increase of only 1 dB is observed, meaning that the proposed topology is not detrimental neither in terms of smaller oscillation amplitude nor in terms of additional noise due to switches.

Finally, Table I reports a comparison of recently published wideband VCOs. In this work, the oscillator performance is evaluated by using a figure of merit $FoM_T^{(1/f^3)}$ that is normalized with respect to the tuning range and that takes into account the $1/f^3$ shape of phase noise. To this aim, the figure of merit has been evaluated as follows:

$$FoM_T^{(1/f^3)} = -SSCR(\omega_m) - 10\log\left(\frac{P_{diss}}{1\,\text{mW}}\right) + \\ +20\log\left(\frac{\omega_0}{\omega_m^{1.5}} \cdot \frac{TR[\%]}{10}\right), \quad (2)$$

where TR is the tuning range expressed as percentage. When compared to the state-of-the-art VCOs, the proposed oscillator shows an average $1/f^3$ phase noise of -48 dBc/Hz at 1-kHz offset. Only the oscillator in [9] outperforms the presented VCO, albeit it was designed in a less scaled technology. Moreover, this result was obtained with a higher power consumption and a narrower tuning range, thus the oscillator in [9] features a lower

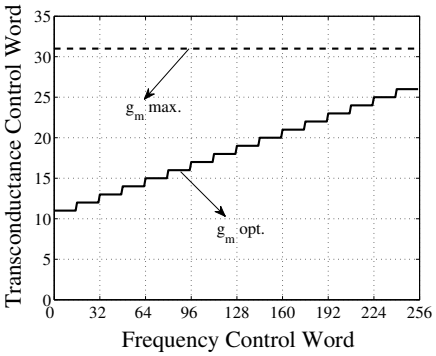

Fig. 5. TCW vs. FCW with g_m max. and g_m opt.

Parameter	[10]	[9]	[11]	this work
Technology	0.13 μm	0.25 μm	65 nm	65 nm
Frequency (GHz)	2.15	2.7	4.01	2.1
Tuning Range (%)	92.6	28.6	75	47.6
Power Supply (V)	1.5	2.0	0.6	1.2
Power cons. (mW)	30	20	9.8/14.2	8/14.5
$\mathcal{L}$(1kHz) (dBc/Hz)	-52/-35	-54/-44	-44/-32	-50/-46
$FoM_T^{(1/f^3)}$ (dB)	148/139.4	147.7/139.6	147.9/144.4	145.4/148.4
$\mathcal{L}$(1MHz) (dBc/Hz)	-124/-120	-135/-133	-130/-125.7	-124/-120.5

TABLE I

$FoM_T^{(1/f^3)}$. In summary, the comparison shows that the presented design achieves both wide tuning range and low $1/f$ noise up-conversion over the whole frequency range.

REFERENCES

[1] A. Berny *et al.*, "A 1.8-GHz LC VCO with 1.3-GHz tuning range and digital amplitude calibration," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 909–917, April 2005.

[2] N. H. W. Fong *et al.*, "Design of wide-band CMOS VCO for multiband wireless LAN applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1333–1342, 2003.

[3] A. Bonfanti *et al.*, "Flicker noise up-conversion due to harmonic distortion in Van der Pol CMOS oscillators," *IEEE Trans. Circuits Syst. I: Reg. Paper*, vol. 59, pp. 1418–1430, July 2012.

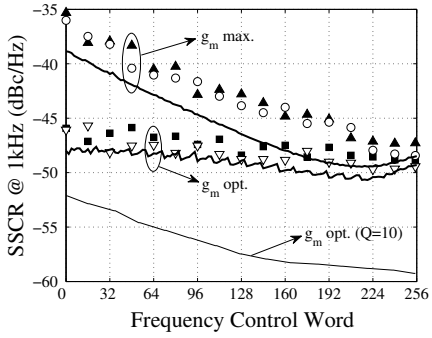

Fig. 6. $SSCR$ at 1-kHz offset of two VCO samples. Symbols refer to measured values, while solid lines to simulations.

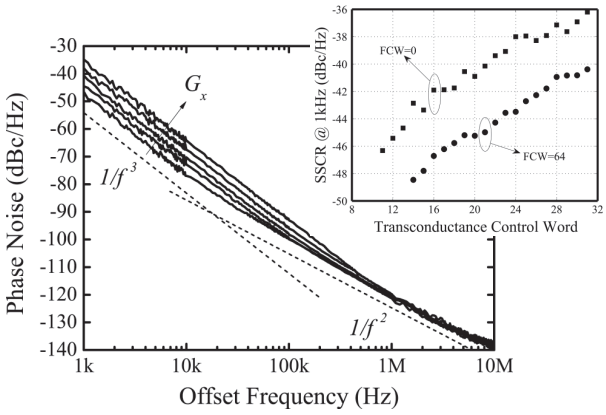

Fig. 7. Measured $SSCR$ for different excess gain values with FCW=0. In the inset, $SSCR$ at 1-kHz offset vs. TCW.

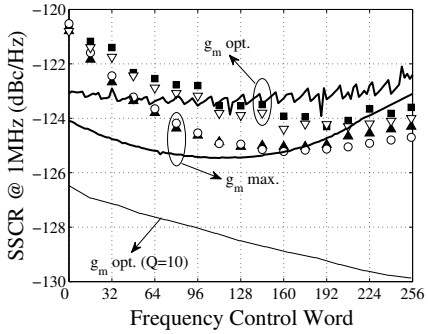

Fig. 8. Measured $SSCR$ at 1-MHz offset of two VCO samples.

[4] S. Levantino *et al.*, "Frequency dependence on bias current in 5-GHz CMOS VCO's: Impact of tuning range and flicker noise up-conversion," *IEEE J. Solid State Circuits*, vol. 37, no. 8, pp. 1003–1011, Aug. 2002.

[5] A. Hajimiri and T. Lee, "A general theory of phase noise in oscillators," *IEEE J. Solid State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.

[6] S. Levantino *et al.*, "Efficient calculation of the impulse sensitivity function in oscillators," *IEEE Trans. Circuits Syst. II: Expr. Briefs*, vol. 59, no. 10, pp. 628–632, 2012.

[7] F. Pepe *et al.*, "An efficient linear-time variant simulation technique of oscillator phase sensitivity function," *Proc. of SMACD 2012 International Conference*, pp. 17–20, 2012.

[8] J. Groszkowski, "The interdependence of frequency variation and harmonic content, and the problem of constant-frequency oscillators," *Proc. of the IRE*, pp. 958–981, July 1933.

[9] A. Koukab, "Reactive power imbalances in LC VCOs and their influence on phase-noise mechanisms," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 12, pp. 3118–3128, December 2011.

[10] Y. Takigawa *et al.*, "A 92.6% tuning range VCO utilizing simultaneously controlling of transformers and MOS varactors in 0.13 μm CMOS technology," in *RFIC 2009*, June 2009, pp. 83–86.

[11] G. Li, L. Liu, Y. Tang, and E. Afshari, "A low-phase-noise wide-tuning-range oscillator based on resonant mode switching," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1295–1308, June 2012.