A WLAN RF CMOS PA with Adaptive Power Cells

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***Abstract* — A CMOS linear PA for IEEE 802.11 b/g applications is implemented in a 0.13 μm process including all matching networks. An adaptive power cell (APC) scheme is proposed to achieve high linear output power and efficiency and applied to the PA, which delivers the output power of 20.5 (19.5) dBm with the PAE of 20.2(17.5)% for an 802.11g modulated signal with the EVMs at -25(-28) dB.**

***Index Terms* — AM to AM, AM to PM, CMOS Power Amplifier (PA), adaptive, error vector magnitude (EVM), linearization, IMD3, WLAN, 802.11 b/g**

I. Introduction

Recently, the increasing need of high-speed wireless data communications is driving the demand for a fully on chip transceiver. Generally, high data rate systems have strict linearity requirements. Therefore, in designing an on-chip transceiver, the CMOS PA is one of the most challenging works because of its linearity issues.

There have been efforts to resolve these issues, and linearization techniques have been reported for high data rate systems [1], [4]. However, these PAs still depend on digital pre-distortion of linearization, which requires additional current consumption, and they have the drawback of design complexity.

In this paper, we introduce a fully integrated CMOS PA for 802.11 b/g applications with adaptive power cells (APCs). This scheme improves the output power at -28 dB EVM by ~4dB with an 802.11g signal, where the output power and PAE are 19.48dBm and 17.5%, respectively.

II. Implementation

A. Adaptive Power Cell

Figure 1 shows the operation principle of the APC scheme. The gates of the CG_2 and CG_3 power cells are biased at 2.9V and 1.9V, respectively, which are lower than the source voltage of the common gate (CG) power cell, V_{CG_SOURCE}, in low powers. Because the CG_2 and CG_3 power cells are biased below the threshold voltage, the CG_2 and CG_3 power cells are turned off and consume no current in low power state. Thus, only the CG_1 power cell, which has a gate bias of 3.6V, works at low powers.

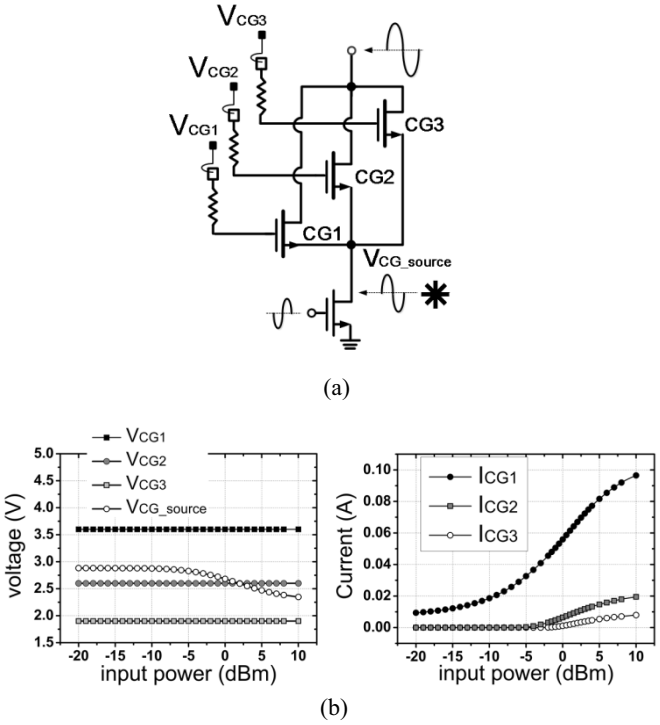


Fig.1.(a) A simplified schematic of the APCs. (b) Voltage and current variations as input power in APCs.

However, with increasing input power, the common gate source voltage, V_{CG_SOURCE}, becomes lower than the gate bias voltage of CG_2. In addition, at high input powers, the gate voltage excursion is large enough to cross over V_{CG_SOURCE}. Thus, the CG_2 and CG_3 power cells are gradually turned on at high powers as shown in Fig 1. (b).

Therefore, the APCs consume less current at low powers and adaptively draw additional currents only at high powers, with which the saturation output power is increased without increasing the quiescent current.

Because of the APC gradually turns on power cells with increasing input power, it modifies the optimal output matching impedance of PAs. The two-one load pull simulations show the output power and IMD_3 contours of the PA with and without APC scheme, respectively, as shown in Fig. 2.

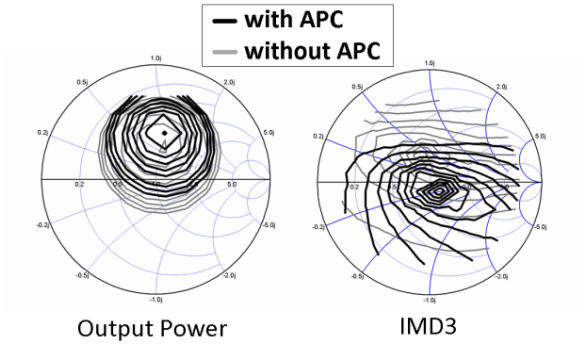
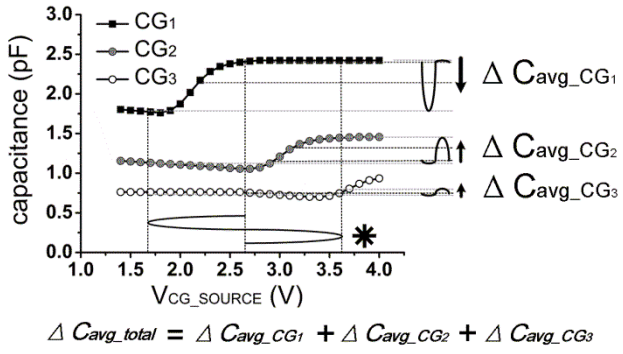
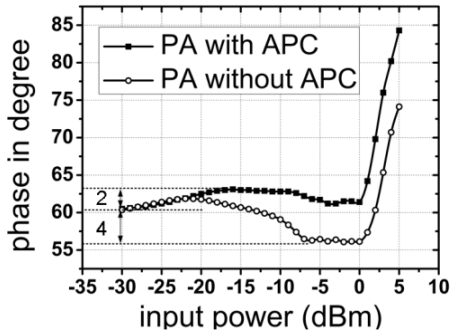


Fig.2. Simulation results of output power and IMD_3 load pull contour in APCs



(a)



(b)

Fig.3. Simulation results of the (a) average capacitance variations and cancellation in APCs (b) AM-PM distortion

The load pull simulations were performed with -5dBm input power for fully matched PAs. To conduct fair comparisons, we tested two PAs at the same current level by adjusting the CG power cell size with respective optimized output matching. The simulation showed that the output power contours almost overlapped at the same impedance in two PAs; however, the IMD_3 contours showed different characteristics. The PA with APCs showed superior 50Ω matching condition than that without APCs.

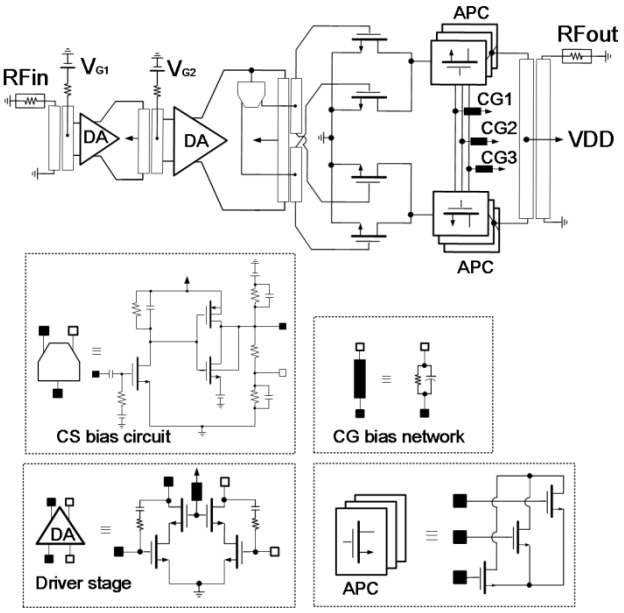


Fig.4. Schematic of the fully integrated APC PA

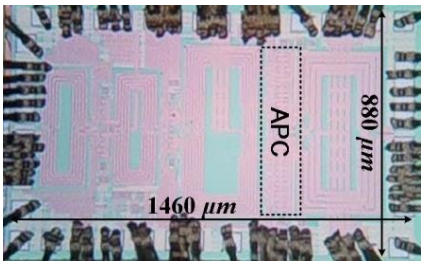
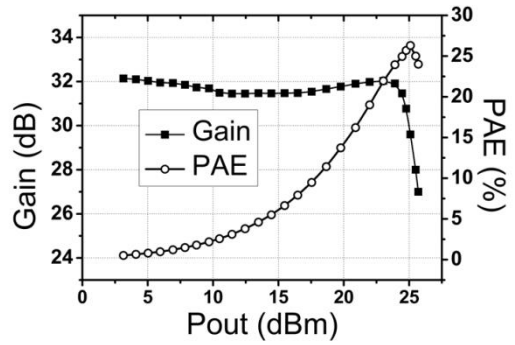


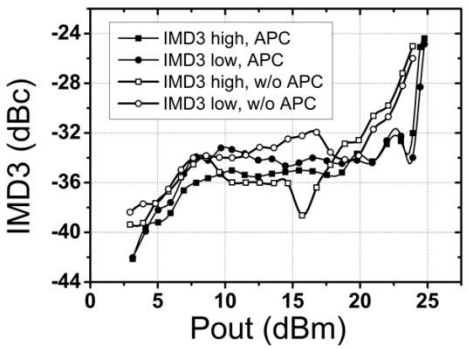
Fig.5. Chip photograph

This indicates that the APC scheme can also contribute to linearization of the PA. The gate widths of the power cells (CG_1, CG_2 and CG_3) used in the APCs are 1440μm, 800μm, and 640μm, respectively. The different gate widths lead to different input capacitances. As the input power increases, V_{CG_SOURCE} gradually decreases; therefore, the CG_1 cell draws more current and goes gradually into the class A bias region. In the same way, CG_2 and CG_3 are in the class B and C bias regions, respectively. Fig. 3.(a) shows how the total average source-gate capacitance of the common gate transistors (APCs) varies in relation to the input voltage. The signal voltage excursion at the source of APCs causes different average capacitance variations in the respective APCs. In CG_1, with increased input, the source voltage excursion reaches the saturated capacitance region at the high end as shown in Fig. 3(a).

Thus, the average input capacitance decreases in the CG_1 power cell. In addition, one can easily understand that a conventional single CG power cell PA usually suffers from a decrease in its average capacitance with the



(a)



(b)

Fig.6. 2-tone measurement results of (a) Gain and PAE (b) IMD_3s with comparison

input power. However, CG power cells of APCs have smaller total input capacitances than a single CG power cell.

Also, the input average capacitance variation of each CG transistor has different signs. As seen in Fig. 3(a), ΔC_{AVG_CG1} varies in the opposite direction to ΔC_{AVG_CG2}, & ΔC_{AVG_CG3} in relation to input voltage; thus, the total average capacitance variation can become small due to mutual cancelling. Since the average capacitance variation mainly causes phase distortion in PAs, the APC PA is expected to have less phase distortion with input power compared to a single CG PA.

The simulation result shows a change of less than 2-degrees with APCs with the input power, while there is a variation of 4-degrees with the optimized single CG PA shown in Fig. 3 (b). As a result, the EVM performance can be improved by using the APC scheme.

B. Design of the CMOS Power Amplifier

Figure 4 shows the schematic of the overall APC PA. In 802.11b/g applications, the power gain of a PA should be considered because the transmitter linearity starts to degrade around -6dBm output power.

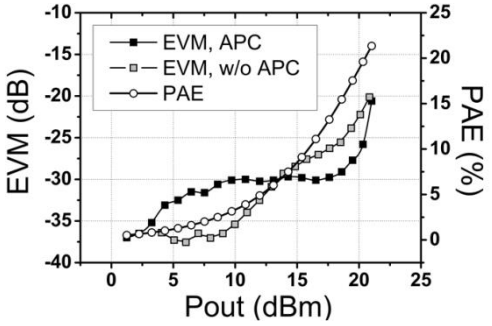
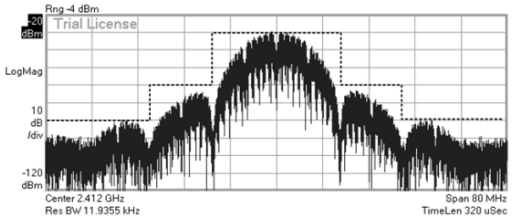
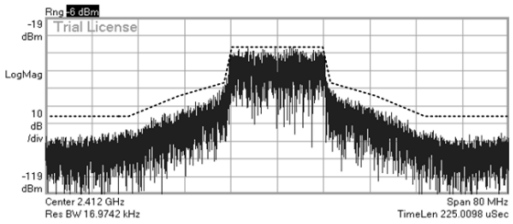


Fig.7. EVM measurement results



(a)



(b)

Fig.8. Measured spectrum of (a) 802.11b and (b) 802.11g

Therefore, to achieve over 20dBm linear output power, a PA should have at least 26dB power gain. We implemented a 3-stage amplifier to obtain sufficient gain.

Each stage covers almost 10dB power gain. To prevent breakdown, 0.35μm thick oxide transistors were used in all CG power cells, and differential structures were adopted to alleviate bond wire effects and increase the power gain. APC linearization was used only in the power stage because the APC scheme works only in large signal regimes.

The APC configuration has a differential structure. To achieve sufficient gain in a differential structure, virtual grounds in the gates of the CG power cells are essential. To optimize the APC performance, the gate width of APCs was carefully chosen. From the input to output of the overall PA, all stages were matched with an on chip transmission line transformer (TLT), which was also used as the VDD and gate bias feeding line. All the TLTs were designed using 3μm copper top metal. The insertion loss of output matching was simulated to be 1.2dB at 2.412GHz.

TABLE I
Performance Comparison of Recently Reported 802.11g PAs

Ref.	Technology	P_{OUT} (dBm)	PAE (%)	Gain (dB)	EVM @P_{OUT}	V_{DD} (V)	Freq. (GHz)	Output matching networks	Characteristic
Afsahi 10 [1]	CMOS 65 *nm*	22.4 (*14)	19.4 (*8)	14	-25 dB	3.3	2.4	On-chip	DPD Offset g_m
Kim 12 [2]	CMOS 0.18 μm	23.5	13	22.5	-25 dB	3.3	2.4	On-chip	PSCT based PA
Onizuka 11 [3]	CMOS 65 *nm*	23.7	7	24	N/A	2.5	2.4	On-chip	AM-PM canceller
Kaymaksut 12 [4]	CMOS 90 *nm*	20.2(*19.3) 16(*11)	24.7(*22.9) 17(*7)	18	-25 dB -28 dB	2	2.4	On-chip	Doherty PA DPD
SKY65131 [6]	InGaP/GaAs HBT	23.5 20.5	21 20.2	26	-25 dB -28 dB	3.3	2.4	On-chip	commercial product
This works	CMOS 0.13 μm	20.5 19.5	20.2 17.5	32	-25 dB -28 dB	3.6	2.4	On-chip	APC

* measured value without digital pre-distortion

III. Measurement Results

A fully integrated RF CMOS PA was fabricated in 0.13μm technology as shown in Fig. 5. The layout size, including pads, is $880\mu m \times 1460\mu m$. Two-tone measurement was performed with 2.422GHz and 2.402GHz.These frequencies were selected because 802.11g source signal has 2.412GHz with a 20MHz bandwidth in channel 1. The power gain was 32dB and the output saturation power was 27dBm with 27% peak PAE as shown in Fig. 6 (a).

In the IMD3 test, the output powers at -30dBc were 24/22.09dBm with the PAEs of 23.9/19.6% in the scheme with/without APCs. This result reflects an improvement of 2dB output power with 4% efficiency with the APC scheme as shown in Fig. 6 (b).

Next, 802.11g tests were performed with OFDM, 64QAM, 54Mbps and 20MHz bandwidth signal source at 2.412GHz. The maximum output powers satisfying the 802.11g linearity specifications with the EVM of -28dB were 19.5/15.8dBm with PAEs of 17.5/9.5% with/without APC as shown in Fig. 7. This result indicates an improvement of 3.7dB output power and 8% PAE with the APC scheme. Also 802.11b tests were performed with DSSS, CCK, and 11Mbps signal source. The maximum output power satisfying the 802.11b linearity specification was 21.9dBm with a PAE of 22.46%. The table I compares the proposed scheme with state-of-the-art CMOS and commercially available InGaP/GaAs 802.11g PAs.

VII. Conclusion

A CMOS linear power amplifier for WLAN 802.11 b/g is presented. We demonstrated linearization techniques using the proposed adaptive power cells. This linearized the PA in terms of IMD_3, AM to PM, and AM to AM. It improves maximum linear power and PAE significantly.

We achieved 20.5 dBm and 20.5 % PAE at -25 dB EVM with 32 dB power gain with 802.11g signal source. The linearity and efficiency are comparable to those of reported InGaP/GaAs based PAs

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