A Fully Integrated 22.6dBm mm-Wave PA in 40nm CMOS

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***Abstract* — A fully integrated 60GHz CMOS PA with a P_{SAT} of 22.6dBm is presented. To our knowledge, this is the highest reported P_{SAT} at mm-waves in standard CMOS. To achieve a high power level, 32 differential PAs are combined through a network of transmission lines, Wilkinson combiners, and a multi-port argyle transformer. This method of combining minimizes loss while implementing a low impedance load (~12Ω) at the drains of each of the last stage PAs. Electromigration and other reliability issues are discussed.**

***Index Terms* — Differential amplifiers, millimeter wave integrated circuits, passive circuits, power amplifiers, transformer.**

I. Introduction

A continuing challenge for radios operating in the 60GHz ISM band or the 71 to 76GHz/81 to 86GHz E-band is that the output power level of the power amplifier limits the radio's functional range. Although other processes like SiGe HBT may be better suited for PA design due to their higher power handling capabilities, standard CMOS is preferred due to lower cost and ease of integration with other RF and digital blocks.

The achievable output power in sub-micron CMOS PAs is limited by reliability concerns. To avoid device breakdown and hot carrier injection, supply voltage has to be kept low resulting in low P_{SAT}. Worse yet, even if operating within the device breakdown limits, the high voltage stress on the transistors of the last stages in a PA chain can result in a gradual drop in gain and/or P_{SAT}. To mitigate metal electromigration concerns, thick top metals and wide V_{DD} and GND traces (sometimes both in the same layer) are employed but the resulting geometries make achievable performance strongly dependent on the floor plan.

Power combining techniques have achieved P_{SAT} levels of 17 to 20dBm at mm-waves in standard CMOS processes [1]–[3]. However, conventional power combining approaches (e.g., solely combining with Wilkinson combiners) suffer from both the loss in combiners (0.6 to 1.5dB per stage) and significant interconnect loss (0.7 to 1dB per mm) between the output nodes. In-air power combining using antenna arrays can avoid combiner in some cases [4]. However, this method may not be applicable in emerging applications that employ a single-feed high-gain radiator such as a reflector antenna (e.g., PtP wireless backhaul).

The fully integrated CMOS PA presented here achieves the highest reported P_{SAT} by combining the outputs of eight PA chains through a combination of transmission lines (TL), Wilkinson combiners, and multi-port argyle transformer (Fig. 1). The PA is designed in 40nm CMOS with 6 metal layers (UTM6) and an ultra-thick RDL layer.

II. Architecture

A schematic of the individual PA chains is shown in Fig. 2 (see Fig. 4, Cell B2 also). Four PA stages, each employing common source differential pairs with neutralizers, are cascaded via transformers. A parallel RC structure stabilizes the PA. Stage 2 and 3 employ transformers with two pairs of input and two pairs of output differential nodes (Fig. 2.) This divides the total voltage swing between 4 sets of transistors instead of two sets if conventional transformer coupling were employed. Consequently, the swing on the drains and gates of each transistor is reduced thereby enhancing lifetime reliability.

Each of the 4th stage transformers converts a 50Ω differential output to two pairs of 25Ω differential nodes at the drains of the last stage PAs. The low impedance seen by each differential pair (25Ω differential) alleviates the voltage stress on the drain of each device. These argyle-shaped transformers also reduce the routing length (and thus the parasitic inductance) between the transformers and the drains of the differential pairs. They also enable a tile-based placement of bypass capacitors between V_{DD} and GND on each side of the transformer, resulting in an efficient allocation of space between transformers, transistors, bypass capacitors and V_{DD} and GND routing.

A schematic of the 8-way output combiner is shown in Fig. 2 (see also Fig. 4, Cells C-D-E: 2-5). It combines the outputs of 8 pairs of differential nodes and delivers power to a 50Ω-SE output with just 3dB loss. The outputs of each pair of PA chains are combined through a compact implementation of a Wilkinson combiner with two 50Ω inputs and a 50Ω output. A pair of 50Ω differential coplanar TLs follow the combiners and are connected in parallel at the inputs of the final transformer (Fig. 4, Cell D3 & D4). The coplanar TLs combine the output power of the Wilkinson combiners with low loss (<0.6dB) and

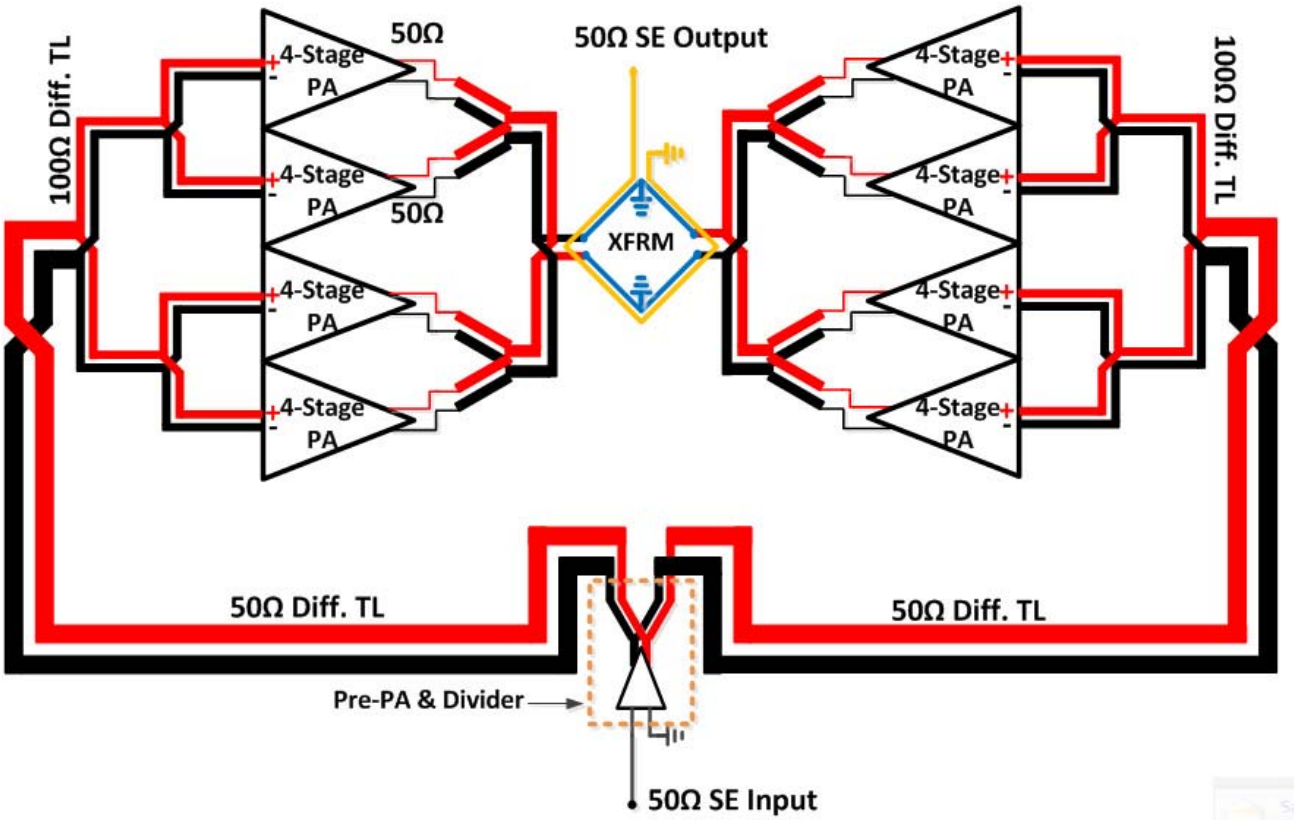

Fig. 1. Block diagram of the fully integrated 60GHz PA.

provide a 50Ω to 25Ω impedance transformation. The argyle transformer that follows the TLs performs three tasks with 1.5dB loss. It combines two pairs of differential nodes, implements a 25Ω to 50Ω impedance transformation, and transforms differential input signals to a single-ended output. Grounding the mid-points of the input loops enhances differential behavior of the transformer.

The 8-way combiner needs to maintain the same impedance level (50Ω) at the inputs (for proper loading of each pairs of PA chains) and the output (for impedance matching to the antenna) with low loss. This is challenging since each parallel combination divides the impedance by two and each series combination multiples it by two. Conventional combining approaches would have required additional stage(s) of transformation and suffer from extra loss.

In the process used for this design, M6 is the only layer that can handle a reasonable current density (~34mA/μm at 110^0C compared with 12.6mA/μm of UTRDL). Due to this, both V_{DD} and GND routings are implemented in M6. An M6 V_{DD} line goes through each stack of PAs. It is wider in the final stages (10μm) and narrower at the initial stages (8μm), and is capable of handling 340mA at 110^0C without significant degradation over 10-year/100% operation.

The input power is delivered to the PA stacks through two branches of 50Ω differential coplanar lines on each side of the input pad. Each branch is divided into two 100Ω TLs connected in parallel as shown in Fig. 1 (see also Fig. 4, Cells A3 and A4). Each 100Ω line is further divided into two differential TLs.

Although realizing a 200Ω-TL is impractical in silicon, the length of the last-stage TL is small and thus does not result in significant impedance mismatch. To compensate for the insertion loss of the TL divider network (~3.7dB), a pre-PA is added between the Wilkinson divider and the input GSG pad (Fig. 1 and 2). A 1:2 transformer is used to match the input of the first amplifying stage to a 50Ω-SE probe. As shown in Fig. 3, return loss at the input (S11) is better than –10dB across the 60GHz band. S22 is well matched from 50GHz to beyond 67GHz.

III. Measurement Results

Fig. 5 shows P_{OUT} vs. P_{IN} of the PA at 60GHz with a V_{DD} of 1.2V. The graph is obtained by driving the PA with a mm-wave signal generator and measuring the output power by a mm-wave power meter.

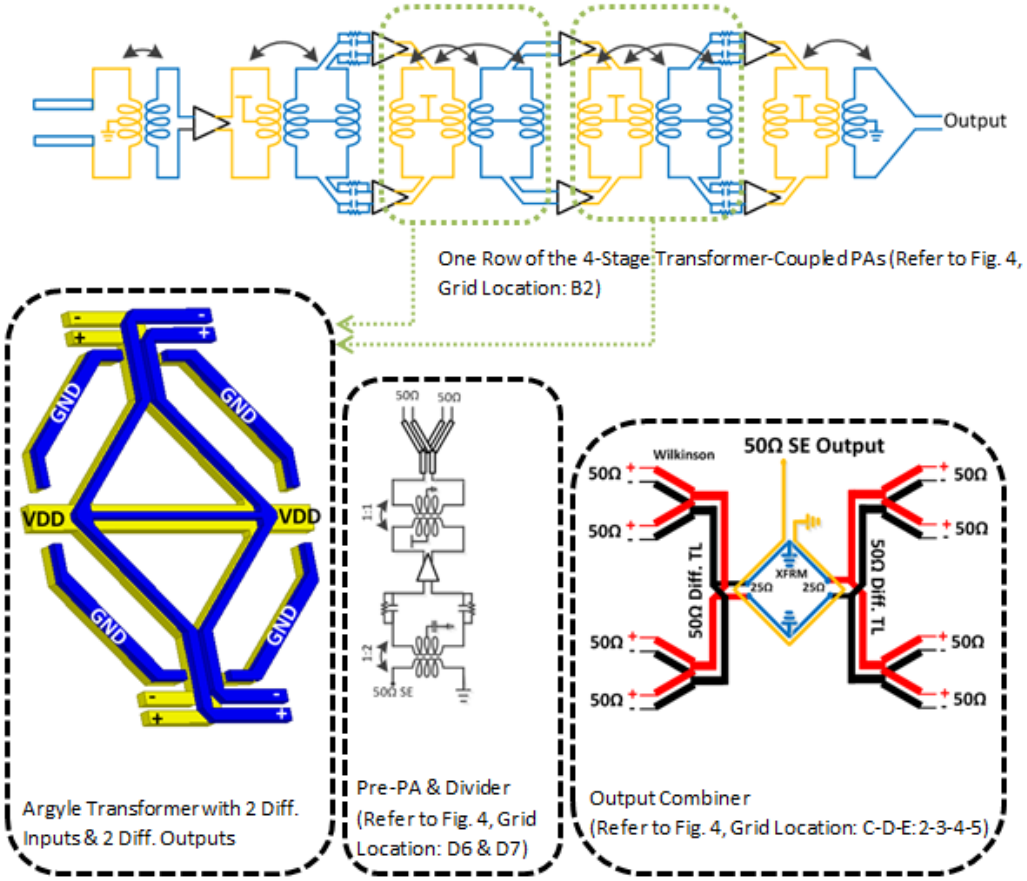

Fig. 2. Sub-blocks of the PA.

The loss of the cables and GSG probes are de-embedded by measuring an on-wafer thru GSG structure. The PA has a gain of about 30dB with an estimated measurement accuracy of 1dB. OP1dB is 17dBm at 60GHz.

Fig. 6 shows P_{SAT} and maximum PAE versus both frequency and V_{DD}. Biasing of the differential pairs is adjusted for each supply level to achieve the highest P_{SAT} for the given V_{DD}. The IR drop of the DC probes is de-embedded by monitoring the voltage difference between a V_{DD} and a GND pin. With a V_{DD} of 1.2V, the PA achieves a P_{SAT} of 22.6dBm at 60GHz with less than 1dB variation across the band; PAE peaks at 7% at 59GHz. Efficiency can improve by 1% to 2% with wider V_{DD} and GND routings between DC probes and the center of the chip (Fig. 4, cells A7 & B7) where V_{DD} is fed to the PA chains. In an actual product a large number of DC bumps that distribute the supply current more evenly would reduce the IR drop. When operating with a reduced 0.7V supply, this design achieves a P_{SAT} of 17dBm. This high level of mm-wave P_{SAT} on even a low V_{DD} indicates that the proposed architecture can also be utilized in more refined CMOS processes such as 28nm CMOS that use a lower supply voltage.

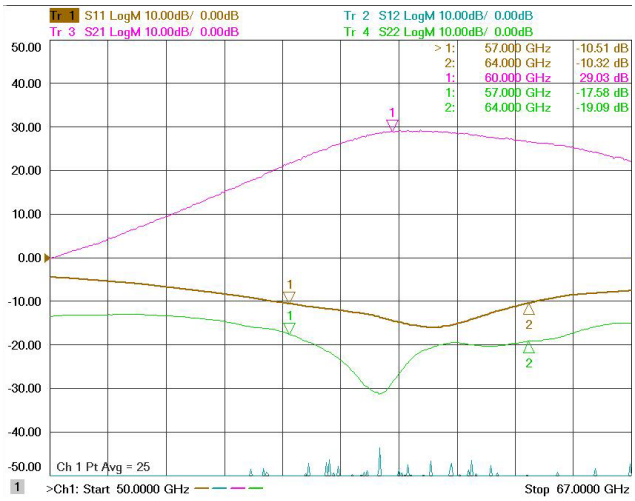

Fig. 3. Measured S-parameters of the entire PA

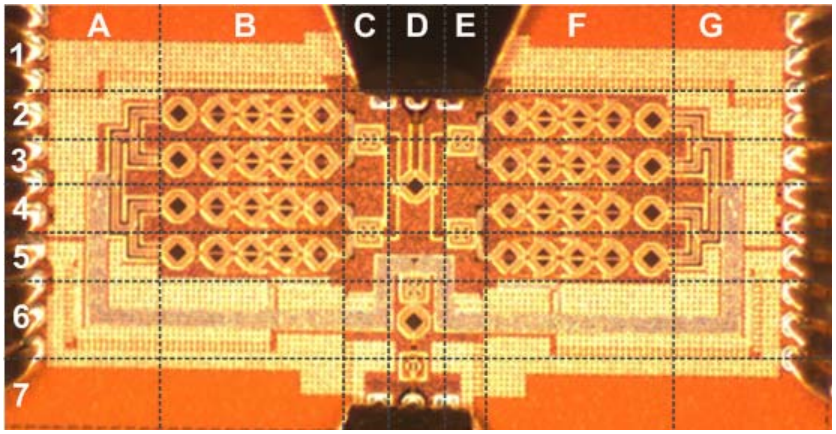

Fig. 4: Die Photo

TABLE I. COMPARISON OF STATE-OF-THE-ART MM-WAVE CMOS POWER AMPLIFIERS

	This Work	**[1]**	**[2]**	**[3]**
Technology	40nm CMOS	90nm CMOS	65nm CMOS	65nm CMOS
Supply V/I/P	1.2V/2.03A/2.44W	1.2V	1V	1V
S21[dB] @ 60GHz	29dB	20.6dB	20.3dB	19.2dB
OP1dB @ 60GHz	17dBm	18.2	15dBm	15.1dBm
P_{SAT}	22.6dBm	19.9	18.6	17.7dBm
PAE @ P_{SAT}	7%	14.2%	15.1%	11.1%
Area	2.16mm^2 [1x2.16mm]	1.76mm^2 [1.85x0.95mm]	0.28mm^2	0.83mm^2

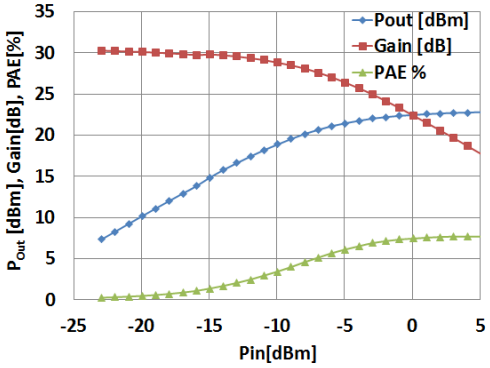

Fig. 5. Measured PA P_{OUT}, Gain and PAE vs. P_{IN} at 60GHz (V_{DD} =1.2V).

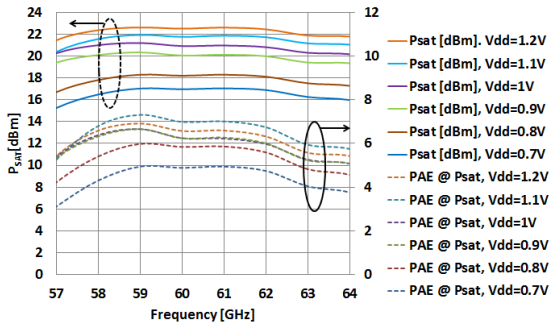

Fig. 6. Measured P_{SAT} and Max PAE vs. Frequency and V_{DD}.

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