A Multichannel, Multicore mm-Wave Clustered VCO with Phase Noise, Tuning Range, and Lifetime Reliability Enhancements

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***Abstract* — Clustering and multi-core transformer coupling techniques are presented to improve phase noise, tuning range, and reliability of a mm-wave VCO. A proof-of-concept design targeting the WiGig protocol is shown. Each cluster of VCOs covers one channel resulting in better phase noise performance. Multicores of VCOs with uncorrelated noise are combined using transformers to further enhance phase noise and combat the voltage swing reliability issues. Furthermore, due to realization of multiple inductive elements in parallel instead of one small inductor, this approach bypasses Q-degradation of small inductors (<50pH). The VCO achieves a phase noise of -101.8dBc/Hz at 1MHz offset with over 12.6% tuning range (50.7GHz to 57.5GHz) and an FOM of -183dB/Hz.**

***Index Terms* — integrated circuit reliability, millimeter wave integrated circuits, phase noise, tuning, voltage-controlled oscillators.**

I. Introduction

Demand for wireless links capable of handling Gigabits-per-second data transmission continues to drive new generations of wireless protocols that use more complex data modulation schemes. Protocols like IEEE 802.11ac/ad and E-band PtP wireless backhaul require oscillators with excellent phase noise and a reasonable tuning range. These requirements exceed the performance of conventional LC oscillators. New approaches such as multiport inductors [1] and multi-turn magnets [2] provide a reasonable solution in the phase noise, frequency tuning range, and power consumption design space.

The fundamental challenges in LC-oscillators at RF and mm-waves are still present and multifold. To get the roughly 5% to 10% tuning range needed in most applications, the ratio of the varactors or capacitor arrays to the capacitance of negative-gm structure has to be significant. The large varactor limits the effective Q and degrades the phase noise quadratically. Furthermore, as the effective capacitance at the cross-coupled nodes increases, the resonance inductor becomes smaller and its Q would drop because the parasitics become more significant. As explained later, the proposed approach bypasses this Q-degradation by placing multiple inductors in parallel. The conventional approach to get better phase noise is to increase the current and thus the voltage swing in a single VCO core. The voltage swing, however, is bounded by the device breakdown voltage limits which also set the maximum current for a given effective resistance. This issue becomes a more restrictive design challenge with technology scaling due to the lower breakdown voltage of more refined processes.

To address these intertwined issues, a clustered transformer-coupled multicore VCO design technique is proposed. An implementation is presented in a 40nm CMOS process as a proof-of-concept for the WiGig protocol (Fig. 1). The design targets four channels of the WiGig protocol, minus an LO of 8GHz. The clustered design relaxes the tuning requirements of each cluster while the transformer coupled multicore VCO design realizes low phase noise and insensitivity to the external load.

II. Architecture

1. Clustering

In the proposed quad-cluster topology, each cluster covers one target channel. The four clusters are connected in parallel using an H-shaped 100Ω differential coplanar transmission line (TL) with a GSSG pad tied to its center point. The H-shaped figure makes the design symmetrical and facilitates good floor-planning (Fig. 4). The desired cluster is activated by digital control switches while other clusters are turned OFF.

Splitting the VCO into clusters limits the tuning range requirement for each cluster to a few hundred megahertz at mm-waves and thus eliminates the need for large varactors or capacitor arrays. Using a quad-core transformer-coupled VCO reduces the sensitivity of the ON VCO cluster to the load presented by the OFF clusters and by the gates of the buffer (Fig. 1). The clusters can be connected in parallel with TLs without performance degradation. This architectural advantage also eliminates a mm-wave frequency multiplexer that is needed in systems with multiple VCOs.

Fine-tuning for each cluster is achieved using NMOS varactors which provide more than 550MHz of continuous analog tuning for each channel. This range is sufficient for calibration and frequency locking in a PLL system.

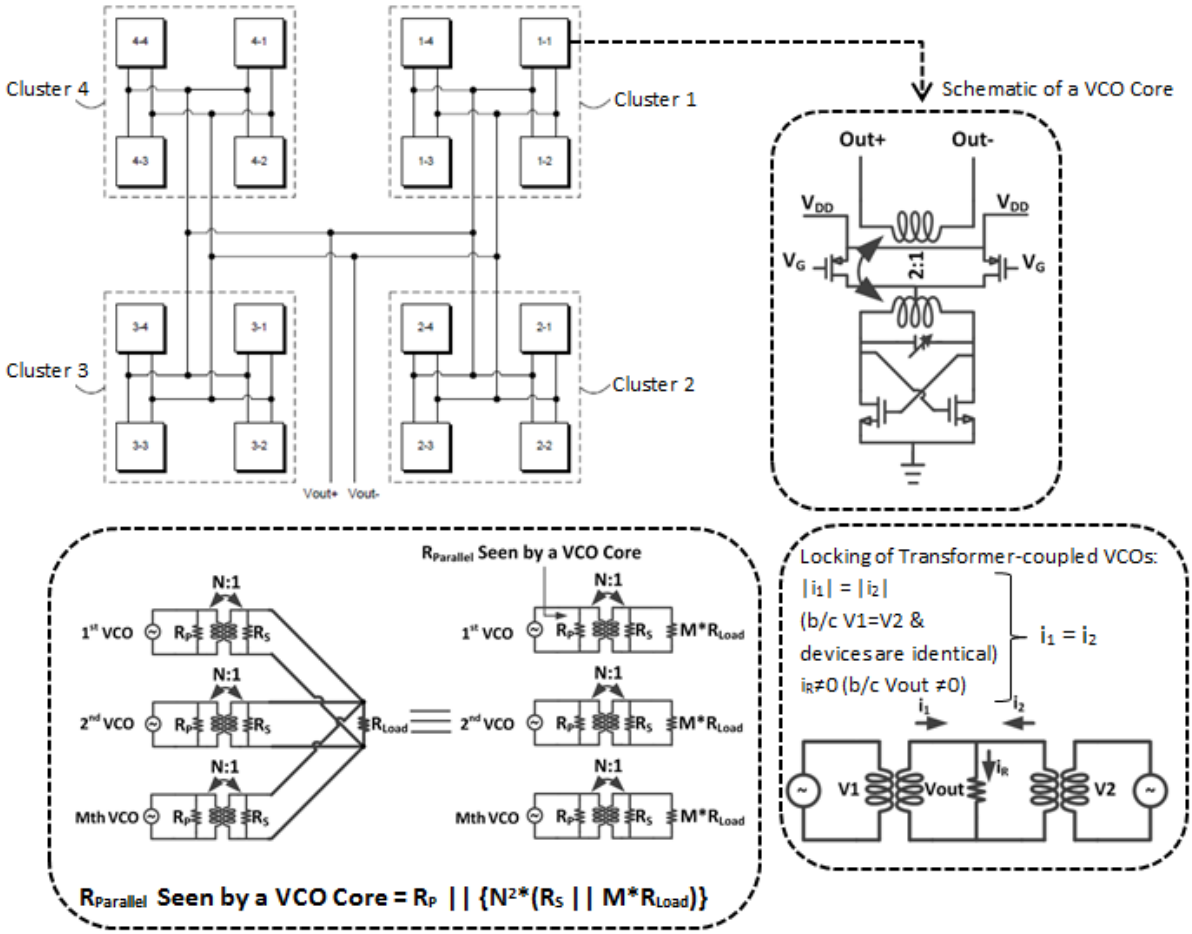

Fig. 1. Schematic view of the clustered VCO.

2. Transformer coupled multi-core VCO

Each cluster contains four identical VCO cores connected by the aforementioned H-shaped differential coplanar TLs. Each VCO core consists of an NMOS cross-coupled pair, a 2:1 transformer, and two identical PMOS current sources placed on each side of transformer's center tap. The proposed combination boosts the load impedance seen by each cross-coupled pair in two ways.

First, coupling M VCOs improves the impedance due to the replica-loading Q enhancement effect (Fig. 1). If the number of VCOs is doubled, R_{Load} seen by each VCO due to the external load is doubled. Second, the transformer provides further impedance transformation. As depicted in Fig. 1, the effective $R_{Parallel}$ seen by each VCO is N^2xM, where N is the turn ratio of the transformer and M is the number of coupled VCOs (assuming ideal transformers). Consequently, Q-degradation of the LC tanks due to the external load is minimal. Furthermore, having multiple cores in parallel improves the phase noise due to uncorrelated nature of device noise.

This approach also addresses the voltage swing reliability issues by combining the current of multiple VCO cores in parallel. This allows for the scaling of power without violating voltage swing constraints. The design achieves –101.8dBc/Hz at 1MHz offset with over 12% of tuning range.

Note that the cores in a multicore VCO will lock in phase if there is a finite external load across the differential output nodes. Consider the two-core case. Establishing a voltage swing across the load (and oscillation in the VCO) requires a current to pass through R_{Load} ($I_R \neq 0$). In the absence of mismatches, two identical VCO cores connected in parallel experience the same voltage swing and must have the same current magnitudes (Fig. 1). This implies that the current through the load can only be applied as the summation of two in-phase currents induced by the VCOs. (If the currents were out-of-phase, there would be no current through the load and zero voltage swing; however, we assume that the VCOs are designed with enough negative-gm to compensate for the loss of the load.) In practice, to ensure functionality in the

TABLE I. PERFORMANCE COMPARISON OF CLUSTERED VCO FOR DIFFERENT CONFIGURATIONS

Config.		Measurement Results				Simulation Results		
CH	# of Cores ON	Freq. [GHz]	PN @ 1 MHz	PN @ 30 MHz	FOM	Freq [GHz]	PN @ 1MHz	PN @ 30MHz
1	4	50.72	–101.8	–132.1	–182.1	50.55	-102.2	-132.2
1	3	51.15	–101	–132.2	–182.6	51.14	-101.6	-130.2
1	2	52.01	–99.5	–129.6	–183.0	52.0	-97.2	-127
1	1	54.98	–86.5	–117.1	–173.5	54.75	-87.5	-117
2	4	52.8	–99.7	–131.9	–180.4	52.48	-100.3	-130.5
3	4	55.46	–98.2	–131.1	–179.3	54.52	-99.6	-130.3
4	4	57.45	–97.3	–130	–178.1	57.51	-98.9	-128.8

presence of mismatch between the VCO cores, R_{Load} should be chosen such that a small delta in the induced currents from the VCOs going through the load does not produce a large enough swing that is comparable to the VCO swing. Similar arguments can be applied when more than two cores are combined.

III. Simulation and Measurement Results

Fig. 6 shows the measurement setup. Testing was done cluster-wise by turning each cluster ON/OFF independently using DC needles. Furthermore, each core of cluster one could be turned ON/OFF, resulting in 15 different configurations for channel 1. Phase noise of each configuration is measured by an Agilent E5502B Signal Source Analyzer connected to an Agilent E5053A downconverter and two external mixers which downconvert the mm-wave frequency to the operating range of the signal source analyzer. Fig. 3 shows the phase noise graphs obtained from different configurations of channel 1. With only a single VCO of cluster 1 turned ON, the phase noise is –86dBc/Hz at 1MHz offset. By turning two cores ON, the phase noise is improved significantly. This is primarily due to two reasons.

With two cores ON, the effective $R_{Parallel}$ of the tank improves, which results in a quadratic improvement in the phase noise due to replica-loading Q-enhancement. Additionally, the correlated oscillation generated by enabling multiple VCOs in the cluster reduces the impact of uncorrelated noise signals. As more cores turn ON, the oscillation frequency shifts down due to the change in capacitance of the cross-coupled pairs. The best phase noise is achieved when all four VCOs are ON as expected. This configuration achieves a PN value of –101.8dBc/Hz at 1MHz offset with an oscillation frequency of 50.72GHz and an FOM of -182.1dB/Hz. The phase noise and oscillation frequency for different configurations are listed in Table I. Table II compares the proposed VCO's performance with the state-of-the-art mm-wave VCOs. The proposed clustered, transformed coupled multi-core VCO achieves the lowest phase noise and best FOM without sacrificing frequency tuning range.

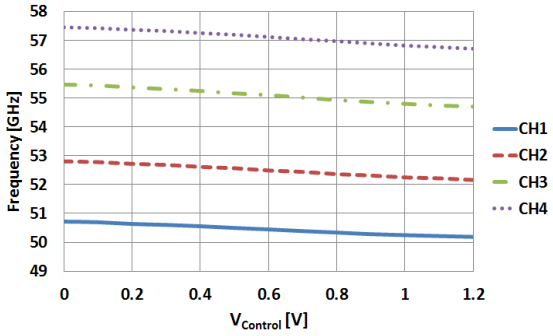

Fig. 2. Measured VCO frequency tuning range in quad-core operation mode.

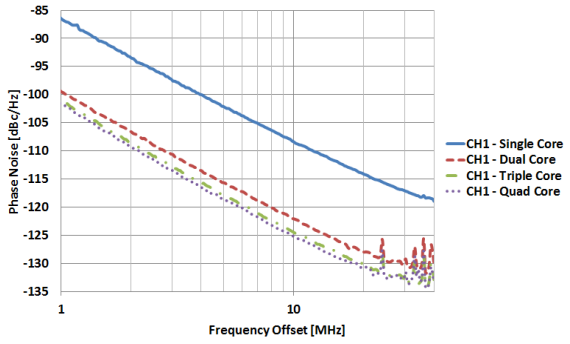

Fig. 3. Measured phase noise for CH1 configurations.

TABLE II. OVERVIEW OF STATE-OF-THE-ART MM-WAVE CMOS VCOS.

	This Work	[2] (QVCO)	[3]	[4] (QVCO)	[5]
Technology	40nm CMOS	65nm CMOS	90nm CMOS	90nm CMOS	65nm CMOS
Frequency [GHz]	50.7 to > 57.5	56 to 60.5	53.2 to 58.4	48.2 to 51.7	34 to 40
Tuning Range [%]	>12.6%	7.7%	9.3%	7%	15.1%
PN @ 1 MHz	–101.8	–97	-91	-87	-98.1
P_{DC} [mW]	24	22	8.1	22.7	14.4
FOM [dB/Hz]*	–182.1	–179	-176.7	-167.4	-178.5
Area	0.33mm2	0.075 mm2	0.077mm2	N/A	0.15mm2

$* FOM = L(\Delta\omega) - 20 \times \log(\frac{\omega_0}{\Delta\omega}) + 10 \times \log(\frac{P_{DC}}{1mW})$

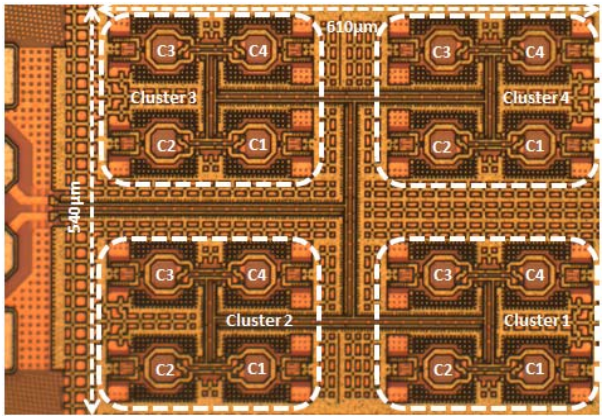

Fig. 4. Die Photo.

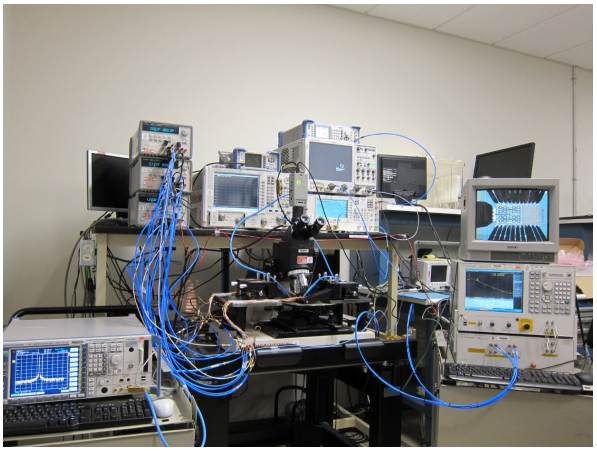

Fig. 5, Measurement Setup.

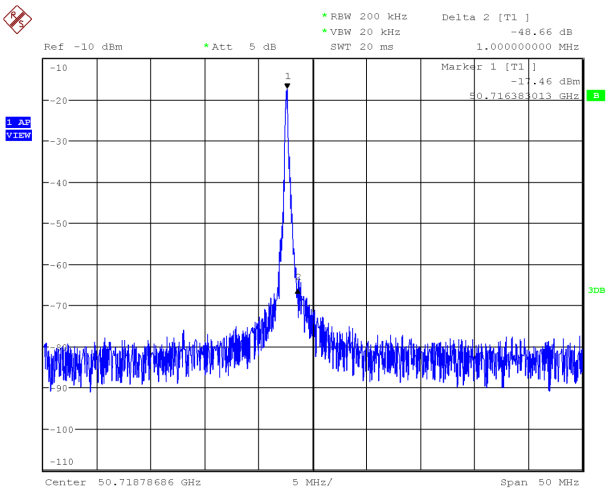

Fig. 6. Spectrum of CH1 with four cores ON.

REFERENCES

[1] Zhiming Deng; Niknejad, A.M.; "A 4-Port-Inductor-Based VCO Coupling Method for Phase Noise Reduction," *Solid-State Circuits, IEEE Journal of*, Vol. 46, No. 8, pp.1772-1781, Aug. 2011.

[2] Decanis, U.; Ghilioni, A.; Monaco, E.; Mazzanti, A.; Svelto, F.; , "A mm-Wave Quadrature VCO Based on Magnetically Coupled Resonators," *Solid-State Circuits Conference Digest of Technical Papers (ISSCC),2011 IEEE International*, pp. 280-282, 20-24, Feb. 2011.

[3] L. Li, et al., "Design and Analysis of a 90nm mm-Wave Oscillator Using Inductive-Division LC tank," IEEE J. Solid State Circuits, vol. 44, no. 7, pp. 1950-1958, Jul. 2009.

[4] K. Scheir, S. Bronckers, J. Borremans, P. Wambacq, Y. Rolain, "A 52GHz phased-array receiver frontend in 90nm digital CMOS," IEEE ISSCC Dig., pp. 184-185, Feb. 2008.

[5] Nariman, M.; Rofougaran, R.; De Flaviis, F.; "A switched-capacitor mm-wave VCO in 65nm digital CMOS," *Radio Frequency Integrated Circuits Symposium (RFIC), 2010 IEEE*, pp.157-160, 23-25 May 2010