Analysis, Design and Implementation of mm-Wave SiGe Stacked Class-E Power Amplifiers

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***Abstract*—Design equations and performance limits of stacked Class-E power amplifiers at mm-waves, including the limitations imposed by device parasitics, are presented in this paper. As a proof of concept of this parasitic aware mm-wave Class-E design methodology and to demonstrate the beyond BVCEO Class-E operation in a stacked architecture at mm-wave frequencies, a Q-band, single ended, two-stage, double-stacked, Class-E power amplifier is designed in a 0.13 μm SiGe HBT BiCMOS process. The measured performance of the fabricated chip show 23.4 dBm maximum output power at 34.9% peak power added efficiency (PAE), and 14.6 dB of power gain across 5 GHz centered around 41 GHz for a supply voltage of 4 V. The total chip area including the pads is 0.8 mm $\times$ 1.28 mm.**

***Index Terms*—Power Amplifier (PA) , silicon germanium (SiGe) HBT, millimeter-wave, BVCEO, Q-band, Class-E .**

I. Introduction

The low breakdown voltage of nano-scaled silicon transistors with f_T and f_{max} of above 200 GHz limits the maximum output power that can be generated from a single device. Series stacking of multiple transistors increases the allowable output voltage swing and power for a given load impedance, at the cost of lower PAE due to higher series resistance loss and intermediate node parasitic capacitances [1]-[3]. Mm-wave power amplifier design using Class-E architecture is an attractive proposition due to high theoretical collector efficiency as well as higher allowable voltage swing due to non-overlapping voltage and current waveforms. Specifically, in HBTs the voltage swing can be as high as BVCBO as opposed to BVCEO that sets the limit in linear amplifiers [4]. However, in practice, maintaining the non-overlapping Class-E voltage and current waveforms at mm-waves both in simple and stacked Class-E amplifiers, is a major challenge in presence of device and layout parasitics. While mm-wave stacked amplifiers using FETs are reported [1]-[3], this paper demonstrates the first stacked HBT amplifier at mm-waves in a Class-E operation. The parasitic-aware mm-wave Class-E PA design methodology is covered in Section II. This analysis is extended to stacked mm-wave Class-E designs in Section III. As a proof of concept, a double-stacked Class-E power amplifier is implemented and the measurement results are shown in Section IV.

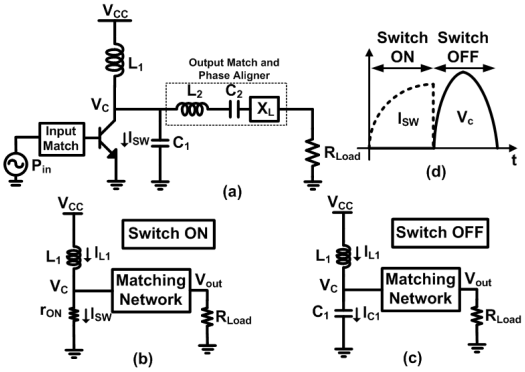

Fig. 1. Generic switch model Class-E power amplifier schematic.

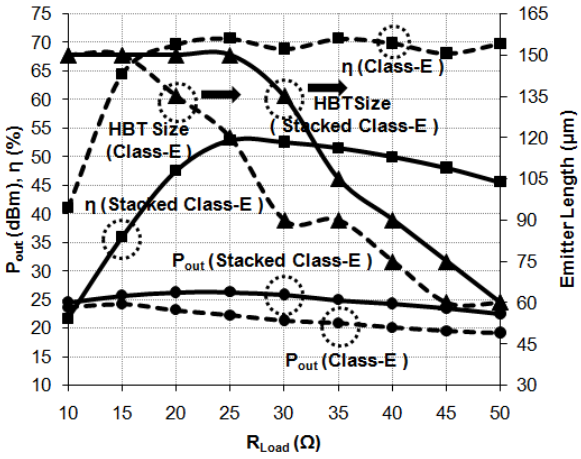

Fig. 2. Simulated maximum achievable efficiency in Class-E and double-stacked Class-E at 45 GHz for real HBT models and lossless passives versus the load resistance and the corresponding device size.

Section V concludes the paper.

II. Mm-Wave Class-E Design Methodology

Analysis of the generic Class-E power amplifier topology (Fig. 1) based on an ideal/non-ideal switch model [5] is not necessarily applicable to mm-wave SiGe HBT designs due to large non-linear device collector capacitance, base to collector capacitor, and the inability of HBTs to perform as an ideal ON/OFF switch unlike

FETs. Low frequency Class-E amplifier designs usually involve choosing the the supply voltage V_{CC} such that the peak collector voltage, $V_{C_{MAX}}$ is less than transistor's breakdown voltage, $V_{Breakdown}$ in order to obtain maximum output power. With V_{CC} fixed, the output power is determined by the load resistance, R_{Load}, and the output passives (L_1, C_1) [5]. R_{Load} also determines the maximum current needed to be supplied by the device which determines the device size that now must be chosen so that it can supply the current required for proper Class-E operation. In mm-wave designs, however, the capacitance C_1 is entirely realized from the device output capacitance which places another requirement on the device sizing. Satisfying both requirements is possible only within a certain range of load impedance as shown in Fig. 2. Lower than optimal R_{Load} leads to efficiency degradation due to excess parasitic capacitance, while higher than optimal R_{Load} leads to lower output power. Assuming Class-E operation, the maximum achievable collector efficiency limited by the finite ON-resistance of the devices, r_{ON}, is analytically shown to be

$$\eta_{\,Maximum} = 1 - \frac{\omega}{\omega_{switch}} * \chi\,, \qquad (1)$$

where ω is the frequency of operation, C_{OFF} is the collector capacitance when the transistor is OFF, and $\omega_{switch} = 1/(r_{ON} * C_{OFF})$ is constant across different device sizes for a given technology and χ is a fixed value under maximum output power condition in a Class-E architecture. In the 0.13 μm IBM8HP process, from simulations, ω_{switch} is determined to be 9.11×10^{12} radians/sec corresponding to a theoretical peak achievable collector efficiency of 87.5% at 45 GHz for the typical Class-E topology.

III. Mm-Wave Stacked Class-E Design

In this work (Fig. 3), a double-stacked Class-E PA in a low resistive bulk SiGe HBT BiCMOS process, with each series stacked HBT device operating in beyond BVCEO mode [4], has been realized to achieve higher voltage swing and output power while maintaining high efficiency at mm-waves. In the double-stacked Class-E amplifier, the active devices in series (Q_1 and Q_2) are designed to turn ON and OFF simultaneously (Fig. 4). This ensures that the voltage swing across the transistors add up in phase leading to larger overall output voltage swing and power delivered to a fixed load. Ideally, the dynamic voltage swing must be equally divided amongst all the series stacked HBTs to avoid stressing any single HBT. In stacked switching amplifiers, the voltage division mechanism differs in the ON and OFF states. When the switching HBTs are ON, the ratio of the device ON-resistances, r_{ON1}/r_{ON2}, determines the voltage division.

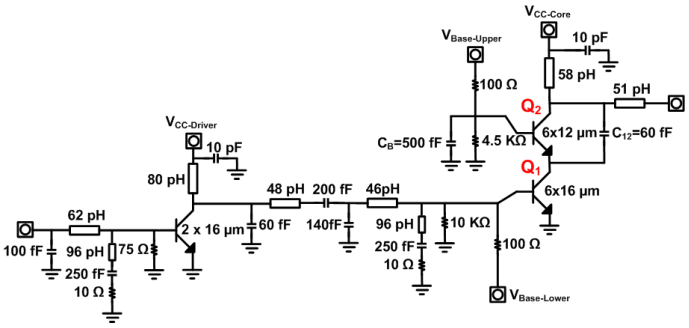

Fig. 3. Q-band SiGe HBT double-stacked Class-E PA schematic.

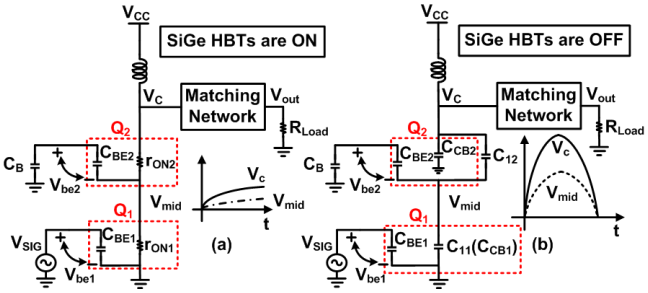

Fig. 4. Series stacking of SiGe HBTs in a Class-E amplifier architecture when (a) HBTs are ON, (b) HBTs are OFF.

In the OFF state, a capacitive ladder network is used for voltage division in the intermediate node. For mm-wave Class-E design, the bottom capacitor, (C_{11}), of the ladder network is realized mostly by the intrinsic collector to bulk capacitance of Q_1, C_{CB1}, which makes sizing of Q_1 a design parameter while the capacitor C_{12} is realized by an explicit Metal-Insulator-Metal (MIM) capacitor. The base terminal of Q_2 is terminated with the capacitance C_B whose value depends on the base-emitter capacitance C_{BE2} of the stacked transistor Q_2. The $C_{BE2} - C_B$ capacitive divider ensures (1) the base terminal of Q_2 swings up along with its collector in the dynamic operation; thus, preventing collector-base junction breakdown, (2) the base-emitter voltage of Q_2, V_{BE2}, swings up and down in phase with the input signal applied to the base of the driving transistor, Q_1; thus, ensuring synchronous switching of the stacked devices.

A simplified analysis of a double stacked Class-E design predicts a 6 dB increase in output power for the same maximum collector efficiency than that of a non-stacked Class-E amplifier. However, mm-wave stacked PA designs fail to reach this output power due to the parasitic collector bulk capacitance of the top transistor as well as lower than expected swing of the bottom device. In addition, meeting both capacitance and device current requirements for Q_1 become more difficult in stacked designs due to voltage scaling. The collector-bulk parasitic capacitance of Q_2, C_{CB2}, forces the design to operate under non-Zero

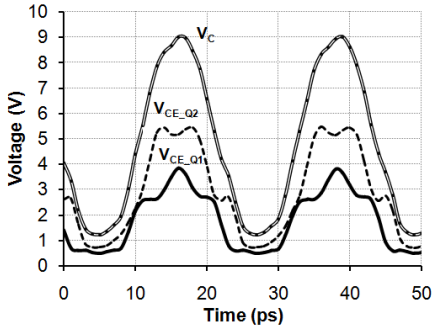

Fig. 5. Simulated transient voltage waveforms.

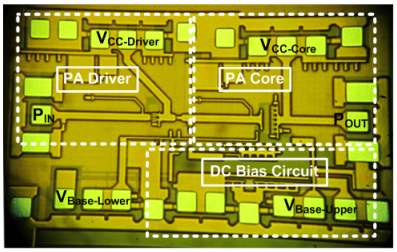

Fig. 6. The chip microphotograph.

Voltage Switching (ZVS) conditions, which reduces the output power to 87% of its theoretical 6 dB improvement. The base capacitance, C_B, designed to ensure synchronous switching of Q_2, also loads the middle node, resulting in lower voltage swing across the bottom device, and hence, a lower overall voltage swing across the load (Fig. 5). It can be shown analytically that the output power and maximum achievable collector efficiency of the double-stacked Class-E design approximate to

$$P_{out} = 0.87[\frac{2 + \frac{C_B C_{BE2}}{2C_{12}(C_B + C_{BE2})}}{1 + \frac{C_B C_{BE2}}{2C_{12}(C_B + C_{BE2})}}]^2 P_{out\ Class-E}\ , \quad (2)$$

and

$$\eta_{\ Maximum} = 1 - 2\frac{\omega}{\omega_{switch}} * \chi\ . \quad (3)$$

At 45 GHz, using the 0.13 μm SiGe HBT BiCMOS process, when C_B is designed to ensure the base voltage of Q_2 swings half that of V_{mid}, stacked Class-E output power scales 3.5 dB over a simple Class-E design with 75% maximum theoretical achievable collector efficiency. In comparison, on-chip passive power combining of two non-stacked Class E power amplifiers increases the output power by around 2.5 dB with a power combining efficiency of 85% [6]. The efficiency degradation using real transistor models with all parasitics between a simple Class-E and a stacked design can be seen from Fig. 2. Lower achievable efficiency compared to the theoretical predictions is due to violating Class-E ZVS conditions as explained before.

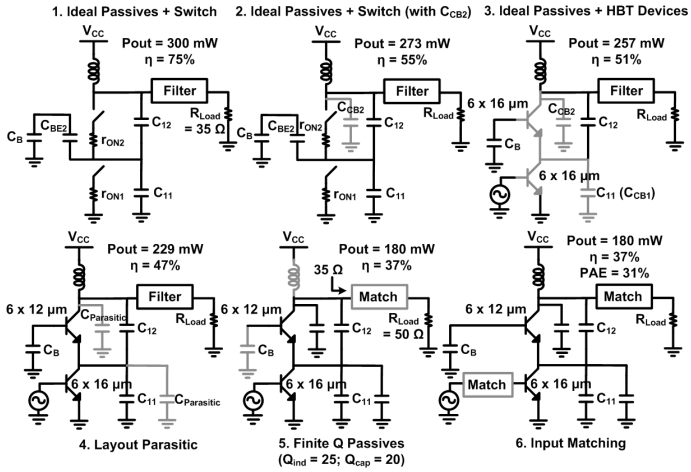

Fig. 7. Design steps of double-stacked Class-E HBT PA.

IV. Implementation and Measurement Results

To demonstrate the aforementioned methodology, a two-stage double stacked Q-band Class-E power amplifier is designed in the IBM 8HP technology offering 7 metal layers (Fig. 6). Based on Fig. 2, Q_1 is realized as a parallel combination of 6 HBTs, each with emitter length of 16 μm. Ideally Q_1 and Q_2 should be of the same size to handle the switch ON current. However, to reduce the effect of C_{CB2}, a smaller Q_2 (6 $\times$ 12 μm) is chosen. The PA is designed for a supply voltage of 4 V with base voltage of Q_2 biased at 2.7 V to ensure the dynamic voltage swing across each series HBT (Fig. 5) is lower than the BVCBO of 5.9 V [7]. The HBTs are laid out in a CBEBC (collector-base-emitter-base-collector) configuration for additional collector current handling reliability at the cost of increased device parasitics. Half harmonic traps are added at the base of each stage to eliminate the possibility of large signal spurious oscillation. The design steps of the stacked Class-E PA is shown in Fig. 7. The effect of C_{CB2} in reducing the collector efficiency due to ZVS violation is clear from steps 1 and 2.

Measured and simulated small-signal S-parameters are presented in Fig. 8 for $V_{Base-Lower}$ = 0.9 V, $V_{Base-Upper}$ = 2.7 V, and $V_{CC-Core}$ = 3.6 V. The large signal power measurements are conducted at $V_{CC-Core}$ = 4 V, $V_{Base-Lower}$ = 0.75 V, and $V_{Base-Upper}$ = 2.7 V. Fig. 9 shows the measured output power and power gain versus the input power at 41 GHz, while the corresponding drain efficiency and PAE versus the output power are plotted in Fig. 10. Fig. 11 shows the measured performance at peak PAE across 39 GHz to 47 GHz indicating a P_{-1dB} bandwidth of more than 5 GHz. The downward shift in the frequency of operation, from the designed 45 GHz to 41 GHz, may be due to inaccurate device interconnect modeling. The PA performance at peak PAE, measured

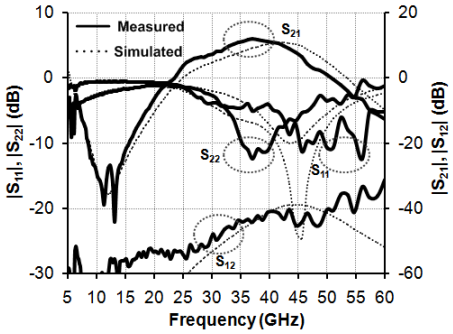

Fig. 8. Measured small-signal S-parameters.

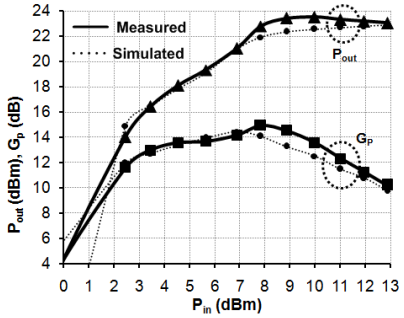

Fig. 9. Measured output power and power gain versus input power.

across 3 different chips to show consistency, is presented in Table 1.

V. Conclusion

A Q-band SiGe two-stage double stacked Class-E power amplifier with 23.4 dBm peak output power and 34.9% peak PAE based on a parasitic aware mm-wave stacked Class-E power amplifier design methodology is presented. This work compares favourably with previously reported silicon mm-wave PAs (Fig. 12) validating the merit of the design approach.

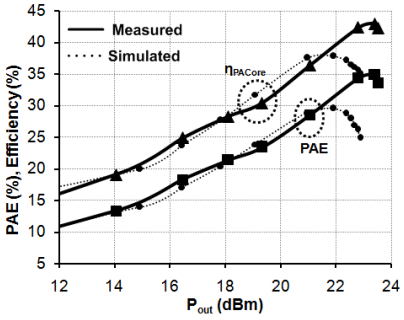

Fig. 10. Measured efficiency and PAE versus output power.

TABLE I
Measured Performance Summary

Performance Metric	Chip 1	Chip 2	Chip 3
Frequency (GHz)	41	41	41
BW_{-1dB} (GHz)	5	4	-
Supply Voltage (V)	4	4	4
$P_{out\ at\ Peak\ PAE}$ (dBm)	23.4	23	23.6
$G_{P\ at\ Peak\ PAE}$ (dB)	14.5	13.3	12.5
PAE_{peak} (%)	34.9	31.4	31

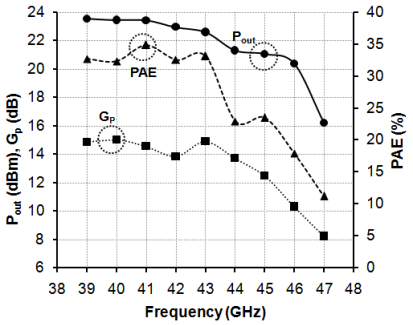

Fig. 11. Measured performance across the Q-band.

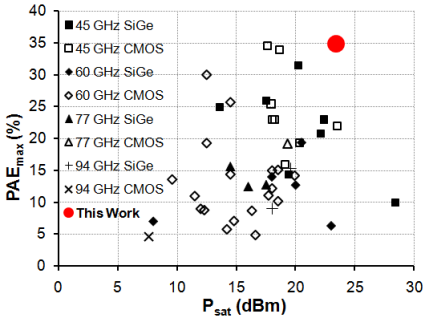

Fig. 12. PAE versus output power at peak PAE of published mm-wave silicon power amplifiers.

Acknowledgment

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