A 10-b, 300-MS/s Power DAC with 6-V_{pp} Differential Swing

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***Abstract* — A 10-bit digital-to-analog converter (DAC) is presented that delivers 6-V_{pp} into a 100-Ω differential load. The circuit is implemented in 45-nm CMOS SOI, which provides benefits for using a FET-stack current buffer. The measured DNL is better than 0.44 LSB. The DAC consumes 476 mW and achieves a peak SFDR of 54.4 dB and a minimum IM3 of -55.6 dBc. This DAC demonstrates the largest output swing and highest power efficiency for a high-resolution (>8b), high-speed (>100MS/s) DAC.**

***Index Terms* — digital-to-analog converter, DAC, current-steering.**

I. Introduction

Reconfigurable RF front-ends are increasingly pushing the digital-to-analog converter (DAC) towards the antenna. However, RF standards place high dynamic range and linearity specifications on transmitter circuitry on top of peak power requirements. Migrating towards fineline CMOS typically improves the bandwidth and resolution of the DAC at the cost of low breakdown voltage on the transistors.

Here, we use a 45-nm CMOS SOI process to realize a 10-bit power DAC with a 6-V_{pp} differential output swing. Prior work has proposed 12-b DACs with 2.5-V_{pp} swing [1]. Implementations in fineline CMOS introduce two sources of linearity degradation. First, we propose a novel local feedback circuit for each DAC current cell to increase the low output resistance of the fineline FETs. Additionally, a wideband current buffer based on a stacked-FET amplifier is placed between the current cells and a 100 Ω differential load to allow for high output voltage swing. Prior work has shown that stacked-FET amplifiers support high power for RF applications [2] but this technique has not been demonstrated for high-resolution DAC applications.

Section II outlines features of the proposed power DAC circuitry related to the 45-nm SOI process. Section III presents the chip architecture. Measurements of the power DAC are demonstrated in section IV. Finally, section V presents the conclusion.

II. Design Considerations

Device issues that impact differential nonlinearity (DNL), integral nonlinearity (INL), spurious-free dynamic range (SFDR), and third-order intermodulation (IM3) are discussed here.

A. Unit Current Cell with Local Negative Feedback

High current swing is required to drive a large voltage swing into a 100-Ω differential load. In this 10-bit DAC, the least significant bit (LSB) current is 60 μA. This large LSB current demands using FET geometry with large width in the unit current cell. While increasing the transistor width reduces the DNL and INL errors due to mismatch [3], it also lowers output resistance of the current cell, which results in higher distortion.

Fig. 1 (left) shows the simplified structure of a current steering DAC. Here, the switches are ideal and current cells are modeled with an ideal current source I_u in parallel with Z_u, which is the output impedance of the unit current cell. Depending on the state of the switch, Z_u is connected to either O_1 or O_2. As a result, the total effective load impedance is signal-dependent, which leads to distortion [1], [4]. The third-order harmonic distortion caused by current cells with finite output impedance is

$$HD3 = \left[\frac{M}{4}.\frac{R_{L,d}}{|Z_u|}\right]^2 \quad (1)$$

where M is the total number of current cells and $R_{L,d}=2R_L$ is the differential load resistance [4]. Increased output resistance improves the linearity and has been proposed by using devices with large lengths or by transistor cascodes [1], [3], [5], [6].

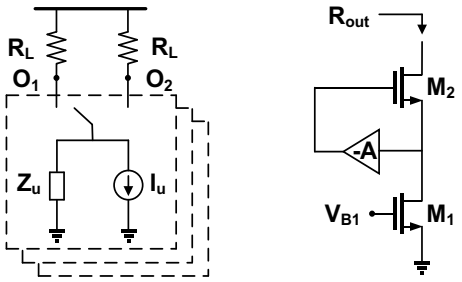

Fig. 1. Simplified structure of a current-steering DAC (left), unit current cell with local negative feedback (right).

The current cell proposed here uses both of these techniques. However, due to the large current cells, a

regulated cascode is proposed here to further increase the output impedance in each current cell. Fig. 1 (right) shows the proposed unit current cell. The output resistance of current source is

$$R_{out} \cong g_{m2}(1+A)r_{o1}r_{o2} \quad (2)$$

where r_{o1} and r_{o2} are the output resistance of M_1 and M_2 respectively. The output resistance of the unit current cell is $1+A$ times higher than a conventional cascode current source. Simulation indicates that the low-frequency output resistance is greater than 120 MΩ, however, the bandwidth of the negative feedback loop limits the bandwidth over which the distortion remains low.

B. High Voltage Swing Output Buffer

A stacked-FET current buffer is introduced between the DAC current sources and the output load to overcome the low breakdown voltage of the transistors. Fig. 2 shows the stacked-FET buffer. In a cascode configuration, the gate of the cascode transistor is a small-signal ground. In the stacked-FET buffer, the gates are connected to capacitors C_1, C_2, C_3, which form capacitive voltage dividers with the gate-source capacitance of the transistors M_1, M_2 and M_3, respectively [2]. This arrangement generates in-phase voltage swing at the gate and drain of each device. Therefore, drain-gate, drain-source and gate-source voltage swings of individual transistors remain less than the device breakdown voltage while the swing at the drain of M3 is large.

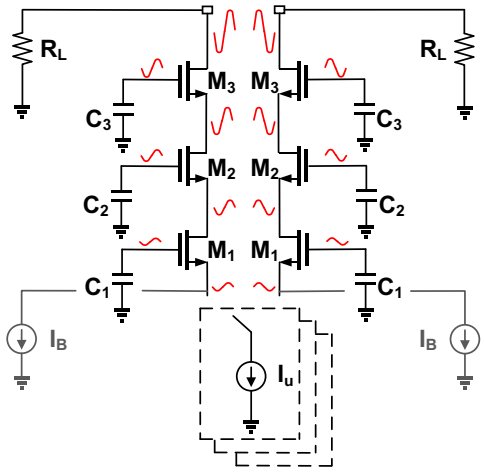

Fig. 2. Stacked-FET output buffer is placed on top of the current sources and switches. Current bleeders are connected to the bottom of the stacked-FET buffer.

In this work, we seek to understand the linearity constraints of the stacked-FET buffer. Increasing the number of transistors in the stack allows higher voltage swing but inevitably reduces linearity of the current. Fig. 3 shows the simulated spectrum of the differential 3-stack buffer driven by an ideal current source. At full swing, HD3 is 68.6 dBc. However, the current sources in the DAC are not ideal and have limited output impedance. Therefore, the input impedance of the stacked-FET buffer relative to the output impedance of the current sources should be negligible.

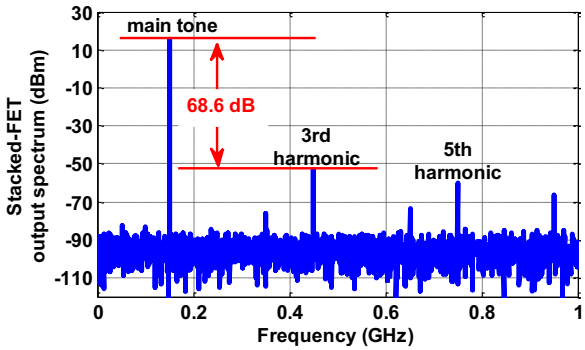

Fig. 3. Simulated output spectrum of the differential stacked-FET buffer at 150 MHz.

C. Current Bleeder

The impedance seen looking into the stacked-FET current buffer becomes dependent on the bias current through the stack. Therefore, the impedance looking into M_1 (α $1/g_m$) and the gate-source capacitance of the stacked FETs are signal dependent, which results in nonlinearity. To reduce the signal-dependent input impedance in the stacked-FET, two current bleeders (I_B) shown in Fig. 2 are connected to the bottom of the stacked-FET to ensure that there is d.c. current through both branches of the differential stack and avoid a drastic increase in the $1/g_m$ of the stack-FET buffer and keep the parasitic capacitance of the transistors constant [1].

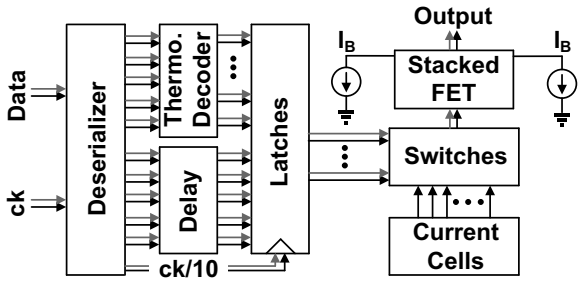

Fig. 4. The 10-bit DAC architecture.

III. DAC Architecture

Fig. 4 shows the 10-b power DAC architecture. The data input is demuxed into a 10-b word and the input

clock is divided by a factor of 10. The DAC is segmented into 5 unary MSBs and 5 binary LSBs. The thermometer decoder converts the 5 MSBs into a 31-bit thermometer decoded output. A delay block in the LSB path adjusts the latency between the binary and thermometer codes.

To avoid voltage glitches in the current sources during signal transitions [1], the crossing point of the switch drive voltage should be high to ensure that the switches connected to each current source are not simultaneously off. In the latches, the intrinsic delay between nMOS and pMOS transistors is used to lower the crossing point and an inverter shifts the crossing point voltage to higher voltages [7].

IV. Measurement Results

Fig. 5 shows the chip microphotograph. The DAC is implemented in 45-nm CMOS SOI and the area is 2.25 mm^2. The stacked-FET amplifier requires a 4-V supply and consumes 84 mA for a power consumption of 336 mW. The negative feedback in the current cells consumes 102 mW, and the deserializer and digital circuitry consumes 38 mW. Therefore, the total power consumption is 476 mW. Fig. 6 shows the measured INL and DNL of the DAC. The maximum measured INL and DNL is 0.6 LSB and 0.44 LSB, respectively. The LSB output voltage is 6 mV.

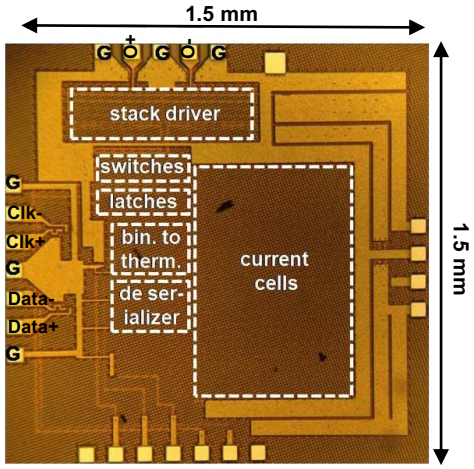

Fig. 5. Chip photograph.

Fig. 7 demonstrates the differential peak-to-peak output full swing at 150 kHz. As shown the DAC is capable of a 6.3-Vpp swing. Fig. 8 shows the output power of the DAC from DC to the Nyquist frequency. The 3-dB output power bandwidth is more than 100 MHz. In the dynamic measurements, the load is 100-Ω differential and the data and clock are provided with Agilent 81134A. The maximum speed of this pulse pattern generator is 3 GHz, so the maximum available clock speed is 300 MHz.

Fig. 9 demonstrates the SFDR and IM3 of the DAC. The SFDR is measured with one tone test at full swing and the IM3 is measured with two-tones at 6 dB back off (the envelope of the sum of the two tones has full swing). Both SFDR and IM3 have been measured from DC to Nyquist and they vary from 54.4 dB to 44.2 dB and -55.6 dBc to -47.9 dBc, respectively.

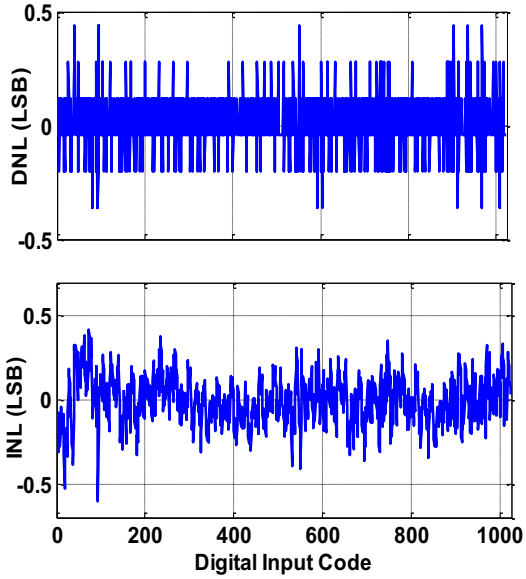

Fig. 6. Measured INL and DNL.

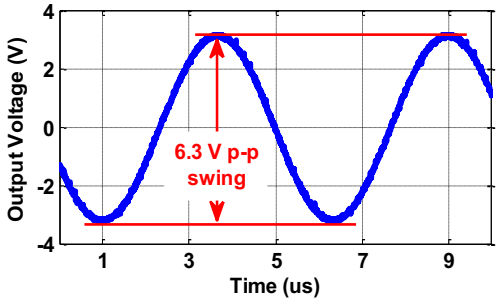

Fig. 7. 6.3 Vpp differential measured output swing at 150 kHz input frequency.

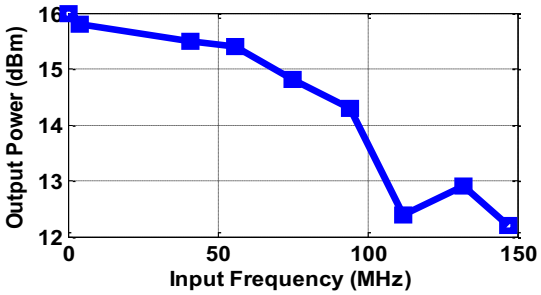

Fig. 8. Measured output power over 100 Ω differential load, DC to Nyquist, with 300 MS/s sampling rate.

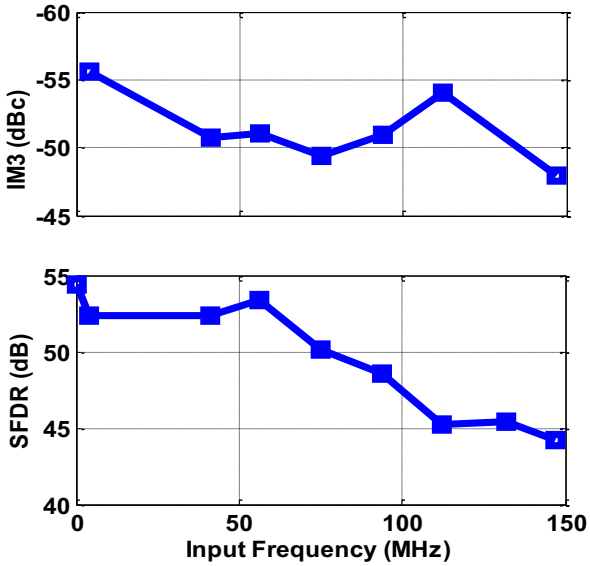

Fig. 9. Measured SFDR and IM3, DC to Nyquist. SFDR is measured with one tone at full swing and IM3 is measured with two tones, each at -6 dB back off.

To bias the circuit, a transformer can be used at the output, which avoids the voltage drop on load [1]. When comparing power dissipation, the available RF power should be considered [1]. The normalized power efficiency (NPE) of a DAC is defined as

$$NPE = \frac{P_{\text{peak,RF}}}{0.25 P_{\text{supply}}} \quad (3)$$

where the $P_{\text{peak,RF}}$ is the maximum available power for the load and P_{supply} is the total consumed power [1]. Table I compares this DAC with recently published current steering DACs. As Table I shows, this work demonstrates the highest power efficiency and largest swing for a high-resolution DAC.

V. Conclusion

A 10-bit, 300-MS/s power DAC is demonstrated in 45-nm CMOS SOI that provides a 6-Vpp differential output swing into a 100-Ω differential load. The linearity of a stacked-FET output buffer is discussed and demonstrated to provide sufficient linearity for 10-b operation. Additionally, the local negative feedback is used to increase the output resistance of the DAC current cells.

Acknowledgment

This work was supported through a subcontract from Rockwell Collins under the DARPA Microscale Power Conversion Program (FA8650-11-C-7184). We appreciate access to IBM12SOI through TAPO. Additionally, the authors thank the members of the High-speed Integrated Circuits Group at UCSD.

TABLE I

Comparison With Published Data

Ref.	Res. [bits]	Tech [nm]	F_{clk} [GHz]	Swing [V_{ppd}]	Power [mW]	NPE [%]
This work	10	45	0.3	6	476	76
[1]	12	65	2.9	2.5	188	66
[3]	10	350	0.5	2	125	44
[4]	12	90	1.25	0.8	128	10
[6]	6	130	3	0.4	29	11

References

[1] W.-H. Tseng, F. M. L. van der Goes, J. R. Westra, J. Mulder, Y. Lin, E. Arslan, E. Ayranci, X. Liu, and K. Bult, "A 12 bit 2.9 GS/s DAC With IM3 < -60 dBc Beyond 1 GHz in 65 nm CMOS," *IEEE J. Solid-State Circuit*, vol. 44, no. 12, pp. 3285-3293, Dec. 2009.

[2] S. Pornpromlikit, J. Jeong, C. D. Presti, A. Scuderi, and P. M. Asbeck, "A Watt-Level Stacked-FET Linear Power Amplifier in Silicon-on-Insulator CMOS," *IEEE Trans. Microwave Theory & Tech.*, vol. 58, no. 1, pp. 57-64, Jan. 2010.

[3] C.-H. Lin and K. Bult, "A 10-bit 500-MSample/s CMOS DAC in 0.6 mm^2," *IEEE J. Solid-State Circuit*, vol. 30, no. 12, pp. 1948-1958, Dec. 1998.

[4] C.-H. Lin, C.-W. Fan, and J.-T. Wu, "A 12-Bit 1.25-GS/s DAC in 90 nm CMOS With > 70 dB SFDR up to 500 MHz," *IEEE J. Solid-State Circuit*, vol. 46, no. 12, pp. 2845-2855, Dec. 2011.

[5] A. Van den Bosch, M. A. F. Borremans, M. S. J. Steyaert, and W. Sansen, "A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter," *IEEE J. Solid-State Circuit*, vol. 36, no. 3, pp. 315-323, March 2001.

[6] X. Wu, P. Palmers, and M. S. J. Steyaert, "A 130 nm CMOS 6-bit Full Nyquist 3 GS/s DAC," *IEEE J. Solid-State Circuit*, vol. 43, no. 11, pp. 2396-2402, November 2008.

[7] J. Bastos, A. M. Marques, M. S. J. Steyaert, and Willy Sansen, "A 12-Bit Intrinsic Accuracy High-Speed CMOS DAC," *IEEE J. Solid-State Circuit*, vol. 33, no. 12, pp. 1959-1969, Dec. 1998.