Simultaneous Linearity and Efficiency Enhancement of a Digitally-Assisted GaN Power Amplifier for 64-QAM

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***Abstract* — The first dynamic 4-bit, digitally-assisted GaN high power amplifier (DAPA) system transmitting 7.68-Msymbol/s with 64-QAM modulation is presented. An FPGA is programmed to generate the pulse-shaped 64-QAM signal, perform envelope estimation, and time-align the RF and digital control signals arriving at the DAPA. A high-speed, level-shifting circuit converts the FPGA's low-voltage differential signaling (LVDS) DAPA control signals into single-ended logic levels required for the depletion-mode GaN HEMT DAPA auxiliary cells. Measured results show 9.6% DC power savings, 23% improved PAE, and 23% higher output power at 4% EVM_{RMS} compared to the static PA configuration.**

***Index Terms* — Digital control, gallium nitride, linearization techniques, peak-to-average power ratio, power amplifiers, quadrature amplitude modulation.**

I. Introduction

Bandwidth efficient modulation schemes, including quadrature amplitude modulation (QAM) and orthogonal frequency division multiplexing (OFDM), achieve higher data rates with limited spectrum but result in transmitted signals with high peak-to-average power ratios (PAPRs). An undesired result is that conventional power amplifiers (PAs) must lower efficiency to maintain linearity when transmitting these signals. Well-known architectures [1]-[3], including envelope tracking, *N*-way Doherty PAs, polar modulators, and digital predistortion (DPD), have been demonstrated to improve conventional analog PA efficiency while satisfying linearity requirements. A new mixed-signal technique introduced by the authors [4] describes a digitally-assisted power amplifier (DAPA) with dynamically-switched auxiliary (AUX) cells for simultaneous linearity and efficiency improvement.

The proposed approach departs from statically reconfigurable digital-controlled PAs that select gain states or power modes to accommodate different wireless systems. Dynamic digital assistance provides an additional advantage of tailoring PA characteristics on-the-fly, as signal envelopes of high-PAPR signals vary with time, to further improve efficiency by reducing excessive current consumption. This paper describes the design approach for a 4-bit DAPA based on a 0.2-µm, high-f_T, GaN HEMT process and the system architecture, including DSP and drive circuitry, used to verify the overall improvement from digital-assisted architectures, as shown in Fig. 1.

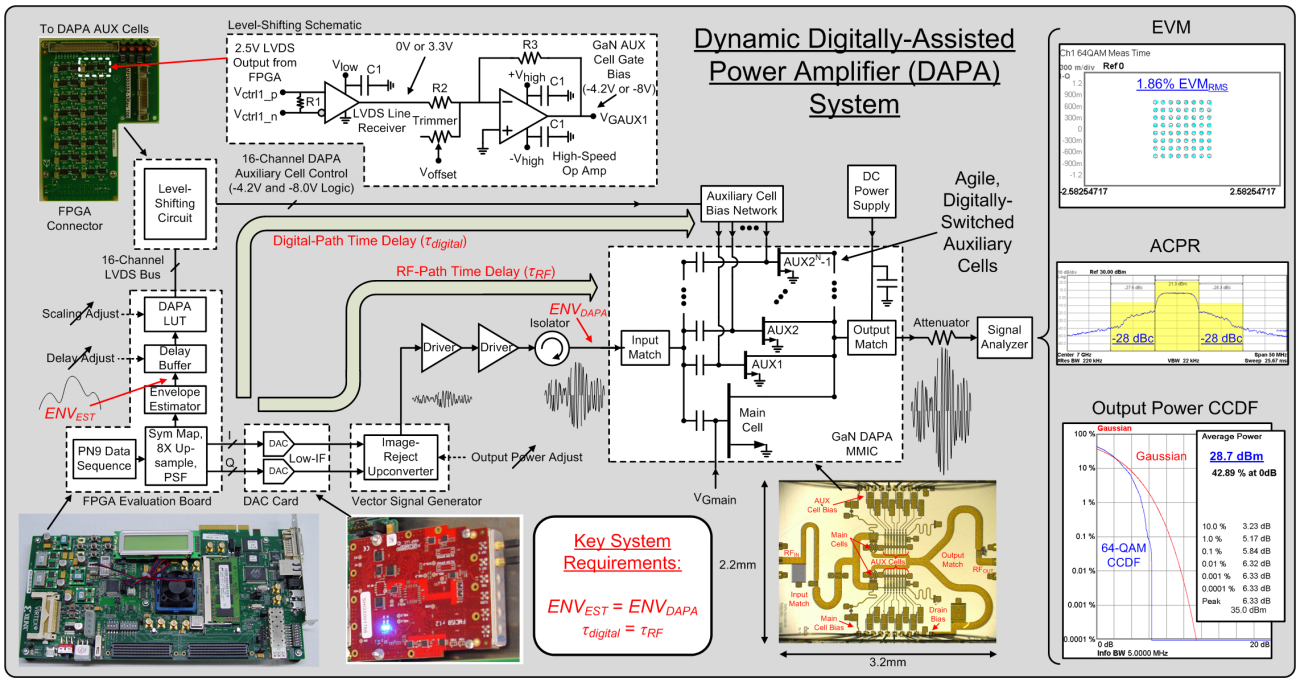


Fig. 1. Dynamic digitally-assisted power amplifier system diagram.

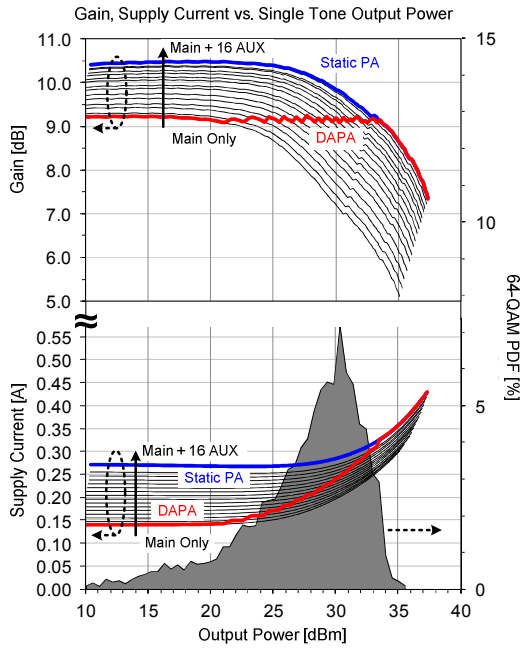


Fig. 2. Measured gain and supply current family of curves for each AUX state of the 4-bit GaN DAPA at 7GHz.

II. Theory of Operation

In the proposed *N*-bit DAPA (Fig. 1), a main transistor, with a constant gate bias, and 2^N - 1 AUX cells are arranged in parallel to form the DAPA core. Individual gate bias networks enable individual control of each AUX cell bias. Fixed RF matching networks and a shared drain bias complete the DAPA. Fig. 2 provides measured gain and DC supply current versus output power as each of the 16 AUX cells are enabled in the presented 4-bit GaN DAPA. These family of curves show incremental gain and supply current increases as AUX cells are enabled. To obtain a flat AM-AM response, the DAPA relies on the main cell at low output power and enables AUX cells as needed to compensate gain compression. AUX cells effectively increase linear output power, but operate nonlinearly compressed themselves. A locally nonlinear, globally linear DAPA-system response, plotted in red (Fig. 2), enables much more linear behavior versus output power than the static PA configuration with all AUX cells enabled, while still delivering the same saturated output power. While this approach sacrifices gain slightly (~1.3dB), examination of the DAPA DC supply current plot shows significant reduction at output power backoff which becomes extremely beneficial when considering the probability density function (PDF) of a 7-dB PAPR 64-QAM signal overlaid in Fig. 2. While a static PA sacrifices current at backoff to meet peak output power needs, dynamic AUX cell switching of the DAPA provides significant supply current reductions across the majority of the 64-QAM output power range.

During dynamic operation, the time-varying envelope of the RF input signal is analyzed by a control circuit which outputs the appropriate AUX cell state to 1) linearize – by compensating for gain compression with additional AUX cell gain and 2) improve efficiency – by disabling AUX cells to reduce average current consumption. Therefore, binning operation by the DAPA AUX cell control circuit relies on accurate envelope information of the DAPA input signal. With this digitally-assisted approach AUX cells are always in either one of two possible logic states, enabled (ON) or disabled (OFF). While there is some quantization error in the DAPA's digital approach, sufficient AUX cell resolution enables the DAPA to avoid bias nonlinearities of envelope-tracking and band-limiting load modulation of Doherty PAs.

III. System Components

Referring to Fig. 1, the main elements of the dynamic DAPA system include the FPGA and DAC, level-shifting circuit, and DAPA. The following subsections provide details on each component's design and implementation.

A. FPGA and DAC

While dynamic operation could be achieved with an envelope detector, lookup table (LUT), and control circuit, an FPGA approach was chosen for its ease of use and overall flexibility. The FPGA creates the digital IQ signals, calculates the envelope amplitude, determines AUX cell states at each sample, and aligns digital and RF signals at the DAPA. A Xilinx ML605 evaluation board was chosen as the development platform for its high speed, numerous inputs/outputs (IOs), wide programming base, and strong hardware support. VHDL code was written for Gray-coded reconfigurable symbol mapping, and square-root raised cosine (SRRC) pulse-shape filtering (=0.3) for 64-QAM generation. The FPGA performs 8X up-sampling on the 7.68 Msymbol/s signal to push out sampled images for improved out-of-band rejection. A pseudorandom noise (PN9) sequence data pattern is used to ensure accurate demodulation by the test equipment. Digital IQ data streams feed into a 4DSP FMC150 dual-channel DAC card where they are modulated into quadrature 61.44-MHz, low-IF signals using the TI DAC3283's built-in complex mixing function. The quadrature low-IF signals from the DAC feed the external baseband IQ inputs of an Agilent E8267C signal generator for up-conversion on the baseband IQ modulation path, resulting in a 7-GHz,

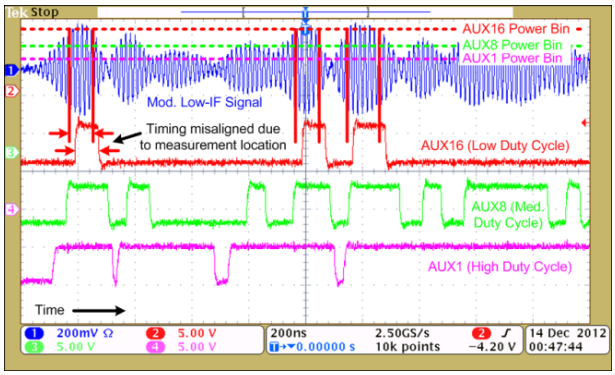


Fig. 3. Oscilloscope screenshot showing digital nature AUX cell control signals and time alignment with low-IF envelope.

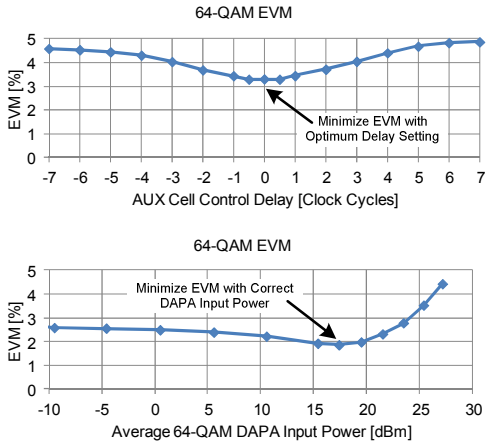


Fig. 4. Measured EVM vs. AUX cell control delay and average 64-QAM input power.

image-rejected RF signal. Agilent 83020A and GaN driver amplifiers provide linear amplification of the 7-GHz modulated signal to sufficient power levels for DAPA gain compression.

B. Level-Shifting Circuit

The level-shifting circuit converts between the FPGA's 2.5V LVDS AUX cell control signals and the large negative voltage required for the depletion-mode GaN HEMT gate bias. With the FPGA's 8X up-sampling ratio, the level-shifting circuit operates at 61.44MHz. A schematic for one channel of the 16-channel high-speed, level-shifting circuit is inset in Fig. 1. Analog Devices ADN4662 LVDS receivers convert the FPGA's differential control outputs to single-ended 0-3.3V logic. Texas Instruments THS3001 high-speed operational amplifiers, configured as inverting summers, complete level shifts by DC offset and scaling of the 0-3.3V logic to obtain -4.2V (ON) or -8V (OFF) logic levels for AUX cells. Trimmer potentiometers provide scaling adjust to handle process variations of the GaN HEMT gate voltage.

C. GaN DAPA

The GaN DAPA is an improved, 4-bit, higher power version of the 3-bit DAPA presented in [4]. Two, 8-finger, 500-µm GaN HEMTs serve as the static main cell and 2-finger, 60-µm GaN HEMTs are used for the 16 AUX cells. Fixed matching networks were designed at 7GHz and all cells share a single 28V drain bias. The MMIC was fabricated in Northrop Grumman Aerospace Systems' standard 0.2-µm AlGaN/GaN HEMT process on a 3-in SiC wafer, with V_{br} = 80V and f_T = 70GHz. A photo of the fabricated DAPA is shown in Fig. 1. Saturated output power with all AUX cells enabled exceeds 5W at 7GHz.

D. Configuration and Alignment

The dynamic DAPA concept specifically requires the FPGA to implement cubic-Farrow time interpolation, equiripple-error magnitude estimation (EEME) envelope estimation, integer/fractional clock delay, and a programmable AUX cell LUT. Time interpolation and clock delay enable precise alignment of RF and digital signals arriving at the DAPA ($\tau_{RF} = \tau_{digital}$), while envelope estimation and the LUT ensure the FPGA determines the correct AUX cell state ($ENV_{DAPA} = ENV_{EST}$).

The AUX cell state input power bins in the DAPA LUT were determined from the static gain measurements in Fig. 2. Accurate envelope estimation and time alignment are critical to DAPA operation with any amplitude or time errors resulting in unintended AM-AM. With the system assembled, an RF power calibration provided the exact DAPA input power values and test-set EVM contribution for each signal generator power setting. The input power information was passed to the FPGA's LUT scaling adjust. Time alignment between the RF and digital control signals was accomplished using the FPGA to adjust integer clock-cycle delay of the AUX cell signals and time interpolate for fractional clock-cycle envelope estimation.

A four-channel oscilloscope was used to capture time domain plots of the modulated low-IF signal and level-shifting channels for AUX1, AUX8, and AUX16 (Fig. 3). The duty cycle and relative timing of AUX cell control signals correlate very well with the envelope amplitude of the low-IF signal. Because the AUX cell control signals were measured at the DAPA and the low-IF signal is captured before the up-converter there appears to be a slight timing advance of the low-IF signal. The signals align at the DAPA when the additional delay of the up-converter and driver amplifiers is added to the RF path.

Fig. 4 shows a plot of 64-QAM error vector magnitude (EVM) versus AUX cell control signal delay and average 64-QAM DAPA input power. As predicted, the optimum delay setting and correct input power information result in

minimized EVM due to proper time/amplitude alignment of the RF and digital signals at the DAPA.

IV. Measured Results

The EVM, supply current, and power-added efficiency (PAE) of the dynamic DAPA system were measured as average 64-QAM input power was swept and the FPGA's LUT scaling factor updated to reflect the actual DAPA input power. EVM and average signal power were measured using an Agilent N9030A PXA signal analyzer. Root sum of squares (RSS) error estimation was used to remove test-set EVM contribution as input power was varied. Average supply current during dynamic operation was recorded from the DC power supply. PAE was calculated for the DAPA and does not include FPGA or level-shifting circuit power draw. Power consumption of the proof-of-concept, level-shifting circuit is 4W due to resistive dissipation in the op-amp design and could be reduced using custom high-voltage CMOS/SiGe circuitry and/or enhancement-mode GaN. ASIC/FPGA overhead to implement the DAPA-specific DSP (time interpolation, envelope estimation, etc.) is estimated to be less than 100mW and smaller than 10% of total power consumption depending on data rate.

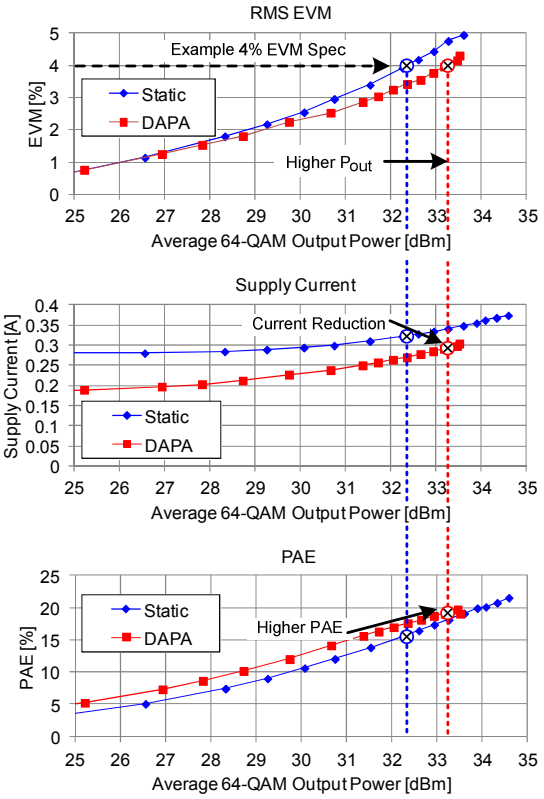
At high output power the dynamic DAPA provides EVM, supply current, and PAE advantages over the static PA without the use of DPD (Fig. 5). For an example 4% EVM spec, the dynamic DAPA has average 64-QAM output power of 33.2dBm, draws 291mA at 28V, and average PAE of 19.1%. Compared to the static PA configuration, an additional 0.9dB more output power, 9.6% decrease in supply current (0.87W power reduction), and 23% improvement in PAE is obtained. Additionally, at output power levels below 30dBm the DAPA provides >2W DC power savings with minimal linearity impact.

V. Conclusion

Dynamic operation of a DAPA system for simultaneous linearity and efficiency enhancement has been presented. Measured results reinforce the benefits of the dynamic DAPA concept by providing 9.6% DC power savings, 23% improved PAE, and 23% higher output power at 4% EVM_{RMS} with a 7.68 Msymbol/s, 64-QAM signal.

Acknowledgement

The authors would like to thank the Office of Naval Research for funding this research under contract N00014-10-C-0166 monitored by Dr. Paul Maki.



4% EVM Spec	Output Power	Supply Current	PAE
Static PA	32.3dBm	322mA	15.5%
Dynamic DAPA	**33.2dBm**	**291mA**	**19.1%**

Fig. 5. Measured EVM, supply current, and PAE vs. average 64-QAM output power for dynamic DAPA and static PA.

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