A Current-Reuse Class-C LC-VCO with an Adaptive Bias Scheme

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***Abstract* — This paper proposes a low-power current-reuse complementary differential LC-VCO which is composed of a pair of NMOS and PMOS transistors with an adaptive bias scheme for both transistors to ensure its robust startup and achieve maximum swing in Class-C operation. The proposed VCO has been implemented in a standard 0.18µm CMOS technology, which oscillates at the carrier frequency of 4.6 GHz. The measured phase noise is -139.5dBc/Hz at 10 MHz offset while drawing a current consumption of 1.6 mA from 1.5 V supply. The Figure of Merit is -189.1 dBc/Hz. To the author's best knowledge, this is the first class-C current-reuse VCO with an adaptive bias scheme.**

***Index Terms* — Current-Reuse, LC-VCO, feedback Class-C, Phase noise, Start-up, CMOS.**

I. Introduction

Recently, the rapid growth of wireless consumer applications in an ISM band, *e.g.*, Wireless Sensor Network (WSN), has driven a demand for low-power and high integration of RF wireless transceivers using CMOS technology [1]. To ensure a reliable communication of low-power System on Chip (SoC), a design of low-power and low-phase-noise voltage-control-oscillators (VCOs) becomes increasingly important.

Classical differential LC-tank oscillators, *i.e.,* NMOS and CMOS topologies, have been standard choices for RF circuit design. As shown in Fig.1, CMOS VCO shares the same maximum theoretical phase noise figure-of-merit as NMOS VCO. However, a CMOS VCO has a 6 dB better performance with the same power budget and resonator when operating in current-limited region. Additionally, the swing is within a supply rail which has less concern for reliability issues.

After Andreani *et al.* introduced the Class-C oscillator [2], which can preserve high DC-to-RF current conversion efficiency, a number of developments in Class-C NMOS VCOs have been proposed [3]-[5]. Similar to conventional class of VCOs, class-C CMOS VCO has a theoretically 6dB better phase noise performance compared to class-C NMOS VCO when operating in current-limited region.

In this paper, a Current-reuse Class-C VCO is proposed, which is composed of a current-reuse CMOS VCO operating in class-C using an adaptive bias scheme shown in Fig.2 to guarantee a robust oscillation start-up and maximize its oscillation swing. The current-reuse topology consumes half the current of the traditional CMOS. Thus, from theoretical limit, class-C current reuse CMOS topology is capable of maintaining the same phase noise figure of merit at half the power of class-C CMOS topology. However, due to its sensitivity to peak dynamic current, current-reuse CMOS topology suffers from amplitude mismatch [6] in voltage-limited regime. In earlier publications, additional circuit components are required, *e.g.,* source resistance [6], cascoded PMOS and NMOS [10]-[11] to operate VCO in the current-limited regime. In this work, the proposed topology inherently achieves symmetric amplitude through undistorted dynamic current in class-C operation. As a result, the

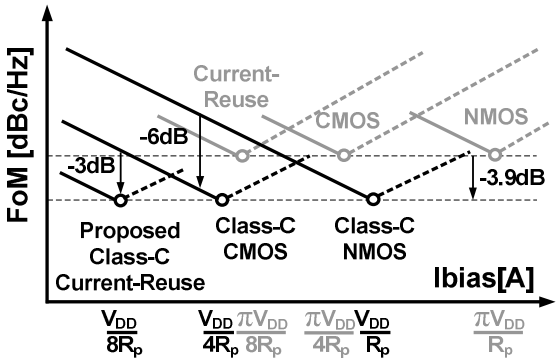


Fig.1. Theoretical FoM limit of a conventional class of VCOs and its corresponding Class-C VCOs.

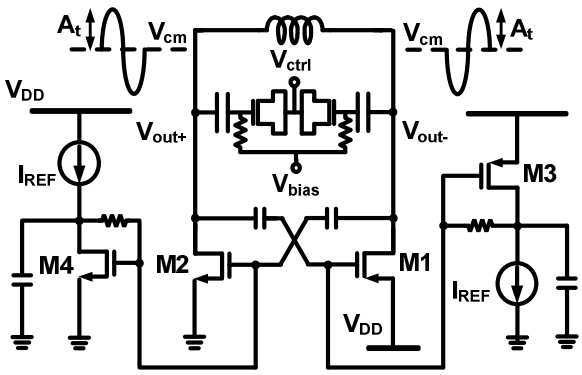


Fig.2. Proposed Current-reuse Class-C VCO with an adaptive bias scheme

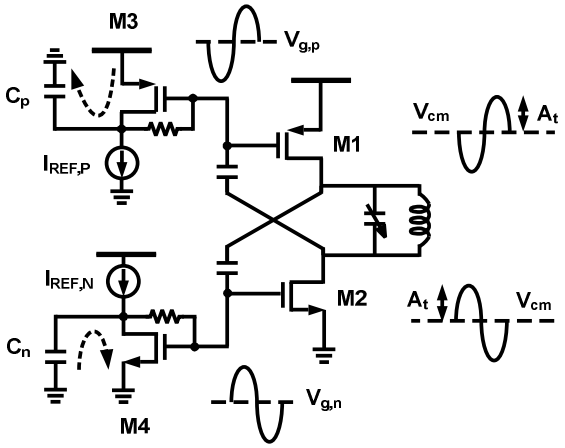


Fig.3. Simplified diagram of the proposed class-c current reuse VCO to describe its operation.

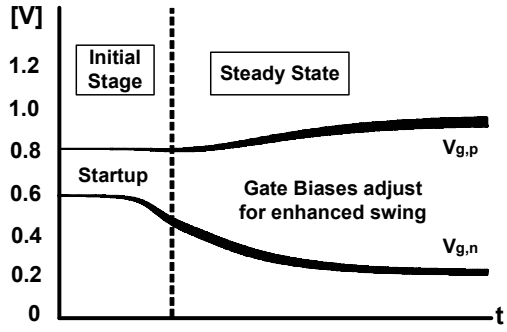


Fig.4. Simulated transient waveforms of adaptive gate bias of PMOS, NMOS.

proposed VCO achieves a good phase noise performance while maintaining its low power consumption.

This paper is organized as follows. Section II presents the analysis and design of proposed VCO which discusses conventional Class-C NMOS VCO and the proposed Current-Reuse Class-C VCO. The following section describes the measurement results. Finally, the conclusion is summarized in Section IV.

II. Analysis and Design of the Proposed VCO

A. Conventional Class-C VCO

To maintain the class-C operation in a conventional Class-C VCO, the NMOS cross-coupled pair must not enter the deep triode region [2]. The maximum oscillation swing is, therefore, limited by $(V_{\mathrm{DD}} - V_{\mathrm{g,n}} - V_{\mathrm{th,n}})/2$ where V_{DD} is the supply voltage, A_{t} is the oscillation amplitude, $\mathrm{V_{g,n}}$ is the gate bias voltage of NMOS transistor, and $\mathrm{V_{th,n}}$ is the threshold voltage of NMOS transistor. To achieve higher maximum oscillation swing, $\mathrm{V_{gbias}}$ has to be reduced. However, this causes an issue for its robust operation since it may not meet startup condition. Some techniques to overcome this have been proposed [3]-[5].

In order to further improve power efficiency, a lower-power class-C current-reuse VCO is proposed with an adaptive bias scheme for both NMOS and PMOS transistors.

B. Proposed Class-C Current-Reuse VCO with Adaptive Bias Scheme

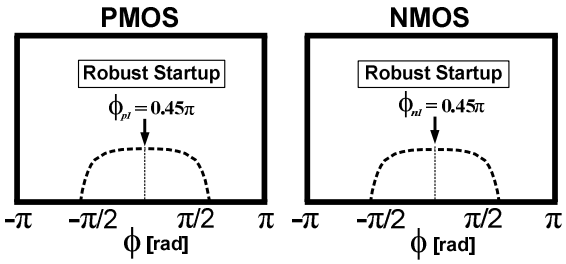
The detailed schematic of the proposed Class-C current-reuse VCO with an adaptive bias scheme is depicted in Fig.3. It is composed of three main parts, *i.e.,* a core VCO and separate adaptive bias circuits for NMOS and PMOS transistors. The core VCO is composed of one pair of cross-coupled PMOS and NMOS transistors. The adaptive bias scheme is composed of two modified current mirrors as shown in Fig.2. The bias circuits do not only provide an adaptive gate bias for robust start-up and enhance oscillation swing, but also add an ability to control current in the main oscillator which is unable in its original design in [6]. Additionally, the bias circuits do not directly load the LC-tank [3]-[5] and does not impose high power headroom.

For a better understanding of the theoretical limit of oscillation swing is explained as follows. If the operation of current-reuse VCO enters voltage-limited region, the output will have asymmetric waveform. Moreover, the conduction angle of devices increases and the drain current shapes are widened which loses its high DC-to-RF current conversion efficiency [2]. This can lead to degradation of phase noise performance. To avoid such issue, both NMOS and PMOS transistors should remain in active region. By assuming the same common voltage, the maximum oscillation amplitude is limited by:

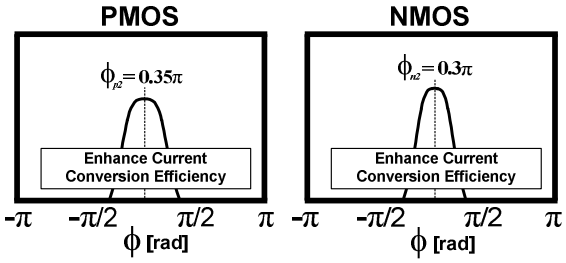
$$A_{\mathrm{t}} < (V_{\mathrm{g,p}} - V_{\mathrm{g,n}} + |V_{\mathrm{th,p}}| + V_{\mathrm{th,n}})/4 \qquad (1)$$

where V_{CM} is the common mode voltage, $\mathrm{V_{g,p}}$ is the gate bias voltage of PMOS transistor, and $\mathrm{V_{th,p}}$ is the threshold voltage of PMOS transistor. According to (1), the maximum oscillation swing can be enhanced by larger difference between gate bias of PMOS and NMOS. However, an increase in $V_{\mathrm{g,p}}$ and a decrease in $V_{\mathrm{g,n}}$ lead to maximum oscillation amplitude, their transconductance drops. To ensure its oscillation start-up, relatively higher and lower gate bias for NMOS and PMOS, respectively, are necessary at the initial state. Once the steady oscillation has been built, $V_{\mathrm{g,p}}$ and $V_{\mathrm{g,n}}$ can adaptively change its value to become higher and lower, respectively, which in turns, maximizing oscillation swing with better phase noise performance at the steady state.

The circuit operation can be described as follows. Before VCO starts to oscillate, the initial gate biases of NMOS and PMOS transistors are determined by $\mathrm{I_{REF,N}}$



(a) Initial state

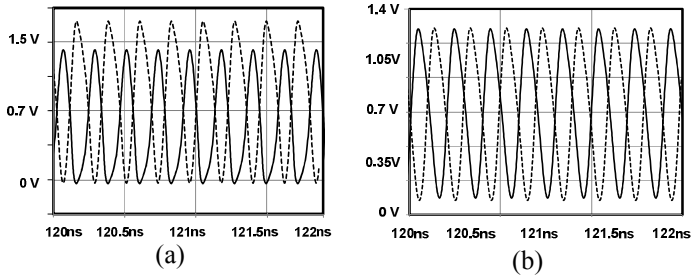


(b) Steady state

Fig.5. Current waveform of the proposed VCO at initial and steady state for NMOS and PMOS

and $I_{REF,P}$. Once the current in the core oscillator provides enough transconductance to meet the oscillation condition, output voltage starts to swing across V_{CM}. Then, the adaptive bias scheme acts like a negative feedback which senses an oscillation swing and adaptively changes gate biases of both transistors to enhance its maximum swing for a current-limited regime at steady state. This is because, once the amplitude of oscillation at the gate of M2 swings high enough to turn transistor M4 on, the capacitor C_n starts to discharges to ground in the first cycle. Consequently, the gate bias of NMOS decreases. At the same time, transistor M3 also turns on when the swing is large enough. This charges voltage to capacitor C_p which in turns increases DC voltage level at the gate bias of PMOS transistor. According to (1), to maximize oscillation swing, the difference between gate bias of NMOS and PMOS at steady state should also be maximized, which can be achieved by a proper size of M1, M2 and C_p, C_n.

From simulation based on 1.5 V supply, at the initial state, the gate bias of NMOS and PMOS are 0.6V and 0.8V, respectively, from 68uA of both $I_{REF,N}$ and $I_{REF,P}$. At steady state, the gate biases of NMOS and PMOS adaptive changes to 0.25V and 1.05V, respectively. Moreover, conduction angle $\left(2\phi_{n,p}\right)$ is defined as $\cos\left(\phi_{n,p}\right) = (-V_{gsn,p} + V_{thn,p})/A_t$. Fig.5 (a) shows the current waveform of the proposed class-C current-reuse VCO in the initial state with conduction angles of $2\phi_{p1}$ and $2\phi_{n1}$ and in the steady state with conduction angles of $2\phi_{p2}$ and $2\phi_{n2}$ for PMOS and NMOS transistors respectively. Initially, ϕ_{p1} and ϕ_{n1} are set at 0.45π and 0.45π for robust start-up condition. In the steady state, as shown in Fig.5 (b), ϕ_{p1} and ϕ_{n1} are 0.35π and 0.3π, respectively. This can increase the maximum oscillation swing. As a result, by comparing the proposed VCO with the current-reuse VCO without adaptive bias circuit scheme which has a conduction angle of 0.5π for both NMOS and PMOS, the proposed VCO can maintain more balanced waveform as shown in Fig.6. and achieve better phase noise performance.



(a) (b)

Fig.6. Output amplitude of current-reuse VCO (a) without and (b) with adaptive bias scheme.

III. Experimental Results

To validate the analysis and design in Section II, the VCO is implemented in a standard 180nm CMOS process. Fig.7. shows the microphotograph of the fabricated VCO. The core chip area is $0.18mm^2$. The measured tuning range is 4.5GHz to 4.6GHz. To compare the performance of the proposed VCO with other state-of-the-art VCOs, a figure of merit (FoM) is defined as follows:

$$\text{FoM} = \mathcal{L}(f_{\text{offset}}) - 20\log\left(\frac{f_0}{f_{\text{offset}}}\right) + 10\log\left(\frac{P_{\text{DC}}}{1\text{mW}}\right) \qquad (2).$$

where $\mathcal{L}(f_{\text{offset}})$ is phase noise, f_{offset} is offset frequency, $f_0$is oscillation frequency and P_{DC} is power consumption. For 1.5V supply, a phase noise of -139.5dBc/Hz @10MHz offset can be achieved while consuming 1.6mA which is approximately a figure of merit of -189 dBc/Hz.

Table I summarizes the comparison to other publications based on current-reuse topology. The reported performance of CMOS VCOs in [7]-[8] cannot achieve better FoM than -187 dBc/Hz due to inefficient

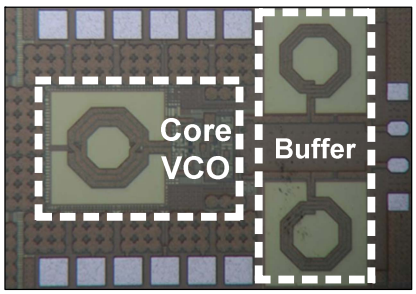


Fig.7. Chip Micrograph

TABLE I
COMPARISON WITH THE-STATE-OF-THE-ART VCOS IN A CURRENT-REUSE TOPOLOGY

Ref.	Tech.	VCO Topology	Frequency (GHz)	Phase Noise (dBc/Hz)	Power (mW)	FoM (dBc/Hz)	Additional components for Balanced Amplitude
[7]	65nm	CMOS	3	-114@1MHz offset	0.7	-187	-
[8]	55nm	CMOS	6.8	-123 @2MHz offset	9	-185	-
[9]	65nm	Current-Reuse	2.1	-126.1@3MHz offset	0.28	-190	-
[10]	180nm	Current-Reuse	16	-111@1MHz offset	8.1	-187	Required
[11]	180nm	Current-Reuse	2.9	-122@1MHz offset	1.7	-188	Required
[6]	180nm	Current-Reuse	2.0	-123@1MHz offset	1	-189	Required
This	180nm	**Class-C Current-Reuse**	4.6	-139.5 @10MHz offset	2.4	-189	**Not required**

DC-to-RF current conversion. The proposed VCO achieves lower power consumption and better phase noise performance since the proposed VCO avoids itself to operate in voltage-limited region. This work achieves a comparable FoM among the-state-of-the-art current-reuse VCOs [6],[9]-[11]. Moreover, the proposed class-C current-reuse VCO can compensate the unbalanced waveform without any additional components[6],[10]-[11].

IV. CONCLUSION

In this paper, a Class-C current-reuse VCO with an adaptive bias scheme is proposed. The proposed adaptive bias scheme can mirror core current, keep both transistors in a proper operation for high current efficiency, and achieve balanced tank waveforms. Moreover, it guarantees a robust oscillation start-up and allows the gate biases to change for higher maximum oscillation swing. As a result, it shows capability of achieving low phase noise with low power consumption. The proposed adaptive bias scheme can also be applied to a CMOS VCO for class-C operation.

ACKNOWLEDGEMENT

This work was partially supported by MIC, SCOPE, MEXT, STARC, Canon Foundation, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Tech. Japan, Ltd.

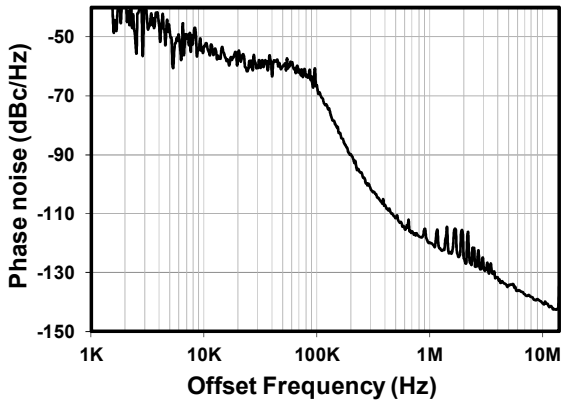


Fig.8. Measured phase noise plot at 4.63GHz

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