# CMOS RF Noise, Scaling, and Compact Modeling for RFIC Design

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***Abstract* — This work presents an analysis of high frequency noise and linearity performance of a 90 nm CMOS process. Measurements are performed for a wide range of nominal gate lengths and bias points at high frequency. Modeling is based on the EKV3 compact model in Spectre RF circuit simulator from Cadence. The model shows correct scalability for noise and linearity accounting for short channel effects (SCEs), such as velocity saturation (VS) and channel length modulation (CLM). Results are presented versus a common measure of channel inversion level, named inversion coefficient. Optimum performance is shown to gradually shift from higher to lower levels of moderate inversion, when scaling from 240 nm to 100 nm. The same trend is observed from investigating the transconductance frequency product (TFP) of a common-source (CS) LNA for technology nodes ranging from 180 nm to 22 nm.**

***Index Terms* — Compact model, distortion analysis, dynamic range, high frequency noise, metal oxide semiconductor field effect transistor (MOSFET), minimum noise figure ($NF_{min}$), moderate inversion.**

## I. Introduction

Scaling CMOS to the deca-nanometer regime, a tremendous improvement of RF performance has been reported in terms of conventional figures of merit (FoM), such as $f_T$ and $f_{max}$ [1]-[2]. However, a large amount of industrial IC design of RF front ends is still done using CMOS technology nodes such as 180 nm and 90 nm, due to their high RF-performance-to-cost ratio [3]. Therefore, accurate modeling of these CMOS processes remains of high interest. Previous published work has shown RF noise performance and harmonic distortion for specific bias points and limited frequency range [4]-[6]. In this paper, we expand the work of previous publications presenting a detailed investigation of RF noise and harmonic distortion expressed by $NF_{min}$ and 3rd-order intercept points ($P_{IP3}$ and $V_{IP3}$), respectively, based on measurements over a wide range of frequency, bias points and nominal gate lengths. These FoMs, which determine the dynamic range of a circuit, are shown with respect to nominal gate length and inversion level, experiencing a shift in their optimum performance to lower inversion level when scaling from 240 nm down to 100 nm. The EKV3 compact model efficiently describes this behavior.

## II. RF Noise

### A. Noise Measurements

Noise measurements have been performed using a system setup consisting of a vector network analyzer, tuners, filters and a spectrum analyzer with a noise figure measurement personality. MOS devices of channel width W=40x2 um and nominal gate length ranging from L=240 nm to L=100 nm have been measured up to 20 GHz. The drain-source voltage ($V_{DS}$) is kept constant at 1.2 V whereas the gate-source voltage ($V_{GS}$) is swept from 0 to 1 V. Noise parameters $NF_{min}$, $R_n$, and $\Gamma_{opt}$ are expressed in terms of two-port network theory as:

$$NF = NF_{\min} + \frac{R_n}{G_s}\left|Y_s - Y_{opt}\right|^2 . \quad (1)$$

$G_s$ is the source conductance and $Y_s$ the source admittance. Optimum admittance results from the measured optimum source reflection coefficient $\Gamma_{opt}$ via

$$Y_{opt} = Y_0 \frac{(1-\Gamma_{opt})}{(1+\Gamma_{opt})} . \quad (2)$$

$Y_0$ is typically equal to 0.02 S. Measured noise parameters along with EKV3 model results (symbols and lines, respectively, as also throughout the rest of the text) are plotted in Fig. 1, up to 20 GHz for an NMOS device of L=100 nm, operating in saturation.

### B. $R_n$, $\Gamma_{opt}$ and $NF_{min}$ with Scaling and Inversion Level

To investigate the behavior of $NF_{min}$ with inversion level we use the inversion coefficient, IC introduced in [7], [8], which is given by simply normalizing drain current $I_D$ to a specific current $I_{spec}$, as $IC = I_D/I_{spec}$. The latter is given by (3) and depends on the effective mobility $\mu_{eff}$ and slope factor n, while $I_0$ is called the technology current [9]. $U_T$ is the thermal voltage.

$$I_{spec} = 2nU_T^2\mu_{eff}C_{ox}\frac{W_{eff}}{L_{eff}} = I_0 \cdot \frac{W_{eff}}{L_{eff}} \quad (3)$$

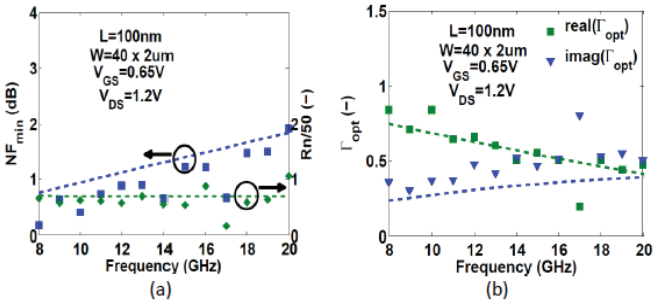


Fig. 1. (a) $NF_{min}$ and $R_n/50$, (b) real and imaginary part of $\Gamma_{opt}$ vs. frequency.

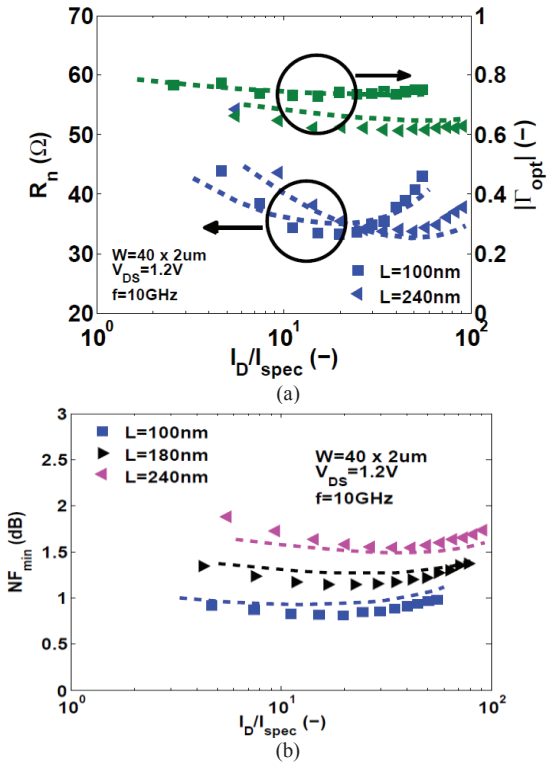


Fig. 2. (a) $R_n$ and $|\Gamma_{opt}|$, and (b) $NF_{min}$ vs. IC for NMOS devices of L values ranging from 240 nm to 100 nm.

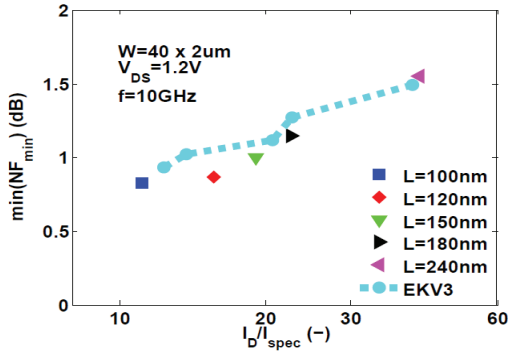


Fig. 3. Minimum values of $NF_{min}$ vs. IC for NMOS devices of different L.

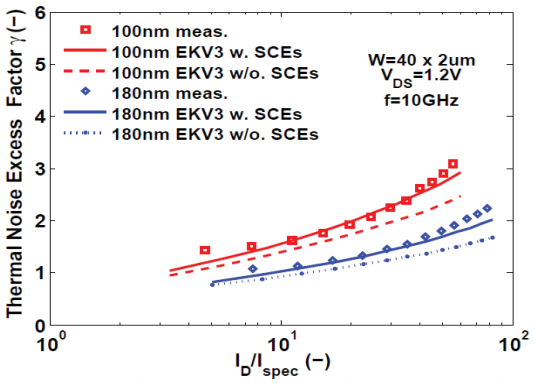


Fig. 4. γ vs. IC for NMOS devices of L=100 nm and L=180 nm, with and without accounting for SCEs.

For IC < 0.1 the device is in weak inversion (W.I.). Moderate inversion (M.I.) corresponds to 0.1 < IC < 10, whereas IC values greater than 10, denote strong inversion (S.I.) operation. $I_o$ amounts to 740 nA for the present NMOS devices.

Equivalent noise resistance, $R_n$ and magnitude of optimum source reflection coefficient, $|\Gamma_{opt}|$, are presented in Fig. 2 (a) with respect to IC for NMOS devices of L=100 nm and L=240nm. $NF_{min}$ is also plotted in Fig. 2 (b) versus IC for different nominal gate length NMOS devices operating in saturation at 10 GHz. The results are in line with those presented in [10]. It is obvious that as we scale down to 100 nm, $NF_{min}$ as well as $R_n$ minima move from higher to lower IC values. This is more evident in Fig. 3, where the minimum values of $NF_{min}$ are presented with respect to IC, for NMOS devices of nominal gate length ranging from 240 nm to 100 nm. It should be underlined that for L=100 nm, the minimum $NF_{min}$ value (0.82 dB) appears at the vicinity of M.I. to S.I., and specifically at IC=11.

### *C. Thermal Noise Excess Factor*

Noise in MOSFETs is dominated by the channel thermal noise given by (4), which is described by its power spectral density ($S_{id}$).

$$S_{id} = 4kT\frac{I_{spec}}{U_T}g_n \tag{4}$$

Thermal noise is characterized by the thermal noise excess factor γ and the thermal noise parameter δ, introduced by Van der Ziel [11]. Both are presented in (5) with $G_n$ representing the thermal noise conductance ($g_n$ is its normalized value).

$$\delta = \frac{G_n}{G_{dso}} \quad , \quad \gamma = \frac{G_n}{G_m} \tag{5}$$

δ is evaluated for zero $V_{DS}$, thus it has no specific meaning in terms of RFIC design.

On the other hand, the thermal noise excess factor γ, which represents the noise that is generated at the drain of a transistor, for a given gate transconductance, is of major importance since it is derived at any given operating point. The short-channel effects on thermal noise, such as CLM, VS and carrier heating, affect mobility and hence $G_m$, effective length, and γ [9]. γ is used for determining the noise figure of a common-source LNA [12]. Fig. 4 presents the thermal noise excess factor, with respect to IC, with and without accounting for SCEs. It is clear that γ is greatly underestimated when SCEs are neglected in noise calculations, especially for the shorter gate length device of L=100 nm and for operation in S.I.

## III. High Frequency Distortion Analysis

Distortion analysis in MOSFETs is usually expressed by the 3rd order products generated by the MOSFETs nonlinearities expressed in terms of 3rd order intermodulation input intercept points $P_{IP3}$ and $V_{IP3}$. The nonlinearities mainly arise from harmonics [13]-[15] induced by higher order derivatives of the channel current $I_D$ with respect to $V_{GS}$, especially by the 3rd order derivative $G_{m3}$, calculated via (6).

$$G_m = \frac{\partial I_D}{\partial V_{GS}}, G_{m2} = \frac{\partial^2 I_D}{\partial V_{GS}^2}, G_{m3} = \frac{\partial^3 I_D}{\partial V_{GS}^3} \quad (6)$$

In general, linearity FoMs are exported from DC measurements. However it is also useful to study these metrics at high frequency, since this would be more meaningful in terms of RFIC design. Therefore RF measurements were performed for several $V_{DS}$ and $V_{GS}$ values and linearity metrics were extracted at 1.1 GHz. $G_m$, $G_{m2}$ and $G_{m3}$ measurements as well as EKV3 simulation data are shown in Fig. 5 versus IC for the shorter device of L=100 nm biased in saturation. $P_{IP3}$ and $V_{IP3}$ are calculated through (7) and presented in Fig. 6 (a) and Fig. 6 (b), respectively, for the longest and shortest measured devices. $R_S$ is a matched input resistance equal to 50 Ω. The model results are in close proximity with measurements and recent published work [10], [14], [15].

Since for low distortion operation all linearity FoMs should be as high as possible, it is worth noticing that moving towards shorter length devices, the peak value of linearity metrics is moving to lower inversion levels, experiencing the same shift as $NF_{min}$, which for L=100 nm approaches the center of M.I. region (IC=1).

$$P_{IP3} = \left| \frac{2G_m}{3G_{m3}R_S} \right|, V_{IP3} = \sqrt{\frac{24G_m}{G_{m3}}} \quad (7)$$

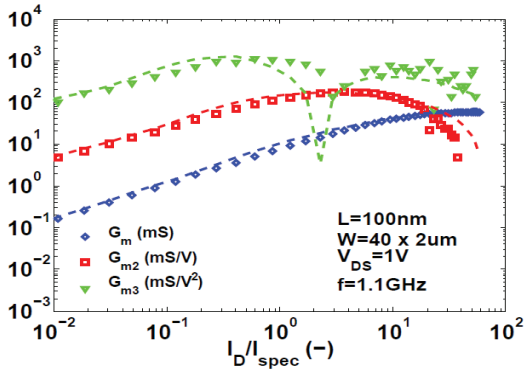


Fig. 5. $G_m$, $G_{m2}$ and $G_{m3}$ vs. IC.

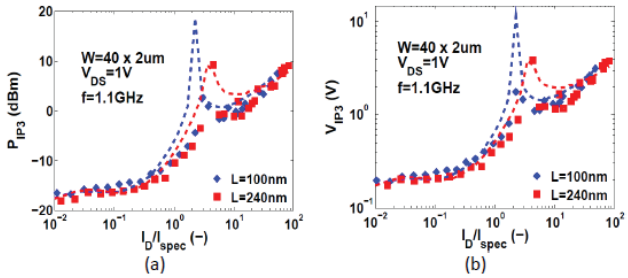


Fig. 6. (a) $P_{IP3}$, and (b) $V_{IP3}$ vs. IC for NMOS devices of L=100 nm and L=240 nm.

## IV. Figure of Merit for CS LNA

For characterizing a low-power LNA performance, an overall FoM is usually used, given by (8) [16]:

$$FoM_{LPLNA} = \frac{G_V f_{RF}}{(F-1)P_{cons}} \propto \frac{G_m f_T}{I_D} = TFP \quad (8)$$

$G_v$ is the voltage gain, $f_{RF}$ is the frequency of operation, F stands for the noise factor and $P_{cons}$ is the power consumption.

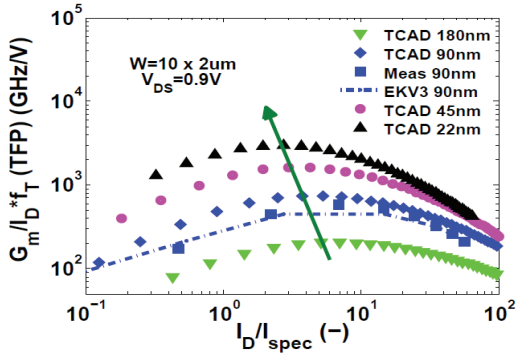


Fig. 7. TFP vs. IC for NMOS devices of L values ranging from 180 nm to 22 nm.

Recently, Taris et al. [16] showed that this low-power LNA FoM is proportional to TFP, when a CS topology is

considered. Moreover TFP becomes maximum in M.I. as shown in [17], [18] for 180 nm and 130 nm CMOS technologies, respectively. Therefore, it is meaningful to study its behavior with technology scaling. In Fig. 7, TFP for measured data, EKV3 model and TCAD simulations from 180 nm to 22 nm technology nodes, is plotted versus IC. It is evident that not only TFP improves with technology scaling, but also its peak value is shifted from higher to lower IC values, close to the center of M.I., when scaling down to 22 nm.

## V. Conclusions

In this work, we outline the relation between inversion coefficient, nominal gate length and FoMs essential for RFIC design, such as $NF_{min}$, $P_{IP3}$ and $V_{IP3}$. For this purpose RF and RF noise measurements of a 90 nm CMOS process were performed for a wide range of devices, bias points and frequencies. The inversion coefficient is used to indicate the shift of optimum performance close to or within the moderate inversion region. Moreover RF performance of a CS LNA topology, expressed in terms of TFP, is studied. Best performance is achieved close to the center of M.I. as technology scales down from 180 nm to 22 nm. Hence it is expected that approaching the sub-30 nm CMOS regime the existing trade-off among power consumption, noise and linearity will become more relaxed in the M.I. region.

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