A 65nm CMOS High-IF Superheterodyne Receiver with a High-Q Complex BPF

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Abstract — **We propose a highly reconfigurable superheterodyne receiver that employs a 3rd-order complex IQ charge-sharing band-pass filter (BPF) for image rejection and 1st-order feedback based RF-BPF for channel selection filtering. The operating RF input frequency of the receiver is 500 MHz–1.2 GHz with varying high-IF range of 33–80 MHz. All the gain stages are merely inverter-based g_m stages. The total gain of the receiver is 35 dB and in-band IIP3 at mid-gain is +10 dBm. The NF of the receiver is 6.7 dB, which is acceptable for the receiver without an LNA. The architecture is highly reconfigurable and follows the technology scaling. The RX occupies 0.47 mm^2 of active area and consumes 24.5 mA at 1.2 V power supply.**

I. Introduction

Integrated RF receivers (RX) are typically zero-IF or low-IF (i.e., homodyne) because of the well-known benefits, such as: high-level of integration, the use of low-pass filtering for channel selection, and avoidance of an external IF band-pass filter (BPF). Weak desired signals are likely accompanied by large blocking interferers. These blockers can dramatically degrade the receiver performance by causing gain compression and higher-order nonlinearities as well as increasing its noise figure (NF). Conventionally, these out-of-band blockers are filtered out by a bulky and expensive SAW filter placed prior to the LNA input. Since the RF wanted signal could be weak and the dynamic range requirements of a given specification need to be met, the gain of the LNA should be kept high and the blockers should be filtered out. Otherwise, the mixer and the following stages could get saturated. SAW-less receivers have been recently discussed in [1], [2]. They are all based on a homodyne architecture. Unfortunately, they all exhibit well-known homodyne RX issues, such as sensitivity to 1/f noise and varying dc offsets, finite IIP2, which will keep on getting worse with the inevitable scaling of the process techonology.

In this paper we propose a superheterodyne receiver of high-IF that solves the aforementioned issues of the homodyne receivers. Another integrated superheterodyne RX was proposed in [3]. It filters the blockers through an N-path filter, as opposed to the DT filtering approach here. However, the image folding issue is not addressed there. The image folding issues of prior attempts are solved here through a discrete-time (DT) charge-sharing filtering. On the other hand, the blockers are filtered through a feedback-based high-Q RF BPF. The new architecture is process scalable and highly reconfigurable.

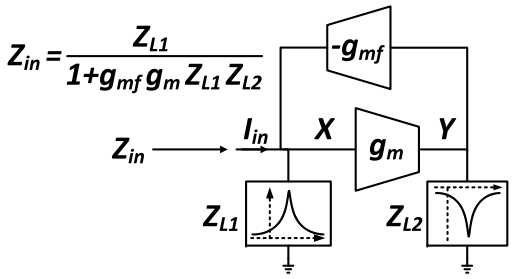

Fig. 1. The basic concept of impedance combinations.

The N-path filters offer high-Q BFP filtering with precise control of the center frequency through clock adjustment [3]. Despite a very high-Q filtering, N-path filters provide only around 7–16 dB of filtering rejection due to the poor switch on-resistance in mixers. On the other hand, this type of filter suffers from folding of images from $(N-1)f_{IF}$ and $(N+1)f_{IF}$ with a normalized gains proportional to $1/(N+1)$ and $1/(N-1)$ [3]. For example, the images of the 16-path filter fold onto the wanted signal via the 24 dB attenuation, which does not appear sufficient. Therefore, it is essential to use pre-filtering (i.e., pre-select, SAW, N-path) to get rid of the images, which degrade NF and causes image folding. Usually, the gain of LNAs is around 10–20 dB, which can saturate the output of an LNA at a presence of a blocker that can be as large as 0 dBm (600 mV p-p). Therefore, in order to prevent the saturation, it is needed to use the BPF right after LNA to attenuate the blockers.

II. High-Q RF BPF Structure

The novel idea of the high-Q RF BPF comes from a combination of two types of impedances. As shown in Fig. 1, the input current is converted to voltage at node X through multiplication by Z_{L1}. Then, it is converted to current and sinked on Z_{L2}. The resulting V_Y voltage gets fed back to input node V_X by a transconductance in the feedback path. As shown in Fig. 1, the input impedance of the circuit is $Z_{L1}/(1+g_{mf}g_mZ_{L1}Z_{L2})$. When the gain $g_{mf}g_mZ_{L1}Z_{L2}$ is smaller than unity, the input impedance is equal to Z_{L1}, which in this design happens at frequencies far from the wanted signal. On the other hand, the input impedance becomes $1/(g_{mf}g_mZ_{L2})$ in the case that $g_{mf}g_mZ_{L1}Z_{L2}$ is much larger than unity, which happens at frequencies very close to the wanted signal. The first impedance Z_{L1}

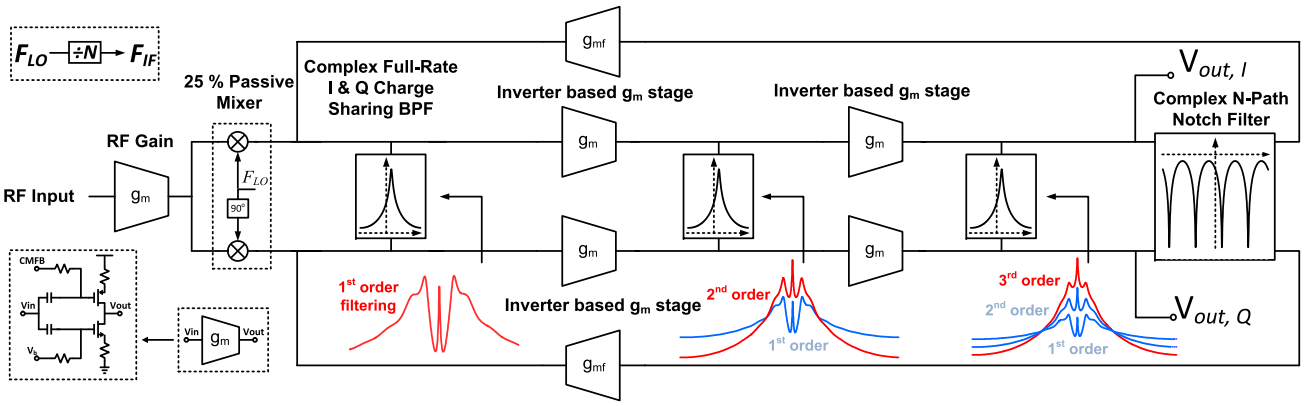

Fig. 2. Detailed block diagram and operation of the high-IF receiver with high-Q BPF.

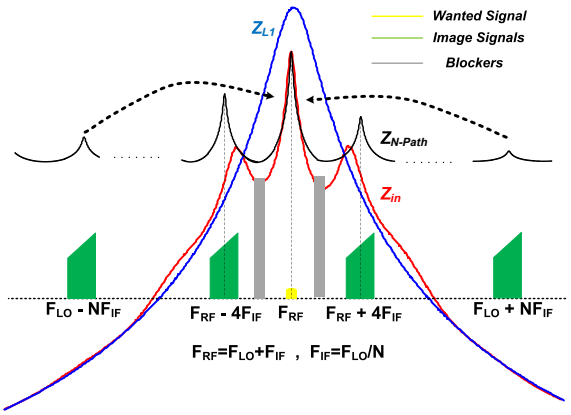

Fig. 3. Frequency translation of the high-IF receiver compared to a typical N-path filter.

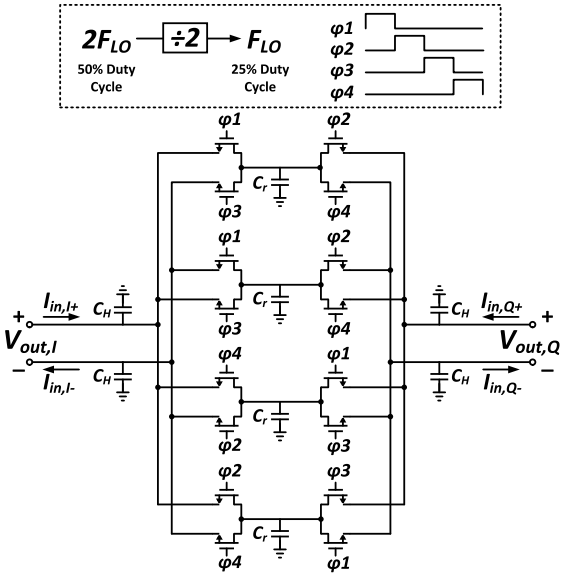

Fig. 4. Circuit level schematic of the wideband IQ charge-sharing BPF.

is a 3rd-order complex IQ charge-sharing filter, which acts here as a wide-bandwidth BPF centered at $+f_{IF}$ to filter out images of the wanted signal. The basic concept of IQ charge sharing filter was introduced in [4] for low-IF with low sampling rate.

The second impedance Z_{L2} is a complex 8-path notch filter (recently introduced in [5] for a real-valued version) to achieve a very sharp high-Q BPF at RF through feedback path. Fig. 2 depicts a detailed construction of a low-impedance node after the RF mixer for blockers with an extra filtering at image frequencies. Input matching of the circuit is provided by the input 50 Ω resistance. First, the RF input signal is converted to a current using a simple inverter-based g_m stage followed by a 25 % passive mixer clocked at f_{LO}. The complex output current of the mixer needs a complex low-impedance node for blockers to eliminate the saturation of the g_m output. As shown in Fig. 3, the blockers are attenuated because of the complex high-Q BPF, while the complex full-rate wideband IQ charge-sharing BPF (including the feedback) rejects other image components, including those at -f_{IF}. The filtered complex signals go through two similar wideband IQ filters for more attenuation of the images and amplification of the wanted signal. Output signals of the last (third) IQ filter go through a complex notch filter centered at $+f_{IF}$ followed by TIA in order to feed back the complex signals to the mixer output. The complex notch filter rejects the wanted signal and passes all blockers and unwanted signals, which get fed back through a transconductance (g_{mf}) and will be canceled at the mixer output.

Fig. 4 shows the concept of IQ charge-sharing wideband BPF. The input current is integrated into the total capacitor $C_t = C_H + C_r$ during four phases of the non-overlapping 25% full-rate LO clock. The full-rate operation means that it works at the maximum sampling frequency of $4f_{LO}$ to avoid decimation. The main drawback of an early decimation would be an unwanted folding due to the change of the sampling rate between stages. Therefore, in order to avoid aliasing, it is crucial to keep the sampling frequency at full rate. After each integration of the current into C_t of each quadrature path, a small portion of the total charge $\frac{C_r}{C_t} q_{in}$

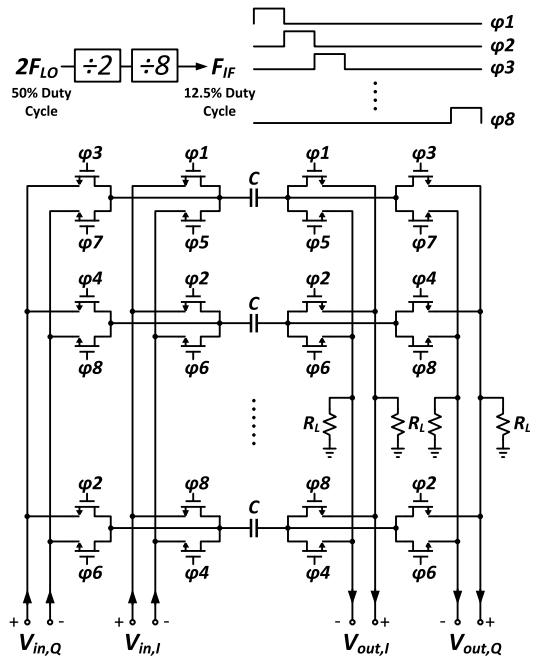

Fig. 5. Circuit level of the complex notch filter centered at f_{IF}.

is shared between the real and imaginary paths in the next clock cycle. This operation forms a complex filter with a transfer function given by

$$H(z) = \frac{Vout(z)}{Qin(z)} = \frac{k}{1 + (a + jb)z^{-1}}, \qquad (1)$$

where $k = 1/(C_H + C_r)$, $a = C_H/(C_H + C_r)$ and $b = C_r/(C_H + C_r)$. According to Eq. 1, the charge-sharing process forms a 1st-order complex filter centered at

$$f_c = \frac{f_s}{2\pi} arctan \frac{b}{a}. \qquad (2)$$

Therefore, it is possible to adjust the center frequency f_c by changing the coefficients a and b. However, it is not possible to make the filter very sharp because the DT charge sharing is a lossy operation, which increases bandwidth of the filter. f_c is a bit sensitive to the capacitance ratio mismatch, as compared with the N-path filter, in which the center frequency is exactly equal to the operating clock frequency. The main advantage of this structure is that the IQ charge-sharing BPF has a very robust filtering at frequencies located at $f_s/2$. As a result, it is feasible to use it as the wideband BPF centered at f_{IF} to reject image signals located at harmonics of f_{IF}. The other benefit of this filter is that its sampling frequency is equal to $f_s = 4f_{LO}$. Therefore, no unwanted folding occurs as compared to the N-path filter, which suffers from harmonics folding.

The proposed architecture offers several advantages over the state-of-the-art receivers. The high-IF RX eliminates the homodyne RX issues, such as LO feed-thorough, dc offset, 1/f noise and 2nd-order nonlinearity, which force all the active devices to be very large. Here, all the gain blocks are simple inverter-based g_m stages. All switches and capacitors, which are used in the filters, are amenable to the technology scaling. The proposed high-Q BPF has a superior image rejection as compared to the N-path filter. In mixer-based BPFs, such as the N-path filter, the rejection of the image components is ultimately limited by the mismatch between the LO clock of I and Q paths. On the other hand, there is no inherent limitation here on the level of image component rejection other than the NF degradation and power consumption of LO distribution.

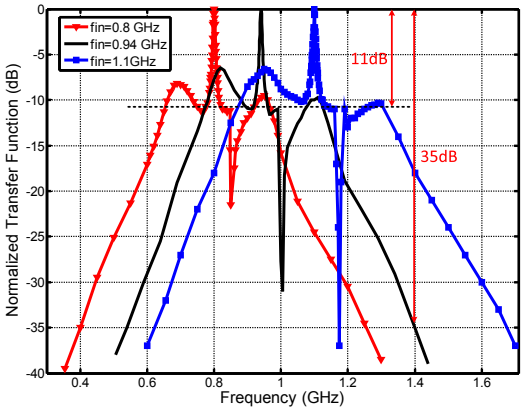

Fig. 6. Measured transfer function of the receiver.

The circuit of the on-chip complex notch filter is depicted in Fig. 5. The wanted signal at f_{IF} is downconverted by the mixers and filtered through the C-R filter, which acts as a HPF at dc. Then, the signal is upconverted to the IF frequency with the second mixer. Similarly to the N-path filter, harmonic mixing might also happen in the N-path notch filter. However, it is not an issue in this RX since the image components are already filtered out via the preceding complex wideband IQ charge-sharing filter. The 8-phase clock for the notch filter is provided by dividing the main LO by 2 and then further dividing it by 8, through the chain of ÷2 dividers, The ÷2 divider ensures that the 8-phase output clocks are non-overlapped.

III. Measurement Results

The receiver (RX) chip is fabricated in 65 nm CMOS technology. The input signal lies in the range of 500 MHz to 1.2 GHz, corresponding to the IF frequency of 33.33 MHz to 80 MHz. The C_H and C_r capacitors are binary adjustable between 3.8–11 pF and 1.2–2 pF, respectively. The notch filter capacitance (C in Fig. 5) is 5 pF . The measured RX gain is 35 dB and the NF is 6.7 dB at the max gain. The in-band IIP3 is +10 dBm at the 25 dB gain with a two-tone test at +5 MHz and +10 MHz; it is 0 dBm at +1 MHz and +2 MHz. The measured RX transfer function at various LO frequencies is demonstrated in Fig. 6. The notch in the transfer function is due to the dc block capacitors in the feedforward path of the g_m stages shown earlier in Fig. 2.

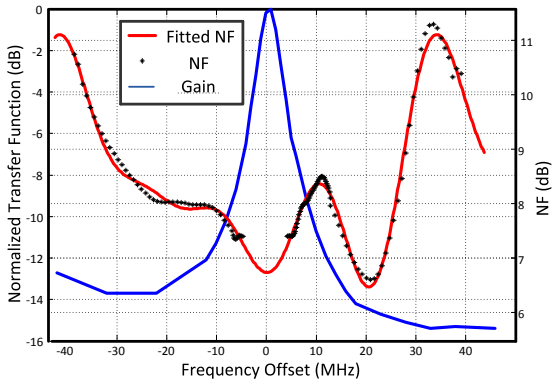

Fig. 7. Measured transfer function and NF around desired RF frequency versus frequency offset.

TABLE I
SUMMARY AND COMPARISON WITH STATE-OF-THE-ART

	This work	[3]
CMOS Technology	65 nm	65 nm
Active Area	0.45 mm^2	0.76 mm^2
Power Consumption	24.5 mA	21 mA
Rejection @ f_{LO}-7f_{IF} f_{LO}+9f_{IF}	<-53 dB	<-18 dB
NF (dB)	6.7	2.8
IIP3 (dBm) @ 1M,2M	0	—-
IIP3 (dBm) @ 5M,10M	+10	—-
IIP3 (dBm) @ 10M,20M	+2	—-
BW (MHz)	4.5	4
RX Frequency (GHz)	0.5-1.2	1.8-2.2

This further improves IM2 and clock feedthrough. The BW of the RX is 4.5 MHz. It can be seen that the rejection around the RF frequency is more than 10 dB. The images at $7f_{IF}$ and $9f_{IF}$ could theoretically be folded into the wanted signal in the complex notch filter. However, this is not an issue because these images are already rejected through 35 dB attenuation in the IQ charge-sharing BPF. Note that no pre-select filters are used here. Therefore, any possible folded images from $7f_{IF}$ and $9f_{IF}$ are first attenuated by 53 dB (35 dB+18 dB). On the other hand, it should be possible to employ the high-Q N-path filter in the feedforward path to improve the filtering function after the IQ charge-sharing BPFs. The two "shoulders" around f_{RF} in Fig. 6 are due to the transition from the filtering function of the sharp high-Q RF BPF to the IQ charge-sharing BPF. The measured close-in transfer function and NF are depicted in Fig. 7.

The Q-factor of the BPF is 208 and the total power consumption of the RX is 24.5 mA. The performance of the RX is summarized and compared in Table I with the only other published high-IF RX [3]. A clock generation circuit consumes 6 mA at 1.2 V. The active area of RX including the clock generation is 0.45 mm^2, as shown in Fig. 8. The presented high-IF RX with high-Q complex BPF offers superior filtering at RF frequencies in addition to the strong filtering of the image components, while achieving

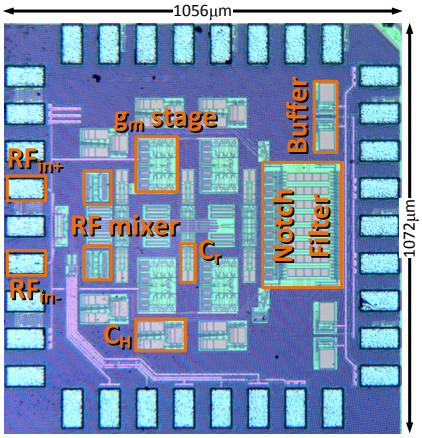

Fig. 8. Chip micrograph.

low power consumption in a very small chip area. It should be emphasized that the LNA was not implemented in this chip in order to better characterize the linearity and noise. Hence, the NF given in Table I is high, just as expected, due to the low gain of the RX front-end (i.e., g_m & mixer) stage, which is about 6 dB.

IV. Conclusion

The first superheterodyne receiver that rejects image folding is proposed and demonstrated. The concept of impedance combination is utilized to realize the complex high-Q RF BPF that rejects the image folding that has prevented the widespread adoption of high-IF RX architectures in the past. The RX occupies 0.45 mm^2 and consumes 24.5 mA at 1.2 V.

V. Acknowledgments

Authors would like to thank W. Straver and A. Akhnoukh of TU Delft for the measurement support and to HiSilicon for chip fabrication.

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