Dual-Core High-Swing Class-C Oscillator with Ultra-Low Phase Noise

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***Abstract*— We propose an ultra-low phase noise oscillator topology that works on the premise that coupling a second identical oscillator core would reduce the overall phase noise by 3 dB. For each core, a high-swing class-C oscillator is used to achieve the lowest phase noise. The realized oscillator is tunable from 4.07-4.91 GHz, drawing 39-59 mA from a 2.15 V power supply. The measured phase noise is -146.7 dBc/Hz and -163.1 dBc/Hz at 3 MHz and 20 MHz offset, respectively, from 4.07 GHz carrier. This is the lowest ever reported phase noise in bulk CMOS IC. This phase noise meets GSM900 normal basestation receiver and mobile station transmitter standards, which have the toughest phase noise requirements in cellular communications.**

I. Introduction

A modern wireless system normally consists of one main CMOS IC, which performs most of the system functionality, some external discrete components (i.e., external inductors, capacitors, resonators, etc.), and perhaps one or several costly GaAs or SiGe ICs. Nowadays, the key challenge is to reduce the total system cost. Therefore, there is an effort to integrate non-CMOS ICs and all external components into the main CMOS chip. Some cellular transmitter/receiver (TX/RX) oscillators require extremely low phase noise for up-/down-conversion of the modulating signal. For example, TX oscillator in GSM900 mobile station (MS) standard should have a phase noise better than -162 dBc/Hz at 20 MHz offset from the 915 MHz carrier. Likewise, the RX oscillator must satisfy the toughest phase noise requirements imposed by the GSM900 normal basestation (BTS) specification, which is better than -147 dBc/Hz at 800 kHz offset from 915 MHz carrier.

Nowadays, this BTS RX phase noise requirement is achieved using expensive SiGe/GaAs ICs or with assistance of high quality discrete components. A fully-integrated oscillator in bulk CMOS meeting this stringent requirement has not been demonstrated in the literature. In this paper, we present design and implementation of such an oscillator by means of parallel-coupled oscillator cores.

II. Design of Ultra-Low Phase Noise Oscillator

A. Reducing Phase Noise in LC Tank Oscillator

A general phase noise formula that can be used for an LC oscillator is Leeson's equation:

$$L(\omega_m) = F\frac{4kTR}{V_0^2}\left(\frac{\omega_0}{2Q\omega_m}\right)^2 \qquad (1)$$

where, k is Boltzmann's constant, T is the absolute temperature, R is an equivalent parallel tank resistance, V_0 is the differential tank oscillation amplitude, ω_0 is the oscillation frequency, ω_m is a frequency offset from ω_0, and Q is the tank quality factor. In this equation, noise factor F is a constant, which depends on oscillator topology and its parameters. This parameter for conventional cross-coupled (i.e., class-B) oscillator and class-C oscillator has been calculated in [1] and [2], respectively.

Based on (1), to reduce phase noise at a given oscillation and offset frequencies, one would first maximize Q of the tank. However, the inductor Q is rather physically limited in each process technology. Oscillation amplitude of an LC oscillator before reaching the output saturation can be estimated by:

$$V_0 = \alpha I_{bias} \cdot R \qquad (2)$$

where α is a bias conversion factor into the fundamental current harmonic. For class-B oscillator, α is $2/\pi$ and for class-C it is about a unity [2]. Hence, a class-C oscillator can have a lower bias current than the conventional cross-coupled one with the same oscillation amplitude. By increasing the bias current and maximizing the oscillation amplitude V_0, the phase noise can be reduced. Note, that after a certain point, V_0 gets saturated (less than $2V_{DD}$) and further increasing bias current degrades the phase noise ([1], [3]).

The other important parameter in the design of a low phase noise oscillator is an inductance value (L) of the LC tank. This parameter affects the equivalent parallel resistance of the tank, which is

$$R = QL\omega_0 . \qquad (3)$$

By decreasing inductance value and, consequently, R (while managing to keep Q constant), phase noise can be reduced. However, the bias current should be increased to have the maximum oscillation amplitude V_0 again. Nevertheless, this will not change the oscillator FoM, which is:

$$\text{FoM} = \left(\frac{\omega_0}{\omega_m}\right)^2 \frac{1}{L(\omega_m)\cdot V_{DD}\cdot I_{total(mA)}} . \qquad (4)$$

Substituting (1) and (2) into (4) and assuming I_{total} is the same as I_{bias}, we have:

$$\mathrm{FoM} = \frac{4Q^2 \cdot \alpha}{F \cdot 4kT} \times \frac{V_0}{V_{DD}} \times 10^{-3}. \quad (5)$$

As (5) shows, the FoM depends on Q, α, F and V_0/V_{DD} but neither on L value nor R directly.

B. High-Swing Class-C Oscillator with RC Coupling

The topology we use in this design is a high-swing class-C (HSCC) oscillator proposed in [3]. Class-C operation of the oscillator gives a higher bias conversion factor α in (2) and (5), which leads to a higher FoM compared to class-B. Moreover, the high output swing of this oscillator allows maximizing the oscillation amplitude to almost $2V_{DD}$ [3]. Fig. 1 depicts the modified HSCC oscillator used in this work. In the oscillator core, instead of a transformer used in [3], a center-tapped inductor and two coupling capacitors $C_{c1,2}$ are used. Also $R_{b1,2}$ are used to set bias voltage of $M_{1,2}$. In the bias control circuit, $M_{3,4}$ mirror currents of $M_{1,2}$ with a ratio much less than one (1/8 was implemented in this chip). The mirrored currents are summed at node labeled V_{ctrl} and subtracted from I_{ref} current. The resulting current is integrated on the bypass capacitor C_b and a control voltage V_{ctrl} is thus generated. This voltage is fed back to the oscillator core through the bias resistors $R_{b1,2}$.

The modified HSCC oscillator works as follows: At the beginning, suppose the oscillation is not started yet. In this condition, $M_{3,4}$ are diode-connected through $R_{b1,2}$. Since $V_{g1,2}$ are equal to V_{ctrl}, I_{ref} is mirrored into M_1 and M_2. If this current satisfies the oscillation condition, the oscillator core starts to oscillate. As the oscillation amplitude increases, average currents of $M_{1,2}$ and, consequently, $M_{3,4}$ are increased. The excess current of $M_{3,4}$ discharge C_b and accordingly reduces V_{ctrl}. In steady-state, the average current of $M_{3,4}$ will decrease to I_{ref}. A larger width of the switching pair at the same bias current decreases V_{ctrl} and the firing angle. By proper choice of $M_{1,2}$ sizes, V_{ctrl} would be set to a small overdrive voltage V_{od} at steady-state resulting with the maximum possible tank swing.

To achieve a very low phase noise oscillation, one might pick a high Q inductor at first. Then, as discussed in Section II.A, one would try to lower the inductance value by shrinking the inductor radius or reducing its number of turns. Although a multi-turn inductor might have a slightly higher quality factor, by choosing a 1-turn inductor, a much lower inductance value can be obtained. Reducing the radius of an inductor results in a lower inductance. However, after a certain point, the quality factor drops dramatically, which is not desirable. By trading off between a low inductance value and a high Q, we can find

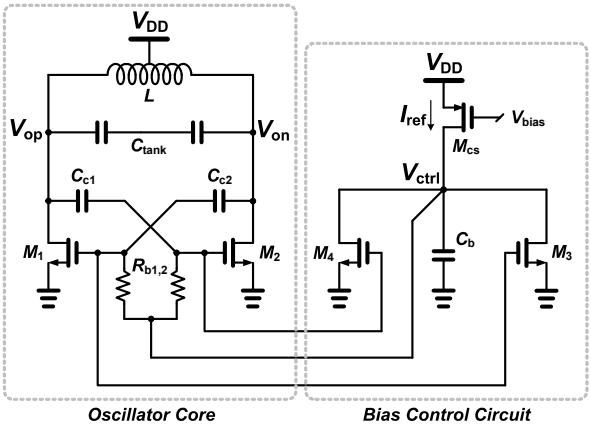

Fig. 1. High-swing class-C oscillator with RC coupling.

the optimum point: A higher inductance gives a higher phase noise, and a lower inductance drops Q and thus degrades the phase noise. At that point, the oscillator could have the lowest possible phase noise in a given process technology with a good FoM.

After optimizing the inductor, capacitor bank, oscillator structure, then maximizing the output swing and oscillation amplitude, the final oscillator could have the lowest possible phase noise. What to do if even a lower phase noise is required? How to break this limit?

C. Breaking the Low Phase Noise Limitation

We now propose an idea to break this limitation through the use of parallel-coupled oscillator cores. Suppose that each of the oscillator cores is designed based on the abovementioned discussion to achieve the lowest practically possible phase noise. By connecting N identical oscillator cores in parallel, the final phase noise would be:

$$L_N(\omega_m) = F\frac{4kTR}{V_0^2 N}\left(\frac{\omega_0}{2Q\omega_m}\right)^2. \quad (6)$$

This ultra-low phase noise oscillator has N-times lower phase noise than each of the single cores. Obviously, the total power consumption would be N times higher. This will maintain the FoM as per (4). For example, the phase noise of the dual-core HSCC should be 3 dB lower than that of each of the cores. Also, phase noise can be improved by 6 dB if 4 cores are connected in parallel.

In this way, there would be no limitation on how low the phase noise can reduce for such an integrated oscillator with limited inductor Q and supply voltage. However, the lower phase noise would come at a cost of proportionately higher power consumption and area.

Fig. 2 depicts this idea for N=2, i.e., a dual-core HSCC oscillator. Two identical HSCC oscillator cores have been 'coupled' in parallel. So, they are locked oscillating in-phase. In this way, equivalent current noise of core #1

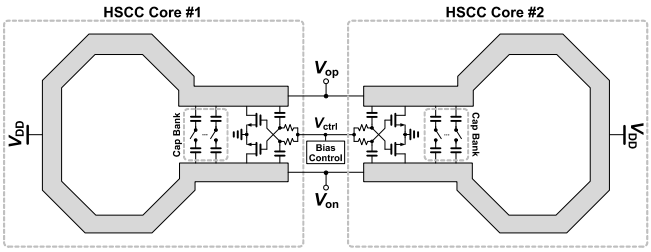

Fig. 2. Dual-core high-swing class-C oscillator.

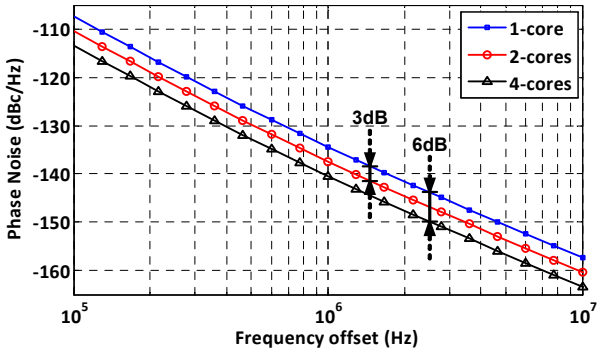

Fig. 3. Phase noise simulation of a single-core, dual-core and quad-core oscillator at 4.7 GHz.

experiences twice the capacitance and therefore its phase noise contribution is reduced by 6 dB. Similarly, phase noise contribution of core #2 is reduced by 6 dB. These two contributions originated from core #1 and #2 are uncorrelated, thus their powers are summed up. Hence the total phase noise is reduced by 3 dB.

In the dual-core oscillator of Fig. 2, each of the inductors has its own local capacitor bank. Hence, the high resonance current of each LC tank gets circulated within the same LC tank. In each cycle, the switching pairs inject impulse-like currents into their own cores. Therefore, in an ideal case (completely matched cores) no static current is passing through the wires inter-connecting the two cores. Nonetheless, a very small noise current (with average of zero) is going back and forth through these wires. In case of a small mismatch between the cores, a small cyclic current at the fundamental frequency goes through the inter-connection wires to balance the cores. Therefore, a small mismatch does not affect the phase noise noticeably. Since the inter-connecting wires do not carry high currents, their impedance does not play a critical role. It should be low enough to only carry the mismatch and the noise currents. Hence, for an oscillator with a large number of cores, long connection wires and their impedance should not be a big concern. Circuit simulation results in Fig. 3 compare the phase noise of three oscillators: a single-core oscillator, a dual-core one and a quad-core one. As depicted, phase noise of the dual-core and quad-core oscillators are 3 dB and 6 dB better than of the single-core, respectively. These results validate (6).

III. Experimental Results

A. Implementation

The dual-core high-swing class-C (HSCC) oscillator has been implemented in TSMC 65nm CMOS with ultra-thick metal option. In this implementation, the HSCC oscillator core uses a standard center-tapped inductor from the inductor library provided in the process technology design kit. Therefore, the design of this oscillator would be much easier and faster than the designs in [2]-[5] with transformer design and optimization that require extensive electromagnetic simulations. The inductor used here for each core has one-turn giving 220 pH.

As has been shown in Fig. 2, the capacitor bank of each LC tank has been placed in the closest possible position to its inductor. This minimizes interconnection parasitics to avoid degradation of the tank quality factor. The capacitor bank has a fixed capacitor and five binary-weighted switchable capacitors for tuning range demonstration. The capacitors used in the tank are all of metal-oxide-metal (MoM) type. Simulation shows that the total quality factor of the LC tank ranges from 22.5 to 25.5.

As the absolute output voltage of this oscillator would be as high as $2V_{DD}$, transistor breakdown and reliability are of concern. Value of the coupling capacitors $C_{c1,2}$ has been chosen such that a lower swing is seen by the gates of the transistors. To have the lowest phase noise by maximizing the oscillation amplitude, thick-oxide transistors have been chosen in order to use a higher supply voltage. This oscillator has been designed for a 2.15 V supply voltage and ensures a good reliability and very long life time for the transistors.

B. Measurement Results

The dual-core HSCC oscillator has an output frequency ranging from 4.07 GHz to 4.91 GHz, giving 18.6% tuning range. The oscillator drains 39 mA to 59 mA from a 2.15 V power supply. Fig. 4 shows the measured phase noise at 4.07 GHz output. Calculated flicker noise corner frequency in this figure is about 130 kHz. It increases to about 300 kHz at 4.91 GHz because of switching off all the capacitors. In Fig. 4 some of the toughest phase noise requirements of cellular communication standards have been plotted, while they have been normalized for our measurement frequency. The measured phase noise is well below the receiver LO purity specifications of GSM900 MS and DCS1800 MS and normal BTS. The phase noise is also 0.6 dB below the toughest GSM900 normal BTS at 800 kHz offset. It also meets mobile station (MS) transmitter standards of GSM900 and WCDMA band VIII

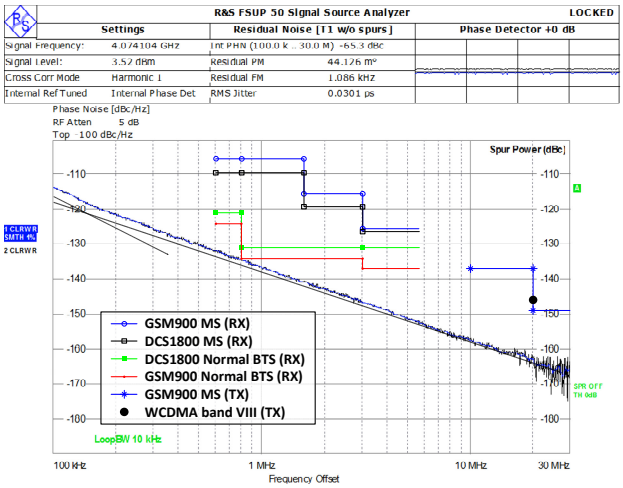

Fig. 4. Measured phase noises at 4.07 GHz. Specifications are normalized to the carrier frequency.

with 14 dB and 17 dB margin. To the best of our knowledge, this is the first-ever reported oscillator in CMOS IC that meets all these requirements with lowest-ever reported phase noise. This phase noise could be easily lowered by 3 dB by adding two more oscillator cores.

Table I summarizes the dual-core HSCC oscillator measurements and compares them with state-of-the-art low phase noise oscillators. This oscillator has the lowest phase noise of -159.7 dBc/Hz and -176.1 dBc/Hz normalized to the 915 MHz carrier at 3 MHz and 20 MHz offsets, respectively. Phase noise of this oscillator at 3 MHz offset with its corresponding FoM is plotted in Fig. 5 within the tuning range. Fig. 6 shows the chip micrograph.

IV. Conclusion

In order to break the phase noise limitations of practical CMOS oscillators, two high-swing class-C oscillators are coupled to each other. Doing so can improve phase noise by 3 dB. The implemented dual-core class-C oscillator shows lowest phase noise of 176.1 dBc/Hz at 20 MHz normalized to the 915 MHz carrier. The oscillator is tunable from 4.07-4.91 GHz, drawing 39-59 mA from a 2.15 V power supply. Measured FoM within the tuning range is 189 dB.

TABLE I: Comparison of Ultra-Low Phase Noise Oscillators

		This Work	ISSCC13 [4]	ISSCC12 [5]	ISSCC12 [6]	RFIC07 [7]	JSSC06 [8]
Description		Dual-Core Class-C	Class-F	Clip & Restore	ClassB/C	Colpitts	ClassB
Technology		65nm	65nm	65nm	55nm	130nm	90nm
Tuning Range (GHz)		4.07-4.91 (18.6%)	2.94-3.78 (25%)*	3.64-4.03 (10.2%)*	3.35-4.6 (31.44%)*	1.5-1.65 (9.6%)	3.21-4.1 (24.3%)
Frequency (GHz)		4.07	3.7	3.92	3.35	1.56	0.915
Phase Noise (dBc/Hz)	3MHz	-146.7	-142.2	-141.71	-142	-150.38	-149
	20MHz	-163.1	-158.6	-158.18	-158.48	-166.85	-167
Phase Noise norm. to a 915MHz carrier (dBc/Hz)	3MHz	-159.7	-154.3	-154.35	-153.3	-155.02	-149
	20MHz	-176.14	-170.7	-170.8	-169.75	-171.49	-167
Supply Voltage (V)		2.15	1.25	1.2	1.5	3.3	1.4
Current (mA)		59	12	21.5	18	88	18
FoM @ 3MHz (dB)		189	192.2	189.9	189	180	184.6

* After division by 2

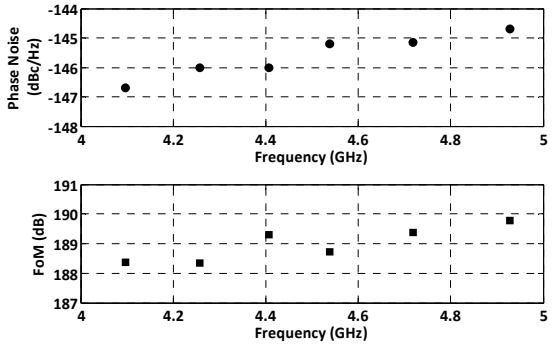

Fig. 5. Measured phase noise and FoM at 3 MHz offset versus carrier frequency.

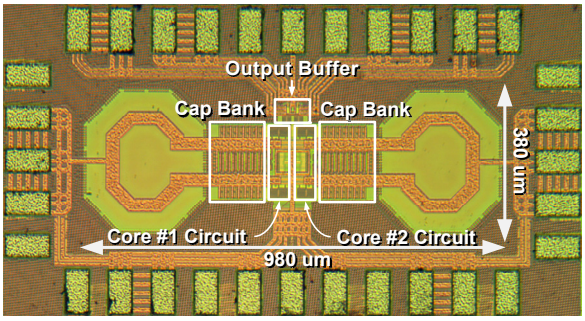

Fig. 6. Chip micrograph of the dual-core HSCC oscillator.

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