A Sub-1mW 5.5-GHz PLL with Digitally-Calibrated ILFD and Linearized Varactor for Low Supply Voltage Operation

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***Abstract*—This paper proposes an ultra-low-power 5.5-GHz PLL which employs a divide-by-4 injection-locked frequency divider (ILFD) and linearity-compensated varactor for low supply voltage operation. The digital calibration circuit is introduced to control the ILFD frequency automatically. The proposed varactor, which applies a forward-body-bias (FBB) technique, is employed for linear-frequency-tuning under the power supply of 0.5 V.**

The proposed PLL was fabricated in 65 nm CMOS. With a 34.3-MHz reference, it shows a 1-MHz-offset phase noise of −106 dBc/Hz, a reference spur level lower than −65 dBc, and the total power consumption of 950 μW at 5.5 GHz.

***Index Terms*—Injection-locked oscillators, phase-locked loop, Class-C VCO, CMOS, low power**

I. Introduction

Power saving is one of the main concerns of today's analog/RF frontend design, which allows longer battery runtime in wireless devices such as mobile terminals and sensors. In an analog/RF front-end, one of the most power-consuming blocks is phase locked loop (PLL) that generates carrier signals with low phase noise. Especially, voltage-controlled oscillators (VCO) and frequency divider (FD), which are main components composing a typical analog PLL, require higher power consumption compared with other PLL components. The use of low-voltage supply is a common approach to lower power consumption of such components [1], [2]. However, it is quite difficult to achieve low voltage operation in PLL since the limited threshold voltage of MOS transistors prevents it from getting sufficient performance such as maximum operation frequency and phase noise. It also causes the PLL operation unstable because the active control-voltage range of a varactor as well as the output-voltage range of a charge pump would be narrower.

This paper proposes a PLL that employs an ultra-low-power divide-by-4 injection-locked frequency divider (ILFD), whose output frequency is controlled by the digital calibration circuit automatically. Furthermore, the linear tuning characteristics with a forward-body-biased (FBB) varactor make the PLL operation stable even under the supply of 0.5 V.

II. Proposed PLL

Fig. 1 shows proposed PLL architecture, which is based on a type-2 charge-pump PLL. The PLL consists of a phase/frequency detector, a charge pump, a loop filter in addition to an *LC* VCO and a divider chain. The digital calibration circuit which controls the free-running frequency of the ILFD is also applied.

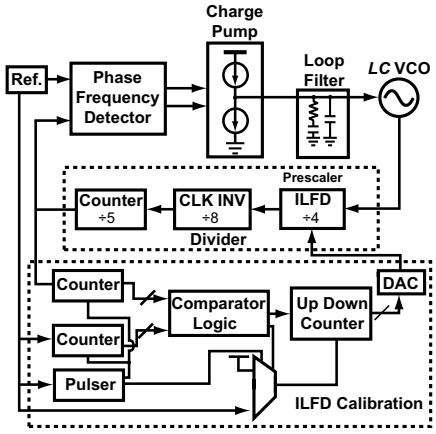

Fig. 1. Proposed PLL.

A. Proposed ILFD

The first stage of divider chain usually requires much power consumption in high-frequency-operation PLL because the power consumption is proportional to the operation frequency. Among many types of divider such as CML-type divider and E-TSPC-type divider [2], ILFD is attractive for low power and low voltage operation because it can be input high frequency signals even in low voltage and has high output swing. In addition, the ILFD can divide input signals by various ratio higher than 2. As a result, it can achieve lower power consumption since the number of divider stages is reduced [3]. However, sufficiently wide lock range of the ILFD is required for the stable operation of PLL, especially in high division ratio.

Fig. 2 shows a proposed divide-by-4 ILFD based on [3] proposed in our previous work. The ILFD is based on a two-stage ring VCO which has delay control terminals (V_{bn},V_{bp}) for frequency tuning. For the low-voltage operation, a forward-body-bias (FBB) technique is employed in delay cells. To achieve divide-by-4 characteristics, the ILFD employs the *double-switch injection* technique. By applying the injection switches for the I/Q output of the ILFD simultaneously, the ILFD has wider lock range in the case of dividng-by-4.

To achieve further wide lock range, the proposed ILFD has differential input nodes, as shown in Fig. 2. V_{injn} is

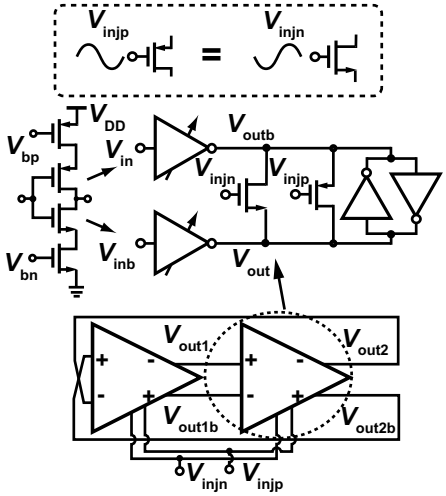

Fig. 2. Proposed divide-by-4 ILFD.

injected to nMOS switches and V_{injp} is injected to pMOS switches. These two differential inputs, that are injected to the nMOS and pMOS respectively, have the same function. Therefore, the balance between differential VCO outputs can be improved and the lock range of the ILFD is also widened.

B. ILFD calibration

To adjust the free-running frequency of the ILFD, circuits for the digital calibration that consist of two counters, a comparator-logic, a pulser, a MUX, a up-down counter and a digital-to-analog converter (DAC) is applied as shown in Fig. 1. When ILFD is calibrated, power supply of VCO is disabled. This means that ILFD oscillates under free-running condition. Two counters measure the output of divider and reference signal respectively. The output of two counters are compared in the following comparator-logic circuit and used in controlling the mode of up-down counter ("up" or "down"). The outputs of the up-down counter adjust the control code for the DAC. The DAC converts the digital code into analog control voltage for frequency tuning of ILFD. The 8-bit DAC has an resolution of about 2 mV. When the comparator-logic judges that the divided- and the reference-signal frequency are same, the MUX stops to supply the clock for the up-down counter. Then, the DAC keeps the control voltage of the ILFD constant. The pulser makes pulses every eighteen periods of the reference signal, and resets the counter to prevent overflowing of counters.

C. VCO

Fig. 3 shows the proposed Class-C VCO. Bias circuit [4] is employed to control the gate bias of the VCO. To achieve the stable operation of PLL under low supply voltage, a linear-region-compensated varactor is proposed.

1) VCO linearity: Using the low supply voltage is good for power reduction, however, causes non linearity of the VCO over the whole control voltage range because the active control voltage range of the VCO in the low supply voltage would be narrower. In this case, the active voltage

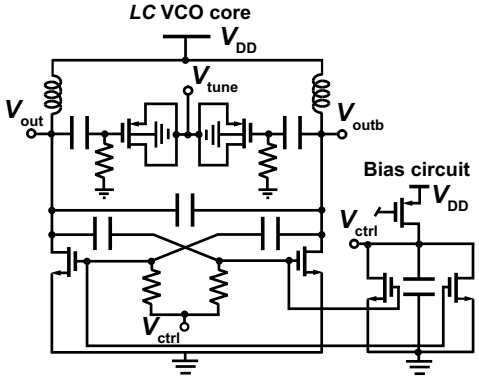

Fig. 3. Proposed Class-C VCO.

range cannot match the linear region of the varactor which is fundamentally used in the normal supply voltage operation, as shown in Fig. 4. The non-linearity of the VCO may deteriorate the PLL stability and phase noise characteristics.

Numerous methods for linear frequency tuning of VCO have been proposed. A distributed varactor biasing technique parallels with some single biasing varactors with same size and different gate bias, and sums the linear region of different varactors [5]. In [6], some different frequency tuning voltage generated by voltage level shifters control the varactor arrays. The method using the tuning voltage converter combines the non-linearity of the VCO and voltage converter [7]. As a results it achieves linear characteristics in total. These previous works have achieved good tuning linearity, however, cannot work effectively in the low voltage region about from 0 V to 0.2 or 0.3 V which is the threshold voltage of the MOS transistor. It is not critical under the normal supply voltage of 1.2 V or higher than 1.2 V because the wide-linear-tuning region can be achieved. On the other hand, the active control voltage range under the low supply voltage is narrow. Thus, these methods are not effective.

In addition, since the output-voltage range of a charge pump would also be narrow under the low supply voltage, the linear region of the varactor is desirable around $V_{\mathrm{DD}}/2$, where the charge pump can works effectively. When the supply voltage is 0.5 V and $V_{\mathrm{DD}}/2$ = 0.25 V, the linear region around $V_{\mathrm{DD}}/2$ cannot be achieved by the previous works [5]–[7].

To solve this problem, a linearized varactor for the low voltage operation is proposed as shown in Fig. 3. Proposed varactor is based on the conventional single biasing varactor [5]. In this case, the gate bias of the pMOS varactor is fixed to ground. To shift the linear region of the varactor to lower control voltage, the FBB is applied to the pMOS varactor to lower the threshold voltage. With this technique, the linear region of the varactor shown in Fig. 4 is shifted to about half V_{DD} when the supply voltage is 0.5 V. Therefore, stable operation of the PLL under low supply voltage can be expected.

Fig. 5 shows the simulation results of VCO tuning characteristics and its VCO gain (K_{VCO}) with and without FBB for the varactor. The linear region without FBB is

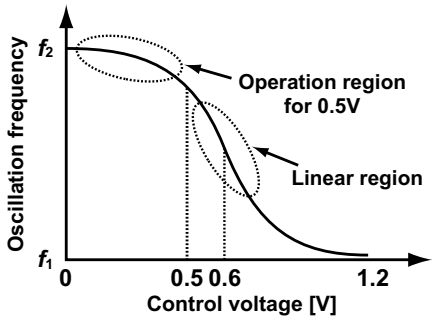

Fig. 4. VCO tuning characteristic.

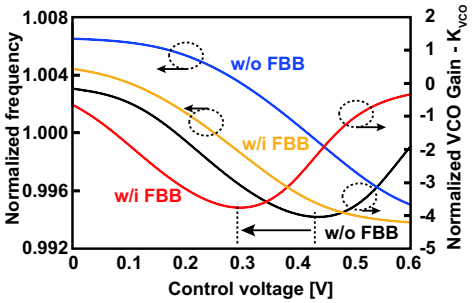

Fig. 5. VCO tuning characteristic and VCO Gain w/o and w/i FBB.

located at higher voltage than 0.4 V, which is lowered by the gate bias of the varactor. However, it is not sufficient because the output-voltage range of the charge pump would also be narrower under low supply voltage and the charge pump cannot work effectively. On the other hand, Fig. 5 also depicts that the linear region can be shifted by about 0.1 V and be around $V_{DD}/2$ by means of the threshold voltage reduction caused by the FBB.

2) Class-C VCO: Among many types of low power VCOs such as class-C VCO [8] and current-reuse VCOs [9], class-C VCO is selected because it is suitable for a low-voltage-operation. As shown in Fig. 3, the bias control circuit for the gate bias [4] is applied to control the operation condition of VCO. The bias control circuit works as an amplitude detector. In the start-up condition, the gate bias of VCO is approximately V_{DD} and works as a conventional cross-coupled LC VCO. On the other hand, when the VCO starts to oscillate and the oscillation amplitude increases, the gate bias is decreased, and then, is fitted the VCO to oscillate in the class-C operation.

D. Other PLL components

In Fig. 1, there are other PLL components, including a phase/frequency detector (PFD), a charge pump, a loop filter, and a divider chain. A conventional three-state PFD is implemented, which has capability of low-supply operation. A current-matched charge pump is employed to suppress the spur level [10]. Fig. 1 also shows a second-order lag-lead filter as an LF. The frequency divider chain has division ratio of 160. Clocked-inverter-type dividers [11] are applied as well as the ILFD to reduce power consumption under the low supply voltage.

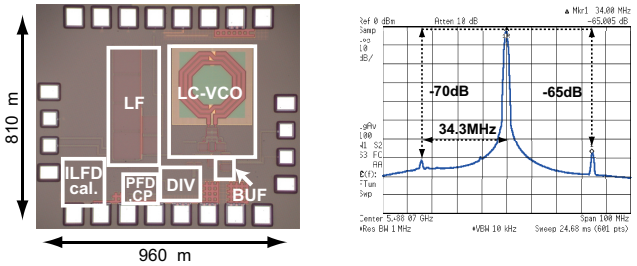

Fig. 6. (a) A chip micrograph of the proposed PLL. (b) Measured spectrum at f_{out} = 5.49 GHz.

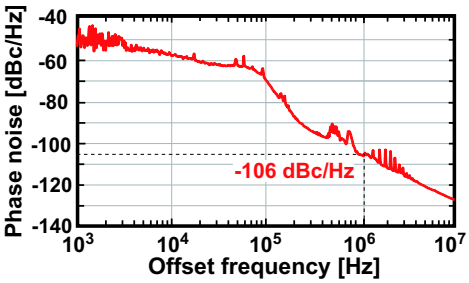

Fig. 7. Measured phase noise at f_{out} = 5.49 GHz.

III. Measurement Results

Fig. 6 (a) shows a chip micrograph of the proposed PLL. The area is 960 μm × 810 μm including testing pad. The PLL is fabricated in a 65nm Si CMOS process and measured with a 0.54 V supply voltage for divider and 0.5 V for other components at the output frequency of 5.49 GHz. The VCO, divider chain including the ILFD, and digital calibration circuit consumes 551 μW, 346 μW, and 32 μW respectively. The other PLL components including an input reference buffer consume 21 μW. As a result, the total power consumption was 950 μW. As a reference signal, 34.3-MHz sine wave (f_{ref}), generated by an Agilent Technologies E8257D signal generator, was input during the measurement.

Fig. 6 (b) shows a frequency spectrum of the PLL output at f_{out} = 5.49 GHz, measured by an Agilent Technologies E4448A spectrum analyzer. In this case, the reference spurious level of -65 and -70 dBc, which were 34.3 MHz away from the carrier, were observed.

PLL phase-noise characteristics at f_{out} = 5.49 GHz measured by an Agilent Technologies E5052A signal source analyzer are shown in Fig. 7. Measured in-band phase noise was about -60 dBc/Hz and out-band phase noise at a 1-MHz offset frequency was -106 dBc/Hz. Measured bandwidth of the PLL was about 100 kHz. Spurs around 500 kHz and 20 MHz were caused by measurement condition.

Performance summary of the proposed PLL and its comparison with other low-power-supply PLLs are given in Table I. The proposed PLL shows the lowest power consumption and acceptable phase noise characteristics compared with other PLLs. In addition, to make a fair power consumption and phase noise comparison among

TABLE I
PERFORMANCE SUMMARY AND COMPARISON OF LOW-POWER-SUPPLY PLLS.

Reference	CMOS technology	V_{DD} [V]	f_{out} [GHz]	f_{out}/f_{ref}	Phase noise (PN) [dBc/Hz]	Offset (Δf) [MHz]	Ref. spur. [dBc]	Power [mW]	Area [mm^2]	VCO
This work	65 nm	0.5/0.54*	5.49	160	−106	1	−65	0.95	0.78	*LC*
[1]	180 nm	0.5	1.9	128	−120	1	−44	4.5	1.3	*LC*
[3]	65 nm	0.5	5.54	160	−105	1	−65	1.6	0.64	*LC*
[12]	90 nm	0.5/0.65**	2.59	162	−113	1	−80	6.0	0.14***	*LC*
[13]	130 nm	0.5/0.8****	9.12	128.5	−105	1	−58	12	1.2	*LC*
[14]	90 nm	0.5	2.24	16	−87	1	−40	2.1	0.074***	Ring

*0.54 V: Divider, 0.5 V: Others supply, **0.5 V: Analog, 0.65 V: Digital supply, ***excluding I/O pads, ****0.5 V: Analog, 0.8 V: Digital supply.

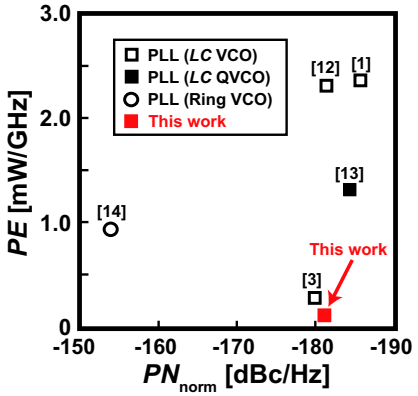

Fig. 8. Performance comparison among low-power-supply PLLs.

low-power-supply PLLs that have different output frequencies, the power efficiency (PE) and normalized phase noise ($PN_{\rm norm}$) are used in Fig. 8. These factors can be expressed as PE =(power consumption)$/f_{\rm out}$ and $PN_{\rm norm} = PN - 20\log(f_{\rm out}/\Delta f)$, respectively. As shown in Fig. 8, the proposed PLL achieves the finest PE with relatively good $PN_{\rm norm}$.

IV. CONCLUSION

We proposed the ultra-low-power PLL with an ILFD as a prescaler and a linearized varactor under low supply voltage operation. The FBB is applied in the MOS varactor to compensate the linearity under low voltage operation, which can achieve the stability of PLL operation. To adjust the control voltage of ILFD automatically, the digital calibration circuit is applied.

The concept was verified with a fabricated chip in a 65 nm Si CMOS process. The proposed PLL shows the great power efficiency with acceptable phase noise characteristics under low supply voltage, at the output frequency of 5.49 GHz.

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