A Highly Selective LNTA Capable of Large-Signal Handling for RF Receiver Front-Ends

M. Mehrpoo and R. Bogdan Staszewski
Delft University of Technology, Delft, The Netherlands

***Abstract* — To achieve ultimately flexible multi-core radio operation, wide-band receiver RF front-ends must be robust against interference well in excess of the requirements usually specified by a radio standard. In this paper, a highly selective, very linear low-noise transconductance amplifier (LNTA) capable of large-signal handling for current-mode receiver (RX) front-ends is proposed and implemented in 65-nm CMOS. It is shown that by combining on-chip high-Q bandpass filters with a push/pull class-AB common-gate stage, a measured 1-dB desensitization point (B_{1dB}) and large-signal $IIP3$ of +8 dBm and +20 dBm, respectively, can be achieved. In addition, by applying a noise cancellation technique, via an auxiliary push/pull class-AB common-source stage, the proposed LNTA measures a moderate NF of 5.9 dB, which is a very competitive number for such high value of B_{1dB}. The circuit consumes 7.5 mA at 1.5 V.**

I. Introduction

The staggering advances in wireless technologies have led to the abundance of wireless/cellular standards over the past few years. Most of the emerging radio standards require flexible RF transceivers capable of handling various frequency bands, channel bandwidths and modulation schemes. Meanwhile, the demand by manufacturers for miniaturization, power and cost reduction have compelled further integration of RF transceivers by juxtaposing multiple RF SoC cores on a single silicon die.

The prominent challenge in multi-radio chips is a blocker interference. Blocking conditions, esp. in cellular radios, are very stringent, requiring high performance external SAW filters or duplexers. However, SAW filters are bulky and expensive; they reduce the RX flexibility and degrade its sensitivity by a few dB. To circumvent these issues, SAW-less receivers (by removing the SAW filter at the input of the RX) have been proposed in the literature.

SAW-less receivers proposed in [1] and [2] attempt to conform to the blocking profile requirements as specified by 3GPP or other similar standardizations. As an example, a GSM receiver should withstand a 0-dBm continuous-wave (CW) blocker at 20 MHz away from 850/900 MHz bands and at 80 MHz away from PCS/DCS bands. Due to the assumption that the blocking conditions are rare, a blocker NF of up to +15 dB is acceptable. While the SAW-less operation of a receiver is already a challenging task, multi-core radio integration further adds to its complexity. In multi-core radios, due to the proximity of antennas, the power of the interferer appearing at the input of the RX can be considerably larger than the values specified by the radio standards blocking profiles. As an example, Wi-Fi transmitter (TX) leakage power into a WCDMA Band-I SAW-less RX front-end can be as large as +5 dBm at a frequency offset of less than 240 MHz, assuming 15 dB antenna-to-antenna isolation and a maximum TX power of +20 dBm. This stresses the necessity of wide-band RX front-ends capable of handling large signals in order to achieve the ultimately flexible (i.e., multi-band/multi-mode) and multi-core radio operation.

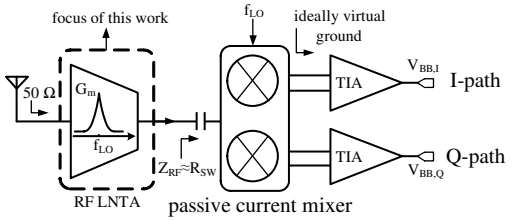

Fig. 1. Current-mode RX topology used as the context for the design of the proposed LNTA.

It has been demonstrated in several publications ([1], [2] and [3]) that current-mode RX architectures, as shown in Fig. 1, usually have superior performance in tolerating large blockers. Although, in this configuration, due to the small LNTA output load impedance, the linearity bottlenecks at the output of the LNTA are relaxed [1], the LNTA input (or any intermediate node) needs to tolerate large blockers as well. In this paper, a highly selective LNTA with a large-signal handling capability is proposed in the context of the current-mode RX architectures.

II. Improving B_{1dB} and NF of Push/Pull Class-AB CG LNTA using HQ-BPFs

A core block of the LNTA proposed here is a push/pull common-gate (CG) amplifier, which is inspired from [4], with its bias tuned for class-AB operation under large signal conditions. The class-AB operation is beneficial since it relaxes the constraining universal trade-off between the power consumption and large dynamic range (or linearity) that exists for typical class-A amplifiers [1], [4]. Because of the class-AB push/pull operation, a large B_{1dB} of +22 dBm has been reported in [4] for the CG LNTA (assuming a 0-Ω load impedance), demonstrating its potential for large-signal operation. However, due to the small g_m of a single CG LNTA (≈20 mS), the overall noise of the RX is dominated by the passive current mixer and the transimpedance amplifier (TIA) following it.

The proposed solution to improve the noise performance of the push/pull CG LNTA is by the g_m-enhancement tech-

nique shown in Fig. 2. It can be shown that the effective g_m of the LNTA increases by a factor of $\approx g_{m,stg2} \cdot Z_L$, where $g_{m,stg2}$ and Z_L are the g_m of the second stage (consisting of M_5 and M_6) and the load impedance of the CG amplifier, respectively. The design formula for the NF of the LNTA is roughly given by Eq. 1, where γ_{stgn} is a fitting parameter of the noise model and R_s is a source impedance and typically equal to 50 Ω. According to this equation, provided that $|Z_L| \gg 8R_s$, the noise contribution from Z_L and the second stage, hence the overall NF, can be minimized. In addition, by increasing Z_L, $g_{m,LNTA}$ increases and the noise contribution of the stages following the LNTA can be suppressed [1].

$$NF \approx 10log_{10}\left(1+\gamma_{stg1}+\frac{8R_s}{|Z_L|^2}\left(real\left\{Z_L\right\}+\gamma_{stg2}\right)\right). \quad (1)$$

However, the successful large-signal operation of the push/pull CG topology of Fig. 2 depends on the value of Z_L, which should ideally be zero to avoid any voltage swing on the drain of M_3 and M_4. The effect of Z_L on the large-signal performance and the compression point of the CG stage is investigated in Fig. 2(right) by plotting the large-signal G_m of the CG stage defined by

$$G_m = \frac{I_{D,n}[1] + I_{D,p}[1]}{V_{in}}, \quad (2)$$

where, V_{in} is the input CW sinusoid amplitude and $I_{D,n}[1]$ and $I_{D,p}[1]$ are the first-harmonic Fourier coefficients of the drain currents. As $|Z_L|$ increases, the gain starts to compress and for Z_L >35 Ω, the gain expansion, thus the class-AB behavior, completely disappears. Nevertheless, according to Eq. 1, to minimize the NF, Z_L >400 Ω is required. To circumvent this apparent trade-off between the noise and large-signal performance, Z_L is proposed to be a high-Q bandpass impedance to provide large in-band (IB) impedance ($Z_{L,IB}$) for the desired signal and low out-of-band (OB) impedance ($Z_{L,OB}$) for large input blockers. By using the impedance transformation property of a passive mixer, such an on-chip high-Q bandpass filter (HQ-BPF)

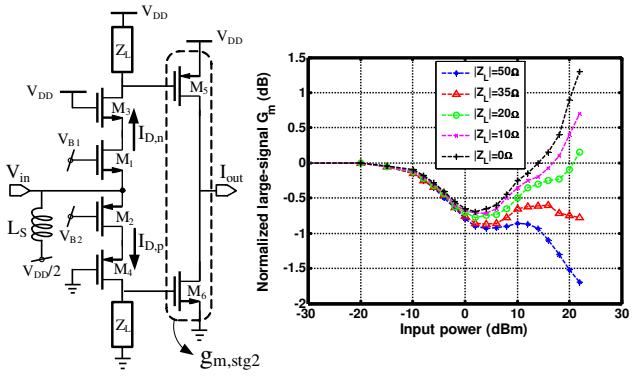

Fig. 2. (left) Enhancement of the push/pull CG LNTA (right) CG stage large-signal performance simulations with 1.4 mA current and 50-Ω input matching. The drain DC voltage of M_3 and M_4 is kept constant and equal to 1.5 V and GND, respectively.

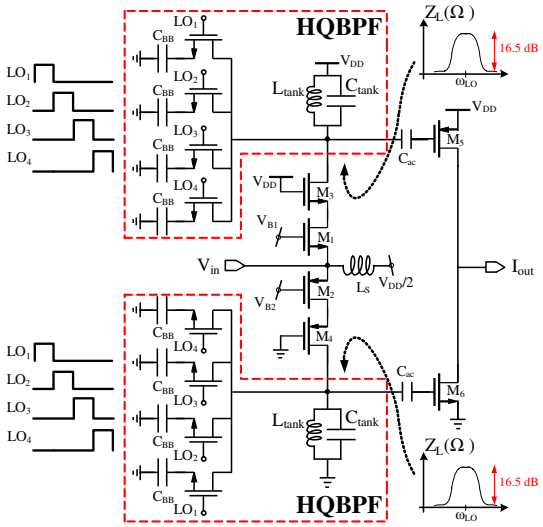

Fig. 3. Schematic of the proposed LNTA using HQ-BPFs to improve noise and large-signal performance of the CG LNTA.

can be realized [2]. The LNTA proposed in Fig. 3 benefits from the large-signal handling capability of a push/pull CG stage, while improving its noise performance.

Through the analysis presented in [6], $Z_{L,OB} \approx R_{SW}$, where R_{SW} is the switch resistance. Similarly, it can be shown that $Z_{L,IB} \approx \beta R_{tot} + R_{SW}$, where R_{tot} is the total resistance at the drain of M_3 and M_4 (excluding the HQ-BPFs) and $\beta = \gamma/(1+\gamma)$. γ can be calculated through

$$\gamma = \left(\sum_{k\neq 0}^{\pm\infty} \frac{1}{(4k+1)^2\left[\frac{j(4k+1)/Q}{1+j\frac{4k+1}{Q}-(4k+1)^2}+\frac{R_{SW}}{R_{tot}}\right]}\right)^{-1}, \quad (3)$$

where, Q is the Q-factor of the LC-tank. For a purely resistive load ($Q \ll 1$), $\beta \approx 8/\pi^2$, which is in accordance with [6]. As another example, β reduces to 0.24 for Q=10, R_{SW}=30 Ω, and R_{tot}=500 Ω. Counter-intuitively, it is concluded that a lower Q is desirable to maximize $Z_{L,IB}$.

III. NF Improvement Using CG/CS NC Technique

The NF of the proposed LNTA can be further improved by incorporating an auxiliary g_m path ($g_{m,aux}$) for noise cancellation (NC) ([3] and [5]) and g_m-enhancement, as shown in Fig. 4. The contribution of M_1 and M_2 drain current noise to the LNTA noise factor (F) is equal to

$$F = \left(\frac{g_{m,aux} - \sqrt{\frac{\pi^2}{8}}\frac{\beta R_{tot}\cdot g_{m,stg2}}{R_{in}}}{g_{m,aux} + \frac{Z_{L,IB}\cdot g_{m,stg2}}{R_{in}}}\right)^2 \gamma_{stg1} + ..., \quad (4)$$

where, R_{in} is the LNTA input impedance determined by the CG stage. It is seen that, by the proper choice of $g_{m,aux}$, NC can be achieved. Contrary to [3], by implementing all the stages using complementary NMOS/PMOS transistors, improved small-signal linearity (IIP2 and IIP3) as well as large-signal linearity (B_{1dB}) can be achieved. In addition, $g_{m,aux}$ bias is also tuned for class-AB operation under the large-signal condition.

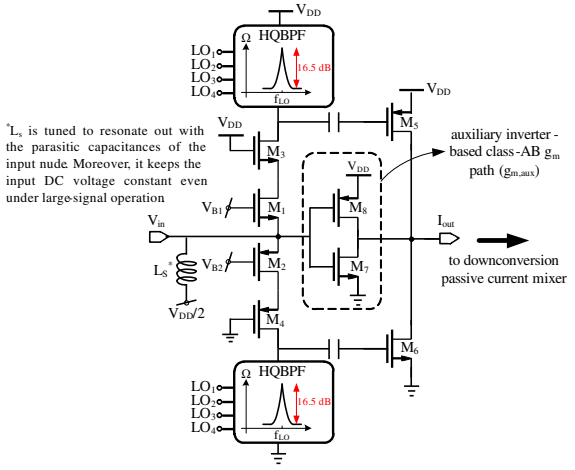

Fig. 4. Schematic of the proposed LNTA with $g_{m,aux}$ for NC.

IV. Measurement Results

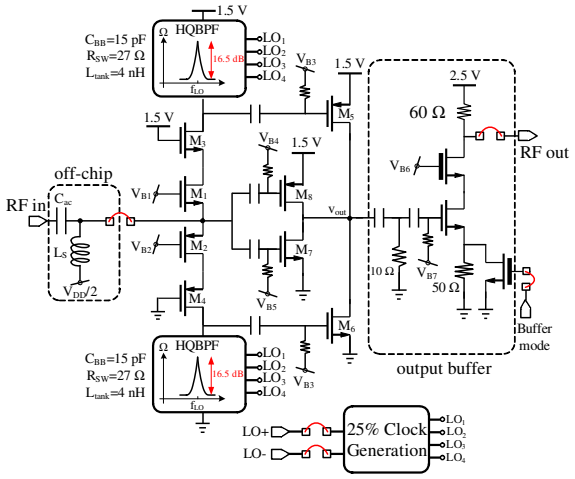

Fig. 5. Simplified schematic of the implemented LNTA.

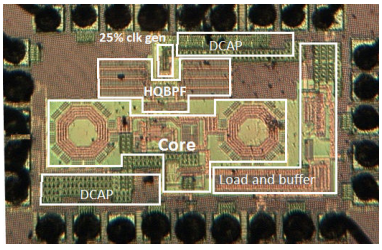

Fig. 6. Die microphotograph.

To verify the ideas and analysis presented above, the proposed LNTA was implemented in 65 nm CMOS with low-V_t devices and a supply voltage of 1.5 V. As shown in Fig. 5, the test chip also includes the 25% duty-cycle clock generation circuitry, the LNTA termination load, which emulates the input impedance of passive current mixer that follows the LNTA[1], and an output buffer. The die microphotograph of the implemented LNTA system is shown in Fig. 6. To generate the 25% duty-cycle clocks, an on-chip $\div 2$ divider, driven by $2\times f_{LO}$, provides quadrature 50% duty-cycle clocks at the desired f_{LO}. By using 4 NAND gates, the 50% duty-cycle clocks are then used to generate the 25% quadrature clocks [2].

The measured S_{11} in Fig. 7a shows a good 50-Ω impedance matching for the frequencies between 0.8 to 2.2 GHz. To show the bandpass characteristic of the LNTA gain, the normalized S_{21} is plotted in Fig. 7b for different clock frequencies. After de-embedding the effect of the output buffer and the LNTA load impedance, g_m of the LNTA is plotted in Fig. 8a. The frequency response of the LNTA when the HQ-BPFs are disabled is determined via the LC-tank, which has a resonance frequency (ω_{tank}) of around 1.8 GHz. When HQ-BPFs are enabled, the 3-dB RF bandwidth is equal to 40 MHz and the LNTA maintains 6 dB OB rejection for the frequencies between 1.5—2 GHz. It can be seen that the maximum in-band gain and symmetry around ω_{LO} is achieved when $\omega_{tank} = \omega_{LO}$.

For the noise measurements, the LNTA was tuned to 1.8 GHz. The measurement result shows an overall in-band NF of 6.5 dB, when the HQ-BPFs are enabled. With no blocker, HQ-BPFs can be disabled to reduce NF by 0.5 dB. However, the NF increase penalty when the HQ-BPFs are enabled is much lower compared to [2], in which the NF degrades by 5 dB (NF is equal to 3.1 dB and 8 dB by disabling and enabling the HQ-BPFs, respectively). In addition, when the HQ-BPFs are disabled, 2.9 dB higher in-band g_m can be achieved, which helps to further mitigate the noise of the stages following it.

The resilience of the LNTA against blockers is measured using the blocker compression, plotted in Fig. 8b. The LNTA is tuned to 1.8 GHz, the CW wanted signal is located in-band and the CW blocker is located at 100 MHz offset frequency. The input blocker power is swept and the change in the small-signal g_m of the LNTA is measured. B_{1dB} of about +8 dBm is acheived. It should be emphasized that the implemented LNTA comprises a single-ended topology. B_{1dB} can be improved by 3 dB by using a differential topology, but at the cost of higher area/power.

[1]To maintain the current-mode operation of the LNTA, its load impedance should be made as small as possible. In this paper, a 10 Ω resistor is chosen to emulate the impedance of the mixer following it.

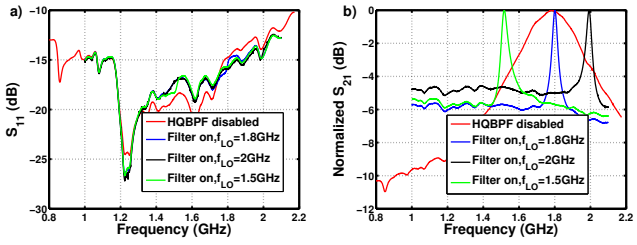

Fig. 7. Measured S-parameters: (a) S_{11}; (b) normalized S_{21}.

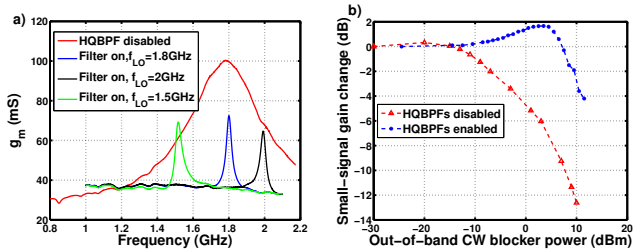

Fig. 8. Measured (a) LNTA g_m; (b) small-signal g_m change for a CW blocker at 100 MHz offset.

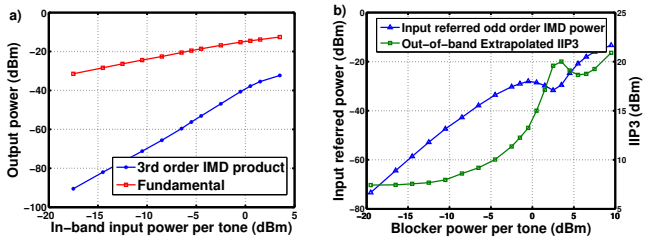

Fig. 9. Measured (a) in-band P_{out} vs. P_{in} fundamental and IMD curves; (b) OB input-referred IMD power and extrapolated IIP3.

Compared to the differential topology in [2], the proposed single-ended LNTA has a 7 dB better B_{1dB}, while its NF is improved by 1.5 dB. Ref. [4] has reported B_{1dB} of +12.4 dBm for a differential push/pull class-AB CG LNTA with actual loading conditions, but the NF is 10.7 dB—this is to be contrasted with the significantly improved NF here while having a comparable large-signal performance. In addition, due to the 6 dB OB filtering prior to the mixer in our scheme, the RX is less sensitive to the blocker reciprocal mixing with the RX LO phase noise. Otherwise, the large blockers at the LNTA input will drive the mixer and the following stages into the compression.

Due to the class-AB operation of the LNTA, a relatively large gain expansion followed by compression in Fig. 8b (blue curve) can be seen. Although the gain expansion exceeds the +1 dB point, it can be expected that this gain expansion will be compensated with the gain compression of the mixer following the LNTA. To demonstrate the effectiveness of the HQ-BPFs in achieving the improved large-signal performance, the measurement results with the HQ-BPFs disabled are also shown in Fig. 8b (red curve). In this case, it is seen that B_{1dB} reduces to -10 dBm.

The measured P_{out} vs. P_{in} fundamental and IMD curves for two in-band CW signals are plotted in Fig. 9a. The in-band IIP3 is around +13 dBm at the tuned center frequency of 1.8 GHz. This relatively large value of IIP3 was expected due to the complementary structure of the LNTA. The out-of-band IIP3 of the LNTA is also measured by applying two CW blockers with equal powers at 1900 MHz and 1999 MHz frequencies. The LNTA is tuned to 1.8 GHz and the in-band IMD product at 1801 MHz is referred to the input using small-signal in-band gain and used to extrapolate out-of-band IIP3 (Fig. 9b). The notch in the IMD curve occuring around +2 dBm blocker power corresponds to the large-signal IMD "sweet spot" of the LNTA. The quiescent current of the LNTA is 7.5 mA, which increases to 21.9 mA at the presence of +8 dBm blocker. The measured performance of the proposed LNTA is summarized in Table I.

TABLE I
COMPARISON WITH STATE-OF-THE-ART.

Parameter	This work	[4]	[2]	[5]
System	Meas. LNTA	Sim. LNTA	Meas. RX	Meas. LNTA
RF input	single-ended	diff.	diff.	diff.
CMOS(nm)	65	90	65	45
$g_m(mS)$	75/100[1]	20	N/A	36.5
NF (dB)	6.5/5.9[1]	1.8/10.7[2]	8/3.1[1]	4.5
Blocker NF[4](dB)	8.5[5]	N/A	11.4	N/A
IB-IIP3 (dBm)	+13	N/A	-12.4	+10
OB-IIP3 (dBm)	+20	+32.8	N/A	≈+10
B_{1dB} (dBm)	+8	+12.4[2]	+1	-3
Supply (V)	1.5	1.5	1.3	2.2
Current (mA)	7.5[3]	5.4	N/A	16

[1]HQ-BPFs disabled, [2]complete RX, [3]core circuitry, [4]for 0 dBm blocker power, [5]predicted from simulations

V. Conclusion

In this paper, a very linear LNTA capable of large-signal handling for current-mode RX front-ends is proposed and implemented in 65-nm CMOS. It is shown that by combining the on-chip HQ-BPFs with a push/pull CG stage and applying the NC technique using an auxiliary class-AB inverter-based g_m-path, a large 1-dB desensitization point, out-of-band IIP3, and in-band IIP3 of +8 dBm, +20 dBm, and +13 dBm, respectively, with a moderate NF of 5.9 dB can be achieved. The large in-band g_m of the LNTA (≈100 mS) can provide sufficient suppression of the noise from the stages following it.

VI. Acknowledgment

The authors would like to thank Dr. Hung Li from Mediatek for technical discussions and sponsorship.

References

[1] C.Y. Yu, et al., "A SAW-Less GSM/GPRS/EDGE Receiver Embedded in 65-nm SoC," *IEEE J. Solid-State Circuits*, vol. 46, iss. 12, pp. 3047–4060, Dec. 2011.

[2] A. Mirzaei, et al., "A 65 nm CMOS quad-band saw-less receiver SoC for GSM/GPRS/EDGE," *IEEE J. Solid-State Circuits*, vol. 46, iss. 4, pp. 950–946, April 2011.

[3] Z. Ru, et al., "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *IEEE J. Solid-State Circuits*, vol. 44, iss. 12, pp. 3359–3375, Dec. 2009.

[4] E.A. Keehr and A. Hajimiri, "A Wide-Swing LNTA and the Enabling of Large-Signal Handling Direct-Conversion Receivers," *IEEE Transactions on Circuits and Systems 1:Regular Papers*, vol. 59, iss. 1, pp. 30–43, Jan. 2012.

[5] H.M. Geddada, et al., "Fully balanced low-noise transconductance amplifiers with P_{1dB} >0dBm in 45nm CMOS," *IEEE Proc. ESSCIRC*, pp. 231–234, Sep. 2011.

[6] A. Mirzaei and H. Darabi, "Analysis of imperfections on performance of 4-phase passive-mixer-based high-Q bandpass filters in SAW-less receivers," *IEEE Trans. on Circ. Sys. I*, vol. 58, iss. 5, pp. 870–892, May 2011.