A 240 GHz Single-Chip Radar Transceiver in a SiGe Bipolar Technology with On-Chip Antennas and Ultra-Wide Tuning Range

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***Abstract* — This paper presents an ultra-wideband single-chip radar transceiver MMIC around 240 GHz in a SiGe:C bipolar laboratory technology with an f_{T} of 240 GHz and f_{max} of 380 GHz. The presented transceiver architecture consists of a fundamental 120 GHz VCO, two 240 GHz frequency doublers, a fundamental 240 GHz down-conversion mixer, a divide-by-four stage, a PLL-mixer and two on-chip patch antennas. The complete transceiver architecture is fully differential. The chip facilitates a -1 dBm peak output power (EIRP) at the transmit patch antenna and a tuning range of 61 GHz. The phase noise at 1 MHz offset is -84 dBc/Hz at 240 GHz (and better than -76 dBc/Hz over the full tuning range). The 240 GHz mixer offers a simulated noise figure below 17 dB, a simulated conversion gain of better than 5 dB, and an input refered compression point of -1.3 dBm. The results are achieved with a power consumption of 750 mW from a single 5 V supply.**

I. Introduction

An increasing number of millimeter-wave systems and circuits above 100 GHz are published of late in silicon technologies thanks to the advances in SiGe HBT and CMOS technologies. There is a number of applications for communication and radar, e.g. in commercial, defense, security, and millimeter-wave imaging, where these advanced technologies are highly suitable for. While waveguide technologies offer excellent performances in receivers based on Schottky diodes and transmitters based on Gunn diodes for these frequency ranges their implementation remains quite costly and space consuming due to their waveguide assemblies. This is where advanced silicon technologies can overcome these drawbacks especially in array implementations due to their highly integrable nature.

Although first fully integrated SiGe receivers at 245 GHz [1],[2] and transmitter chips at 220 GHz [3] have already been demonstrated, the implementation of circuits at these frequencies is still an interesting and challenging part of an MMIC, even though SiGe HBT technologies have reached cut-off frequencies of $f_{\mathrm{T}} = 300$ GHz, $f_{\mathrm{max}} = 500$ GHz [4].

The primary challenge in the design of fully integrated transceivers is to achieve an output power high enough to drive an active mixer fundamentally. Hence, up to date only subharmonic receivers in SiGe technologies have been presented. This paper presents a fully integrated fundamentally driven transceiver design around 245 GHz.

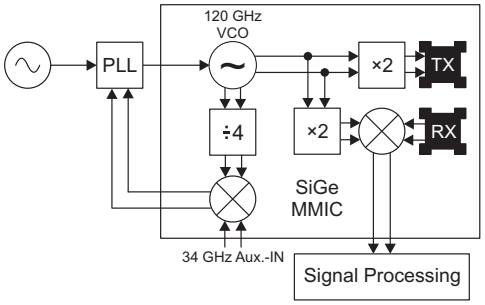

Fig. 1. Block diagramm of the transceiver chip.

II. System Concept

The block diagram of the proposed radar system is given in Fig. 1. The high frequency parts of the radar system are integrated in a SiGe MMIC. For a robust operation all on-chip circuits and interfaces are realized fully differential. The 120 GHz signal is generated by a fundamental VCO which is then feeding two frequency doublers. One doubler directly drives the differential transmit on-chip antenna while the other doubler is used to drive the LO-input of the fundamental mixer, which is directly connected to the receive antenna. For stabilization in a PLL and generation of an FMCW ramp, a divide-by-4 circuit and an offset PLL-mixer, which is driven by an auxiliary 34 GHz signal source, is also integrated on the MMIC. The 34 GHz auxiliary LO can easily be replaced by an on-chip VCO in future designs.

III. Circuit Design and Experimental Results

In addition to the full transceiver chip breakout chips of the VCO and the VCO in combination with one frequency doubler are also available. Both of these breakout chips

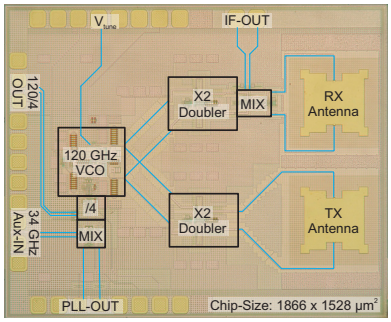

Fig. 2. Chipphotograph with an overall chip size of 2.85 mm^2.

have the divide-by-4 circuit integrated for easier characterization of the chips. The chips were fabricated in an advanced laboratory technology from Infineon [4], which offers transistor cut-off frequencies f_{T} of 240 GHz and $f_{\max}$ of 380 GHz at optimum current density. Fig. 2 shows the photograph of the chip with the highlighted building blocks. The single system voltage of the transceiver chip is 5 V.

The topology of the frequency divider and PLL-mixer have already been published in [5] at a lower operating frequency and in a production technology with lower cut-off frequencies. Here, the operation of the divider is pushed to a operation frequency of 132 GHz, which is actually limited in measurements by the maximum oscillation frequency of the 120 GHz VCO. The frequency divider consists of two cascaded regenerative divide-by-two cells. With a current consumption of 32 mA (160 mW), which probably is much higher than needed, operation over the whole frequency range is ensured. The PLL-mixer shares the same topology as one divide-by-two cell with an additional differential amplifier output stage. The PLL-mixer has a current consumption of only 10 mA (50 mW) including the output buffer.

A. *120 GHz Oscillator*

The integrated fundamental VCO is based on the 80 GHz VCO proposed in [5]. Fig. 3 shows the schematic of the fully differential wideband oscillator, which builds the core of the presented signal source. The resonant circuit, which determines the oscillation frequency is mainly formed by L_{B} and C_{var}. Here, it is tuned to a center frequency of 120 GHz and uses a single varactor at the emitter nodes of the oscillating transistor T_1. The omitted second varactor decreases the relative tuning range compared to [5], but this was necessary in reflection of the layout.

The current consumption of the VCO itself is $\approx$ 60 mA (300 mW). The current is divided into 35 mA for the core current I_0, 15 mA for the additional cascode current I_1 and

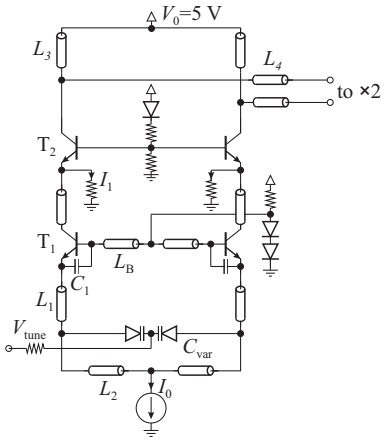

Fig. 3. Schematic of the wideband 120 GHz VCO.

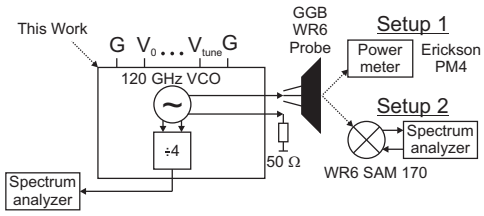

Fig. 4. Block diagram of the measurement setup.

10 mA for the biasing networks of the VCO. This results in a DC current density slightly above half the optimum current density for the cascode stage transistors with the intention of a better phase noise performance.

The breakout chip has been measured on-wafer using a 170 GHz probe (Picoprobe 170, WR6, GSG), a spectrum analyzer mixer (RPG SAM 170, WR6), a spectrum analyzer, and an Erickson PM4 power meter. The block diagram of the measurement setup is shown in Fig. 4. To determine the tuning characteristic and the phase noise, usually a mixer is used for downconversion of the oscillation frequency. Here, however, it is easier to measure the divided-by-four signal at the output of the frequency divider and to multiply its frequency by four and add 12 dB to the phase noise. The output is measured single-ended only due to the nature of the probe, while the other output of the differential output is terminated with 50 Ohm on-chip.

In Fig. 5 the measured output power as a function of the oscillation frequency is shown. A differential peak output power of 14 dBm is achieved. The losses in the waveguide on-wafer measurement setup of 4.5 dB (WR6 probe, WR6 to WR10 taper, WR10 waveguide) are de-embedded and 3 dBm are added for the differential power due to the single-ended measurement setup. The observed ripple in the measured output power is due to the poorly matched

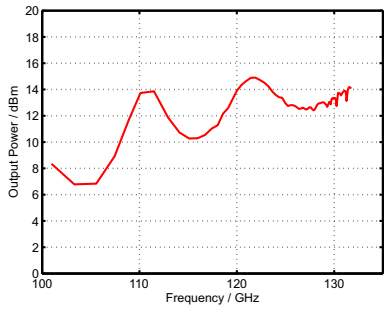

Fig. 5. Measured output power versus frequency of the VCO.

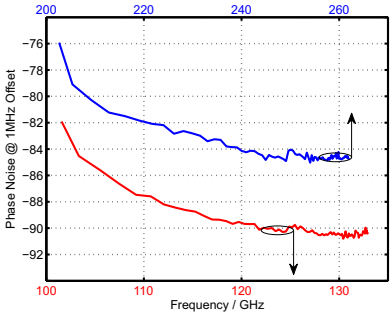

Fig. 6. Measured phase noise versus frequency of the 120 GHz VCO and the 240 GHz VCO with doubler.

probe. The periodicity of the ripple is ≈ 10.4 GHz. With a PTFE dielectric ($\varepsilon_r = 2.1$) this corresponds to a length of the disturbance of ≈ 10 mm, which fits well with the probe dimensions from the tip to the coax-waveguide transition. Neglecting the ripple due to the probe an output power flatness of ≈ 5 dB over the whole frequency range is achieved.

Fig. 6 shows the phase noise versus oscillation frequency of the VCO chip at a 1 MHz offset. Around the center frequency the phase noise is ≈ -90 dBc/Hz and over the whole frequency range it is better than ≈ -82 dBc/Hz. The tuning range of the VCO chip is about 31.37 GHz resulting in a relative tuning range of 26.1%.

B. 240 GHz Frequency Doubler

The 240 GHz VCO and doubler breakout chip is also measured on-wafer in the same manner as the VCO breakout chip (Fig. 4), but with WR3 waveguide components instead of WR6. The concept of the fully differential doubler is based on a Gilbert-Cell multiplier with an additional cascode output stage, which has already been published in [3]. Here, it is optimized for a slightly higher operating frequency. The breakout chip consists of the fundamental VCO which directly drives one Gilbert-Cell frequency doubler and the divide-by-4 stage.

The current consumption of the doubler and the VCO is ≈86 mA (430 mW). The current is divided into 60 mA (300 mW) for the VCO and 26 mA (130 mW) for the doubler. At this point it has to be noted that due to the nature of the frequency doubler topology this is a dynamic current which is proportional to the input power delivered to the doubler. This input power is at least 3 dB higher in this breakout chip than in the transceiver chip with the VCO feeding two of these doublers.

In addition to the phase noise versus frequency of the VCO in Fig. 6, the phase noise of the 240 GHz doubler chip is also shown. The phase noise is better than -76 dBc/Hz at a 1 MHz offset over the whole frequency range and around the center frequency it is ≈ -84 dBc/Hz. These results show that the doubler has nearly no impact on the phase noise performance of the VCO due to the isolation of the cascode stage of the VCO. This is due to the fact that these results are close to the theoretical increase in phase noise of 6 dB from the frequency translation from 120 GHz to 240 GHz. The only observable impact is the loss in relative tuning range at the upper end of the tuning range with still 24.7% of tuning range (59.37 GHz). This results in a loss of about 1.4% in tuning range probably due to local heating in the cascode stage from additional power consumption of the doubler in close vicinity to the VCO. It could also stem from the changed load impedance on the VCO.

The main disadvantage of this doubler type is the low suppression of the fundamental harmonic of the VCO which is shown in Fig. 7. The VCO feed through is measured with the SAM 170, which is usable between 110-170 GHz, and the WR6 probe while the doubler output power is measured with a SAM 325 and a WR3 probe, which are only characterized from 220-325 GHz. This is done instead of power meter measurements, due to the nature of the power meter which would detect the power from all harmonics instead of the interesting harmonic. In the worst case the suppression of the fundamental is only ≈ 6 dB at the upper end of the tuning range, but the output power of the doubler is still higher than the VCO feed through which is needed to drive the 240 GHz mixer fundamentally.

The output power for the transceiver can not be taken from Fig. 7 as the VCO is driving two doublers and they are not connected to a lossy pad compensation network in the transceiver case. In addition to that the doublers are not in close proximity to the VCO and are each only exhibiting a current consumption of 20 mA (100 mW) due to the lower input power into each one.

C. 240 GHz Gilbert-Cell Mixer

The 240 GHz down-conversion mixer is based on a Gilbert-Cell and is driven fundamentally with an LO-signal at 240 GHz from one of the two doublers. The main

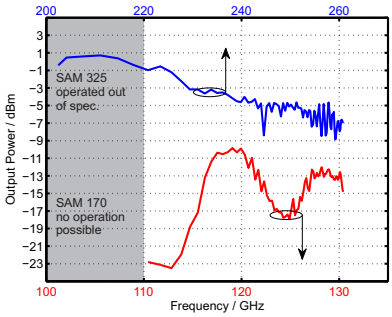

Fig. 7. Measured output power of the frequency doubler and measured fundamental power of the 240 GHz doubler chip.

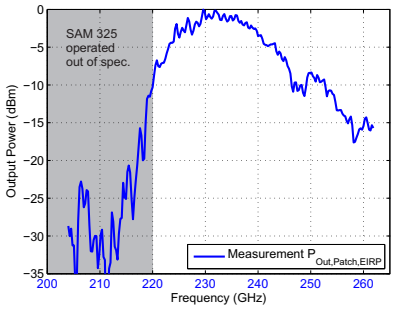

Fig. 8. Measured equivalent isotropically radiated power (EIRP) versus frequency at the transmit patch antenna.

difference to the typical Gilbert-Cell mixer is a miller compensation line between the RF-input stage and the LO-switching quad, which has shown a great influence on the noise figure and conversion gain of the Gilbert-Cell in simulations.

The noise figure and conversion gain are only simulated due to the nature of the free space environment, the lack of a mixer breakout chip, and non-existent signal source equipment around 240 GHz. The noise figure is below 17 dB between 205-265 GHz and the conversion gain is better than 5 dB over the whole frequency range. The current consumption of the complete mixer with biasing networks is 14 mA (70 mW) and has a simulated compression point of about -1.3 dBm at 240 GHz, which is sufficiently high enough to keep the mixer from being saturated by a direct coupling over the antennas.

D. 240 GHz Differential Patch Antennas

The transmit and receive signals of the transceiver are radiated over differentially fed planar patch antennas integrated on the transceiver chip hence building a quasi-bistatic case. This relaxes the requirements on the linearity of the 240 GHz receive mixer due to a minimized maximal reflection at the poorly matched antennas. These antennas have been optimized for bandwidth. But its design is quite limited due to the very small distance from the patch to the ground plane given by the used SiGe technology. A simulated gain of the antenna of only 2 dB is achieved due to the high losses of about 5 dB. The antennas have a size of about 326x326 $\mu\mathrm{m}^2$ and can clearly be seen on the right side in Fig. 2.

In Fig. 8 the output power (EIRP) at the patch antenna of the transceiver chip is shown. It was measured in a free space environment with a WR3 25 dBi standard gain horn antenna placed 5 cm above the chip and corrected to EIRP by adding 29 dB to compensate the free space loss and the gain of the horn antenna. Taken the 2 dB gain of the antenna into account this results in an output power delivered by the doubler of $\approx$ -3 dBm at 230 GHz. This measurement was taken with a prototype radar system fully stabilized over a bandwith of 61 GHz based on this transceiver chip which is presentend in [6].

IV. Conclusion

This paper presents, to the authors best knowledge, the first fully integrated radar transceiver chip around 245 GHz in a SiGe technology as well as the first reported fundamentally driven down-conversion mixer at these millimeter-wave frequencies. Although the transceiver chip exhibits some problems with the fundamental suppression it achieves a tuning range of 61 GHz and a peak transmit power (EIRP) of -1 dBm in a real radar system scenario [6] with a current consumption of 156 mA (780 mW) and shows the potential for silicon technologies at the end of the millimeter-wave range.

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