A 2.4-GHz Low Power High Performance Frequency Synthesizer Based on Current-Reuse VCO and Symmetric Charge Pump

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Abstract — **This paper presents a low power high performance frequency synthesizer. Based on the current-reuse VCO architecture, the whole system power consumption is significantly saved with excellent phase noise performance. Imbalance amplitude problems caused by the unsymmetrical VCO are solved by the pre-tuning mechanism, which automatically chooses the correct frequency band for the certain frequency channel. Besides, the symmetric charge pump (CP) can minimize the current mismatches and phase offset. The frequency synthesizer is fully integrated in 130-nm CMOS technology consuming 5.8 mW. Measurement results show performance of -130 dBc/Hz at 1 MHz offset phase noise, 450 fs rms jitter. The reference spur is below -75 dB, and it operates successfully with 1 Mbps GFSK signals as the two-point modulated transmitter.**

I. Introduction

In a transceiver chain, the frequency synthesizer plays a crucial role of driving the complex mixer to down-convert the received RF signals into the baseband or up-convert the transmitted baseband signal to the desired RF band. VCO is an essential building block in the frequency synthesizer, which is operated at the highest frequency in the whole system and attributes large portion of the total power consumption. Low power designs for VCOs have drawn intensive researches recently. Current-reuse techniques for VCO have been proposed and improved in [1]–[3]. It reuses the current from one negative conductance branch and steers it to the other branch to save half the current. However, this technology for frequency synthesizer has not been published yet. Due to its vulnerable unsymmetrical structure, the resonating frequency deviation is very high due to the parasitic capacitance and process voltage and temperature variations. Secondly, the current-reuse VCO amplitude is imbalanced due to the transconductance mismatches, which would lead to a current leakage when differential topology is implemented. Besides, imbalanced amplitude mismatches can greatly degrade the phase noise performance for the frequency synthesizer [4].

In this paper, a low power frequency synthesizer based on current-reuse VCO with excellent phase noise and reference spur attenuation performance is presented. All the high frequency components are implemented in a single-ended topology to avoid the amplitude mismatch problem and to save power. A pre-tuning system can setup the appropriate frequency band for digital alignment as initial calibration. This alignment is stored externally as preset value for future applications. The proposed charge pump makes use of symmetric load of the control signals, leading to perfect compensation for each switch, and further attenuating the reference spurs in PLLs.

The content of this paper is organized as follows: Section II introduces the fundamentals of the current-reuse VCO. Section III describes the modified design for frequency synthesizer applications, symmetric charge pump design, and the proposed frequency synthesizer architecture with fast self-calibration system. Section IV shows the experimental results and comparison with prior arts. A conclusion is drawn at last.

II. Fundamentals of Current-reuse VCO

Fig. 1 shows the simplified schematics of a conventional VCO and a current-reuse VCO. In the conventional VCO, the cross coupled pairs of NMOS transistors provide the negative conductance. In the current-reuse VCO, one of the NMOS transistors is replaced by a PMOS transistor. Hence, both NMOS and PMOS transistors are stacked in series and the supply current flows from the PMOS to the NMOS. With the current-reuse topology, the coupled negative conductance is generated in one branch. Thus, the current consumption can be reduced by half compared to the conventional LC-VCO while providing the same negative conductance [1].

During the current-reuse VCO operation, both transistors are both turned on in the first half period, steering the current to flow from supply to ground through the inductor L; In the second half period, the transistors are both turned off, so the current flows in the opposite direction through the capacitors C. The PMOS and NMOS are switched simultaneously, while the cross coupled NMOS transistors in the conventional LC-VCO are switched alternately. Therefore, the current-reuse VCO has inherently immunity

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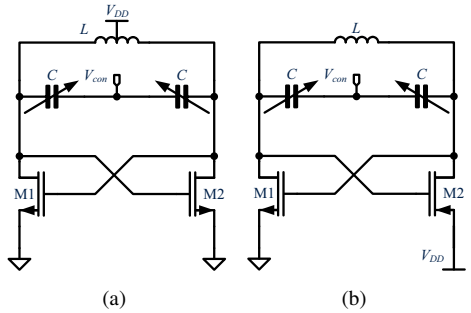

Fig. 1. (a). Conventional LC-VCO; (b). Current-reuse LC-VCO.

to the phase noise degradation caused by the second harmonic terms at the common source node.

The main drawback of the current-reuse VCO is the amplitude imbalances. In the first half period of the oscillation, both transistors are operated in triode region so that the VCO output voltage swing is limited to the supply voltage. In the second half period, both transistors are turned off, and the voltage caused by current flowing through the capacitor can be larger than the supply voltage, which leads to waveform distortion. Inserting resistors between the supply nodes to the transistor source nodes can help to balance the amplitudes. They control the DC current as well as limit the dynamic current. However, the VCO resonating amplitude is still very sensitive since it fully depends on the resistor mismatches. Moreover, the g_m mismatches of PMOS and NMOS can not be perfectly compensated. [3] uses transistors in the triode mode as the adjustable resistors to match the NMOS and PMOS transconductance. However, with all these efforts, the amplitude imbalance problem is inevitable as long as the VCO losses its symmetry.

III. Circuit Implementation

A. Proposed Current-reuse VCO

In the frequency synthesizer design, the VCO output is connected to the feedback loop, at the same time it is also connected to the mixer as the LO signal generator. Differential topology is commonly used to achieve better phase noise. The proposed VCO schematic for the frequency synthesizer is shown in Fig. 2. The left node is connected to the feedback loop while the right node is connected to the mixer as LO generator. This connection approach sacrifices the phase noise performance to obtain low power and to avoid mismatches. M1, M2, Rs_1 and Rs_2 are selected to ensure the differential oscillation waveform to be as symmetric as possible by making $g_{m1}Rs_1 = g_{m2}Rs_2$. Besides, they can limit the VCO current. Although the oscillator voltage swing is reduced by $250\,\text{mV}$, two inverter buffers can provide rail-to-rail signals for each note. Hence, the two outputs share a common oscillating frequency but not differential, since the phase delay in between is unknown. Separate applications for these two outputs connecting will not be harmful.

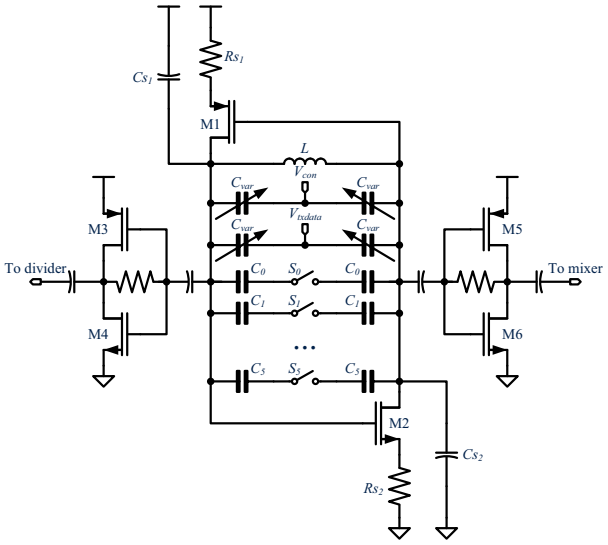

Fig. 2. Proposed current-reuse VCO for frequency synthesizer.

To compensate the high oscillating frequency deviation, the varactor consists of an array of binary weighted PMOS varactor blocks. As shown in Fig. 2, 6-bit coarse tuning inputs are implemented. Three MSB bits are used as the pre-tuning. As long as the initial oscillation frequency is finalized, these bits alignment is stored externally for the further applications. The other three bits can ensure the flexible choice of the output frequency for frequency hopping. Besides, one analog tuning capacitor is controlled by the loop filter voltage, the other one is directly controlled by the transmitted data in TX mode.

B. Proposed Symmetric Charge Pump

In a conventional charge pump, the ripples often occur during the deadzone eliminating period, due to mismatches between the falling time and the rising time of the transistors, even if the area of charge and discharge current of each phase comparison cycle are equalized. This dynamic phase offset is inevitable, as long as the control switches are asymmetric, leading to the reference spurs.

Fig. 3 shows a solution to perfectly compensate rising and falling time differences between the control signals. The loads for U, U_b, D, D_b signals are exactly the same: one PMOS and one NMOS. No switching speed difference will happen as long as these four control signals are synchronized before flowing into the charge pump. The feedback amplifier stabilizes the voltage at the output and its load. The dummy capacitor is connected to V_{outd} to

make the capacitance equalized to the node connected to the loop filter. A rail-to-rail OPAMP is implemented in this design, so that even when the output voltage of the charge pump is close to supply or ground level, the voltages of the two nodes in charge pump can also be pushed or pulled to the same level, making the currents of both paths identical.

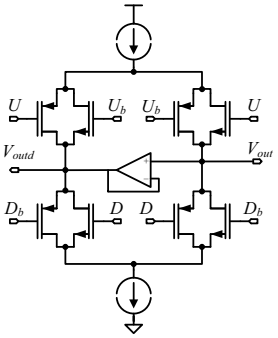

Fig. 3. Symmetric charge pump unit cell

C. System Architecture

Fig. 4 shows the frequency synthesizer architecture both in TX and RX mode. For a frequency hopping system, short settling time is required when the baseband signal is transmitted in TX mode. Two-point modulation scheme is implemented for the signal transmitting. GFSK modulation is realized at two different paths. The transmit path takes the 1-bit data and applies the low-pass Gaussian filter. After passing the digital-to-analog converter (DAC), the signal directly modulates the VCO to get ± 250 kHz frequency deviation. The other path controls the division ratio in the feedback loop by adding the modulated inputs to the $\Sigma\Delta$ modulator. Phase mismatches between the two paths are calibrated by the digital controlled time delay cell. The core building block is a $\Sigma\Delta$ fractional-N synthesizer. It can also be configured as the LO signal generator in RX mode.

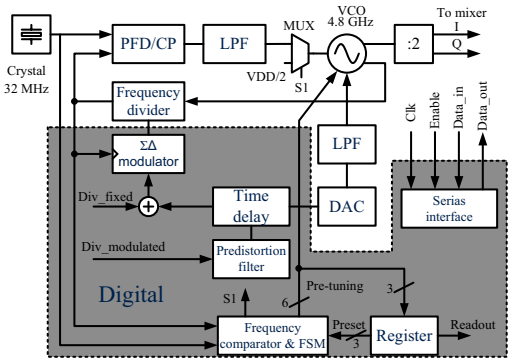

Fig. 4. Architecture of the proposed frequency synthesizer.

The digital frequency comparator uses the one input frequency reference to count the other input in a long cycle and calculates the frequency difference. For example, if the feedback frequency is estimated much higher than the reference frequency, the tuning word is incremented by a large step, lowering the frequency band of the VCO to a far away bank; If the feedback frequency is slightly higher than the reference frequency, the tuning word is incremented by one bit, lowering the frequency band to the next bank. The correct frequency band is finalized when the frequency comparator cannot detect the frequency difference in one cycle. Initially S1 is switched to zero, the PLL loop is open and half of the supply voltage is selected to control the VCO. The pre-tuning system automatically finds the suitable alignment by comparing the feedback frequency with the reference frequency. When the comparator cannot detect the tiny frequency difference, the finite state machine (FSM) switches S1 to one. Then the loop filter is connected into the system while the reference voltage is separated to the VCO. The alignments from the pre-tuning bits are sent to an external memory by the serias interface. These values will be reused everytime when the frequency synthesizer is switched on as fixed preset value. Thus, large frequency deviations from the current-reuse VCO are mostly calibrated at the very beginning stage.

IV. Measurement Results

The proposed frequency synthesizer was fully integrated in 130 nm technology. The mixed-signal and RF parts were a full custom design, and the digital block was synthesized using hardware description language. The micrograph of the frequency synthesizer is shown in Fig. 5, occupying 540 µm x 310 µm area. The power consumption for the proposed frequency synthesizer is 5.8 mW with 1.2 V supply voltage in RX mode. In TX mode, the transmitter can achieve 0 dBm output power when the synthesizer consumes about 10 mW. The internal loop filter is located out of the power ring to make fully use of the chip area. All the digital circuits, including $\Sigma\Delta$ modulator, baseband signal modulator, received signal demodulator and the series interface are synthesized in a single block.

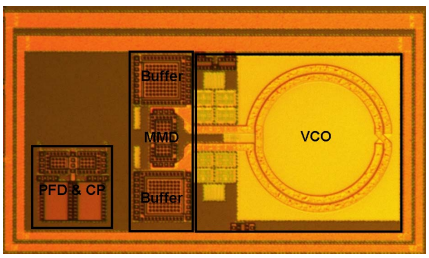

Fig. 5. Synthesizer micrograph.

The proposed frequency synthesizer provides a frequency band between 2.35 GHz and 2.55 GHz. Fig. 6 shows the measured phase noise at 2.433 GHz output. The loop filter bandwidth is set as 100 kHz to limit the $\Sigma\Delta$ quantization noise. -131 dBc/Hz at 1 MHz offset phase noise performance and 0.45 ps rms jitter are achieved.

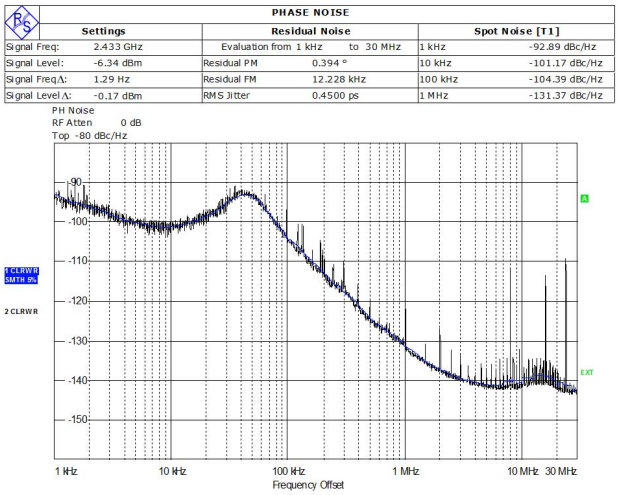

Fig. 6. Phase noise performance of the frequency synthesizer.

The reference spur level is -75 dB at 32 MHz, as shown in Fig. 7. For the two-point modulated transmitter, 1 Mbps GFSK signals with 250 kHz frequency deviation is generated at 2.433 GHz output. They are measured using signal analyzer and demodulated to observe the eye diagram. A clear eye pattern can be obtained.

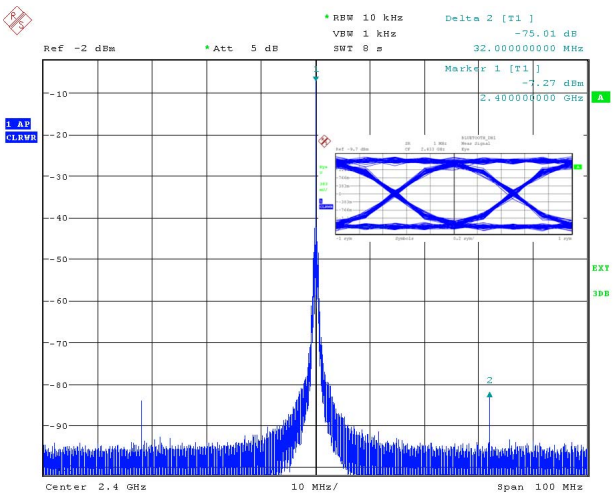

Fig. 7. Reference noise rejection performance of the frequency synthesizer.

Tab. I shows a comparison between the proposed design and other published works. The proposed approach exhibits comparable phase noise and reference spur suppression performance among other works with lower power consumption.

TABLE I
PERFORMANCE COMPARISON WITH PRIOR WORKS

Parameter	[5]	[6]	This work
Technology (nm)	180	65	130
Frequency (GHz)	2.4	2.4	2.4
Bandwidth (kHz)	460	40	100
Phase noise (dBc/Hz)	-124 @3 MHz	-120 @1 MHz	-131 @1 MHz
Ref spur (dBc)	-65	-	-75
Core area (mm^2)	4.8	0.24	0.3
Core power (mW)	38	12	5.8

V. CONCLUSION

A fractional-N frequency synthesizer based on a current-reuse VCO has been demonstrated to achieve low power low phase noise performance. Practical issues for current-reuse VCO in synthesizer applications are discussed and solved with proposed techniques. The pre-tuning system uses external memory to store the initial VCO alignment and reuses it in further implementation to calibrate against the large frequency deviation and save the settling time. The reference spurs are greatly suppressed by the proposed symmetric charge pump. Measurement results show that the proposed frequency synthesizer meets the design target and validates the design choices.

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