A 45GHz CMOS Transmitter SoC with Digitally-Assisted Power Amplifiers for 64QAM Efficiency Improvement

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***Abstract* — A 45GHz 64QAM system-on-chip (SoC) CMOS transmitter with digitally-assisted power amplifiers (DAPA) is presented. The SoC includes a 7M gate ASIC with 9b reconfigurable symbol mapping, 8X upsampling, 161tap pulse shape filtering, IQ imbalance correction and DAPA envelope/time estimation. The ASIC feeds two 10b IQ current-steering DACs and active IQ modulator. A unique transformer splitting up converter drives eight parallel combined DAPAs. The chip is packaged in aluminum housing with WR22 outputs. A 64QAM signal achieves 1.8% EVM with 33dBc ACPR at 45GHz. The data rate is 450Mbps and the integrated output power exceeds -10dBm.**

***Index Terms* — CMOS technology, Power amplifier, Quadrature amplitude modulation, System-on-a-chip.**

I. Introduction

Millimeter-wave (MMW) silicon CMOS based system-on-chip products offer affordable, highly integrated solutions for military communication and sensor payloads on both space and airborne platforms. Advanced, high speed CMOS can reliably integrate low-power digital ASIC technology with MMW front-end architectures for an ultra-compact design. CMOS SoC technology reduces the chip count and assembly costs of multi-chip modules and units that are based on high performance III-V GaAs MMIC technology to meet ever shrinking size, weight and power (SWAP) requirements. Moreover, sophisticated communication, linearization and error correction DSP algorithms can be embedded on-chip to improve performance and compensate for RF related distortion or process variation mechanisms. By implementing these algorithms on the same chip, power consumption is further reduced by eliminating power hungry digital I/O drivers and equalizers.

This paper presents the first MMW SoC transmitter design that integrates a digital 64QAM (reconfigurable) ASIC modulator including error correction with a 45GHz front-end architecture and I/Q DACs as shown in Fig. 1. This integration level is a first for MMW SoC designs. Typical MMW silicon SoC designs focused on phased array technology [1]-[2] with limited ASIC functionality, while other systems separate the baseband and RF chips due to complexity and different semiconductor technologies at the expense of SWAP [3]. But as additional digital functions, such as encryption, frequency hopping, etc., are added to military systems, it becomes desirable to integrate digital functions with the RF/MMW architecture to eliminate SWAP penalties and improve performance. This is the driving force behind this effort.

The paper also introduces a unique digitally-assisted power amplifier (DAPA) technique that reduces PA power consumption by 20%. The DAPA is a segmented amplifier with a main amplification cell in parallel with auxiliary cells (16 AUX in this design) that are dynamically switched with the envelope of a high peak-to-average power ratio (PAPR) signal to reduce overall power while maintaining linearity. This is ideal for CMOS, though we have demonstrated it using GaN [4].

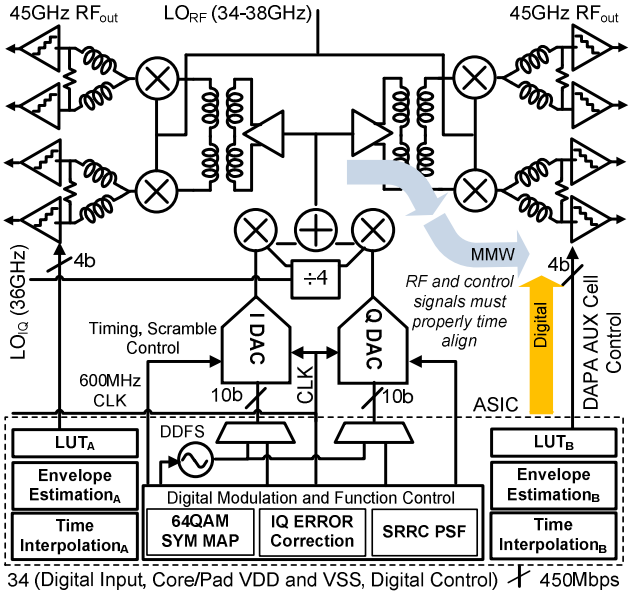

Fig. 1. Block diagram of 45GHz CMOS transmitter SoC.

II. System Architecture

The ASIC drives two 10b DACs for I/Q data and eight 4b DAPAs. A differential 600MHz clock directly feeds the DACs to maintain 1.6ps jitter for re-clocking the data which removes any data skews. The baseband signal is

directly modulated on a 9GHz RF carrier. A heterodyne architecture splits and up-converts the signal to 45GHz. The DAPAs are the final amplification stage, and the signals are combined off-chip in a novel, low-loss 4-way WR22 power combiner. System level design and optimization were performed using Agilent Ptolemy co-simulation tool with GoldenGate to simulate a 64QAM signal at the transistor level. The transmitter SoC uses the IBM 10RFe 65nm bulk CMOS process.

A. ASIC Modulator

A 9b reconfigurable symbol mapper (SYM MAP in Fig. 1) maps the incoming source bits into complex-valued, Gray-coded modulation symbols to be output at 75Msym/sec and is implemented via lookup tables (LUTs). The mapper has three user-selectable modulation modes (64QAM, 16QAM and QPSK) and a user-defined mode that accommodates up to 64 symbols via memory map for memory-less digital predistortion. The 9b resolution is sufficient to meet mapping requirements.

A 161tap SRRC (square root raised cosine) pulse shape filter was designed to meet an internal 65dBc ACPR (adjacent channel power ratio) specification. The filter was implemented as a polyphase parallel structure consisting of 7 20tap FIRs and one 21tap FIR, all operating at 75MHz. The rolloff factor is 0.3 with a 50MHz baseband bandwidth. The sample images are 8X up-sampled for easier out-of-band rejection. Fig. 2 is the measured EVM (error vector magnitude) versus data rate. The ASIC meets the 450Mbps specification.

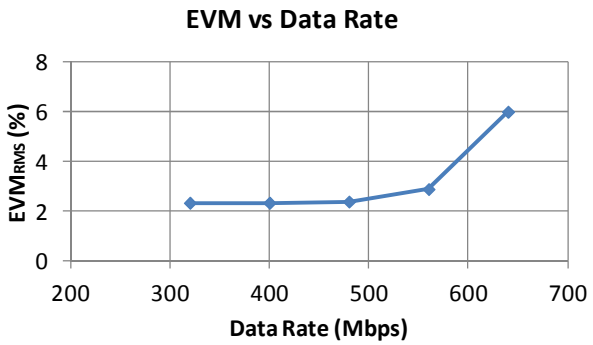

Fig. 2. Measured EVM versus data rate with 64QAM signal.

An I/Q imbalance compensation algorithm is included to reduce degradation due to analog I/Q modulator impairments. The algorithm compensates 2dB (gain), 10deg (phase), and ±2.3% full scale DAC (DC offset). These are static assumptions split even between channels.

B. DAC

Fig. 3 is a block diagram of the DAC. A five-plus-five segmentation 10b current-steering architecture was selected for this DAC. Current steering is the best candidate for high speed operation and simplicity. The segmented approach balances the advantages and disadvantages between binary and unary weighted designs. The 5b MSB is thermometer encoded for improved DNL and monotonicity, and lower glitch energy. The 5b LSB is binary weighted for compactness and simplicity. The DAC draws 20mA from a 1.2V supply. The measured SFDR exceeds 60dBc with INL/DNL less than 0.3LSB. The clock rate is 600MHz and ENOB 8.4.

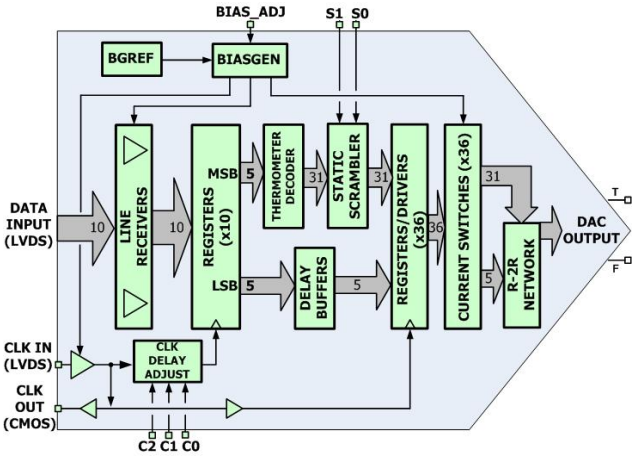

Fig. 3. 10b segmentation current-steering DAC architecture.

Included in the design are a temperature stable band-gap reference and biasgen circuit that distributes the reference voltage. The 31 thermometer coded signals are scrambled, which essentially randomizes the physical position of the unary current sources to reduce systematic mismatch error from process and temperature variation gradients. The 3b clock delay adjustment (C0, C1 and C2) for ASIC controlled data and clock alignment is required to optimize EVM.

C. MMW Front-End

The MMW front-end is a heterodyne architecture. A divide-by-4 circuit divides a 36GHz LO input to create a 9GHz quadrature signal. The divider is implemented as an injection-locked divide-by-two followed by a current-mode logic divide-by-two. The measured locking range is from 35.1GHz to 44GHz (>20%) and draws 28mA. The locking range is controlled by a 4b switched capacitor structure. A final buffer amplifier drives the modulator. The I/Q modulator is an active Gilbert cell based transformer loaded circuit that measures -7dB conversion loss with a P1dB=-2dBm.

A novel combined up-converter and output splitting transformer up-converts from 9GHz to 45GHz and splits the signal. This is shown in Fig. 4. The output transformer

folds the inter-stage match, biasing and power splitter together thus avoiding the insertion loss of an additional passive component. This is a very compact design due to no quarter-wave structures. The amplifier core is a stacked design. The feedback resistor (R12), and bypass capacitor (C1) allows the source voltage of transistor M12 to swing in phase with the drain voltage (node A), thereby avoiding clipping of large signal voltages and improving P1dB and linearity. The dual output up-converter achieves 6.5dB gain and 1.9dBm OP1dB per RF channel with an LO drive of 8dBm. The up-converter consumes 230mW.

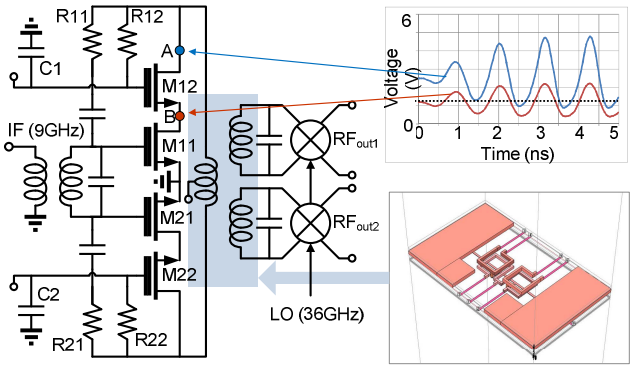

Fig. 4. Dual output, transformer-splitting up converter schematic

III. DIGITALLY-ASSISTED POWER AMPLIFIER

A new digitally-assisted power amplifier (DAPA) concept is introduced to boost PAE (power added efficiency) for high PAPR signals i.e. 64QAM. Dynamic CMOS digital PAs are new [5]-[6]. The DAPA concept as shown in Fig. 5 is a transformer-coupled, differential design with a main cascoded amplifier in parallel with a 4b (16 states) auxiliary (AUX_i) cascoded amplifier consisting of 8 single and 7 dual finger cells, each separately controlled via the ASIC. The AUX_i cells turn ON/OFF with a predetermined envelope level while the MAIN amplifier is always ON. This allows the amplifier to adjust with the size of the signal to avoid clipping or compression. Fig. 6 further explains the concept. A family of large-signal gain curves are generated for each state in Fig.6(a). In order to avoid gain compression, the AUX_i cells are properly binned versus input power to create a flat or linear response even though the individual cell is clipping itself. This creates a globally linear response while driving the cells nonlinearly for optimum efficiency. Fig. 6(b) overlays the DAPA DC response with a 64QAM distribution function. The lowest current is the MAIN amplifier only, and it then increases as the AUX_i cells turn-on. In practice, the cells dynamically turn-on only at the high power levels of the 64QAM signal. This lowers power consumption by over 20% while preserving linearity. Fig. 7 highlights the back-off PAE improvement.

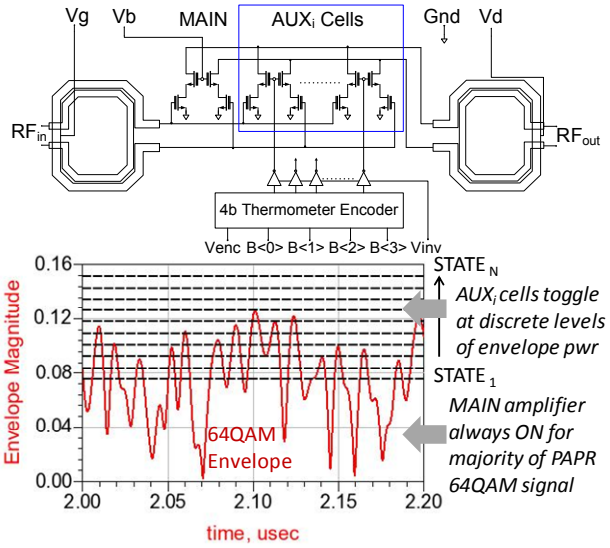

Fig. 5. DAPA schematic and simulated 64QAM envelope with notional AUX cell threshold binning levels.

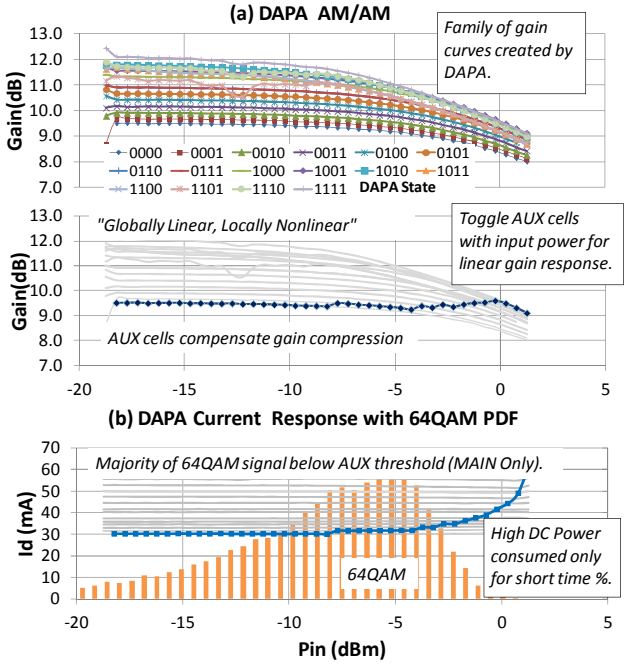

Fig. 6. (a) Measured 45GHz DAPA gain response across digital states and selected linear response with proper power binning; (b) DC response with 64QAM probability density function.

An Equiripple-Error Magnitude Estimation (EEME) algorithm is implemented for envelope estimation. It provides 0.05dB floating point accuracy. This followed by an integer and fractional clock delay for control and RF

signal alignment. A 5b cubic Farrow time interpolation filter was chosen for a fractional delay of 52ps.

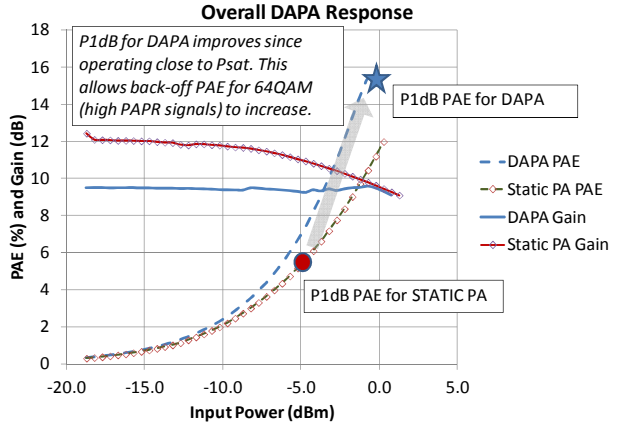

Fig. 7. P1dB PAE increases for DAPA versus Static PA.

IV. SOC MEASUREMENTS AND LAYOUT

The final SoC measurements are shown in Fig. 8.

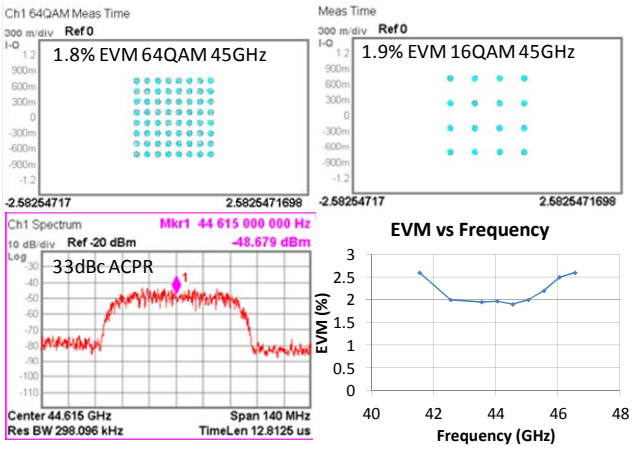

Fig. 8. Measured EVM/ACPR at 45GHz with 600MHz clock.

The measured EVM is 1.8% with 33dBc ACPR for a 64QAM signal. We also tested 16QAM since the ASIC is reconfigurable, and measured 1.9% EVM respectively. The data rate exceeds 450Mbps. The power amplifier current decreased from 320mA to 260mA with the DAPAs turned-on which is over 19% power savings. The output power is low with -10dBm integrated power even though each DAPA will provide over 12dBm Psat preventing proper DAPA time alignment. This is due to unexpected low LO drive power for the IQ modulator which reduced conversion gain, as well as increased loss due to RF routing for SoC causing PAE to be low. The plan is to increase Pout and PAE on future versions. Multiple power domains isolate the ASIC via high resistance BFMOAT layers. A 124 pad ESD protected wire bond padframe rings the periphery of the chip. The chip in Fig. 9 is 5.9mm x 5.8mm and consumes 1.6W.

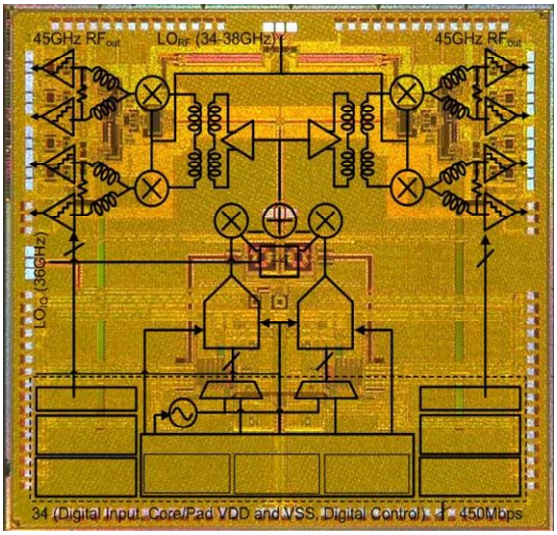

Fig. 9. Die photograph with block diagram overlaid.

V. CONCLUSION

We have successfully designed and measured the first 64QAM 45GHz transmitter SoC with digitally-assisted power amplifiers. CMOS based SoC technology will greatly enhance military systems by lowering their SWAP.

ACKNOWLEDGEMENT

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