A 130nm CMOS Polar Quantizer for Cellular Applications

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***Abstract* — A polar quantizer is presented for detection and quantization of modulated signals in cellular applications. It consists of amplitude and phase quantizers. A time-to-digital converter (TDC) is designed to measure and quantize the phase, while a typical ADC is used for amplitude quantization. Polar quantizer significantly reduces the sensitivity of the quantizer to amplitude resolution. The 10 bit polar quantizer fabricated in 130nm CMOS achieves 5.5dB of SQNR improvement compared to rectangular quantizer for signal bandwidths as high as 20MHz.**

***Index Terms* — CMOS, modulation, polar, quantizer, time-to-digital converter (TDC), SQNR.**

I. Introduction

Modern wireless communication systems need to accommodate sending/transmitting of wideband signals with sophisticated modulation schemes (e.g., 20MHz, 64QAM OFDM for LTE [1]), thereby achieving high data-rate. It not only translates to more challenging RF performance requirements in terms of linearity, noise figure (NF) and dynamic range, but also sets forth stringent requirements on the analog to digital converter (ADC) in terms of its resolution and speed. A high resolution high speed ADC that satisfies all these requirements would be power hungry, directly contributing to higher power dissipation of the RX and shorter battery life.

While polar architectures have been popularly used in RF transmitters, they have not been fully examined for RF receivers. Some scattered theoretical analyses of polar quantizers have been conducted (see [2]). Moreover, a limited use of polar architecture using injection-locking technique for the receiver design was demonstrated in [3].

In this work, we explore the idea of polar detection and quantization to enhance the signal-to-quantization noise ratio (SQNR) and relax design requirements on dynamic range and resolution of ADCs compared to a conventional rectangular quantization. The following sections illustrate, in details, the advantages of the polar quantizer, the architectural design and measurement results of a prototype chip fabricated in 130nm CMOS process.

II. Polar Quantization

A. Description

The receiver in cellular radios typically deals with non-line-of-sight (NLOS) condition. Thus when the receiver is not mobile relative to the transmitter, the channel is considered to be a flat fading channel (FFC) and the received signal is characterized with a complex Gaussian probability distribution function (PDF). This attribute can be exploited to design quantizers with high SQNRs.

The distribution of the Gaussian signal in complex plane is concentrated around the origin compared to that of a uniform signal (Fig. 1). The amplitude of a Gaussian signal has a Rayleigh PDF, implying that high amplitudes are less likely to occur. While a conventional I/Q receiver tries to detect the real and imaginary parts of the received signal (Fig. 1(b)), as was shown in [2], the uniform rectangular quantization does not produce minimum quantization noise, since it allocates equal quantization steps over the input dynamic range regardless of the amplitude of the input signal and its probability of occurrence. An alternative approach is to detect its phase and amplitude, and quantize them to reconstruct the signal in digital domain. While in each phase and amplitude domain, the quantization takes place uniformly, the area of quantization segments become smaller, as the signal amplitude becomes smaller, leading to a lower quantization error. Since the probability of receiving signals with high amplitudes is much lower than that of signals with average amplitudes, the average quantization error will be lower in this type of quantization.

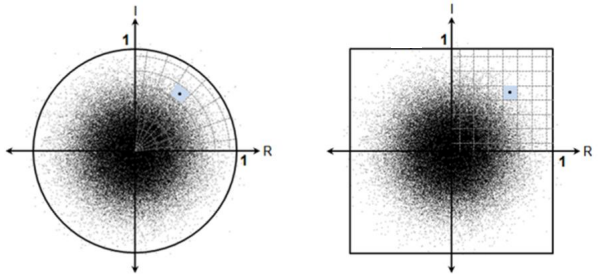


Fig. 1 Distribution of a Gaussian signal in complex plane. (a) Polar quantization; (b) Rectangular quantization.

B. Polar Quantizer Architecture

Fig. 2 shows the block diagram of the polar quantizer, where the RF/IF signal, S_{IF}, is split into two paths: amplitude and phase. The amplitude path extracts and quantizes the envelope of S_{IF}. The rate of amplitude variation is equal to symbol rate of the baseband signal S_{BB}. Therefore, the bandwidth of the amplitude signal is equal to that of S_{BB}. Thus, the sampling rate of amplitude ADC is

identical to that of an ADC used in a conventional rectangular quantizer. On the other hand, the required dynamic range of this ADC is lower than that of its counterpart by a factor of $1/\sqrt{2}$, since the signal amplitude is always positive.

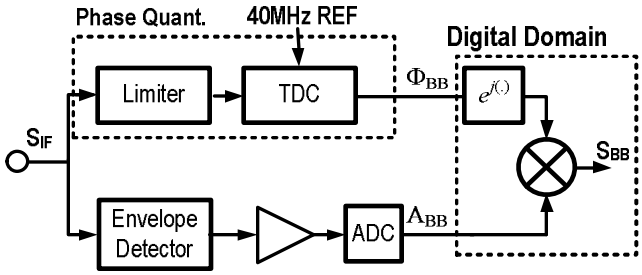


Fig. 2 Polar quantizer architecture.

The phase quantizer path consists of a limiter to remove the amplitude information, and a time-to-digital converter (TDC). The operation of TDC is described in Section III.

Comprehensive system simulations verify the superior performance of polar quantizer compared to rectangular quantizer for communications through FFCs. For Example, Fig. 3 shows that polar quantizer achieves a significantly lower symbol error rate (SER) for a 16- and 64-QAM signal, compared to a rectangular quantizer.

In addition, the received signal cannot always be amplified to the ADC's full scale in a rectangular quantizer, since the RF gain steps are discrete. As a result, the full resolution of ADCs is not always utilized. To guarantee an acceptable quantization noise, the ADC resolution should thus be chosen high enough to account for this under-utilized full scale. On the contrary, the maximum phase variation in the phase path is independent of the signal level, varying between 0^o to 360^o. Therefore, the phase quantization path does not suffer from resolution reduction, caused by discrete nature of gain steps.

III. Phase Quantizer

The phase information of S_{BB} is extracted from S_{IF} by comparing hard limited version of S_{IF} (S_{LIM}) against a locally generated reference signal (*REF*) at the same frequency. More precisely, first, the amplitude information of S_{IF} is removed by a limiter. Then, the time difference between this constant amplitude signal and *REF* is measured. The transition from one symbol of the baseband signal to another will result in sudden change in the phase of S_{IF}. Therefore, the rising edge of S_{LIM} leads or lags relative to that of the reference signal, indicating a phase change.

The time difference between S_{LIM} and *REF* is measured and quantized using a TDC. TDC enables the counters to count the number of zero crossings of high frequency clock signals (CLK) during the time interval between rising edges of S_{LIM} and *REF* [4], as shown in Fig. 4(b). This time difference is calculated as a function of clock frequency and digital outputs of the counters. Higher clock frequency (f_{CLK})

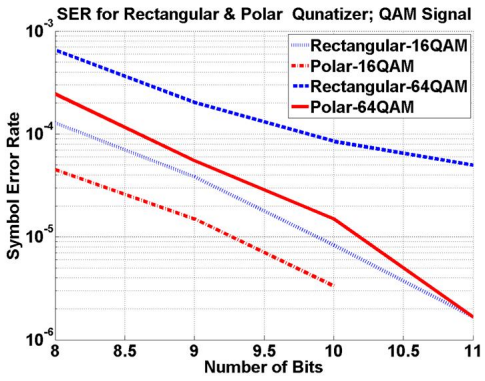
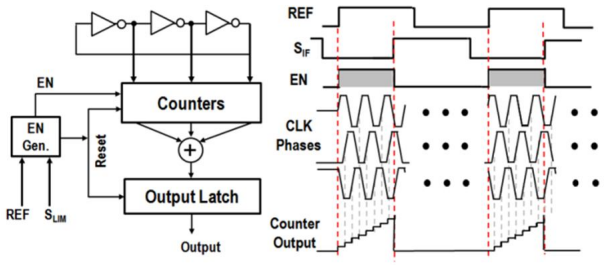


Fig. 3 Simulated SER for polar and rectangular quantizer vs. number of bits.

clearly leads to higher resolution. However, f_{CLK} cannot exceed a certain threshold due to limitations imposed by the technology. To further improve the resolution, several counters are used/enabled concurrently and are fed by the clock and its delayed versions so that more number of zero crossings is counted over the same time interval. All the counters' outputs are added together to obtain the total number of zero crossings, as depicted in Fig. 4(a). Thus, compared to a single counter, higher resolution is achieved at the same f_{CLK}. The minimum time step, t_S, is then equal to

$$t_S = \frac{1}{2Nf_{CLK}}, \qquad (1)$$

where N is the number of different phases for the CLK. To generate different phases of a rail-to-rail clock signal an inverter-based ring oscillator is adopted. Different phases of



(a) (b)

Fig. 4 (a) Simplified TDC architecture; (b) Operation principle.

the clock signal are retrieved at different taps of the ring. However, t_S is constant and independent of the number of taps (inverters), simply because increasing the number of taps in this topology decreases f_{CLK}.

To increase N without decreasing f_{CLK}, two 3-stage ring oscillators are employed and connected to a quadrature cross coupled pair, as shown in Fig. 5(b). While the oscillation frequency is determined by the ring oscillators, the quadrature cross coupled pair forces a phase difference of 90^o between these two circuits. As a result, the phase difference between each two consecutive zero crossings

reduces from 60° to 30° (doubling N from 6 to 12), leading to 50% decrease in the time step or one more bit resolution.

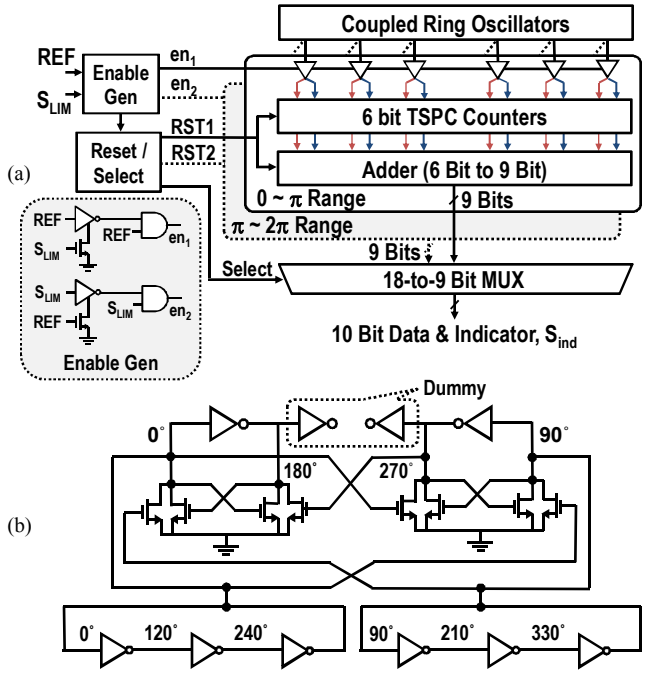


Fig. 5 (a) TDC architecture; (b) Two ring oscillators coupled through a quadrature cross coupled pair.

TDC should be able to detect the phase difference between 0° and 360°. In other words, it should be able to distinguish between the leading/lagging rising edges of S_{LIM} compared to *REF*; Such a wide phase range leaves very short reset time for counters when the phase difference gets close to 360°. Failure to reset the counters will corrupt the output of the TDC for subsequent symbols. In order to avoid this issue, the phase detection is divided into two paths; namely, 0°–180° and 180°–360°, always leaving at least half a period for reset time. At each instance, only one path is active, quantizing the time difference in the corresponding range (Fig. 5(a)). Consequently, TDC incorporates two phase detectors that generate two enable signals for each path, en_1 and en_2, based on leading/lagging conditions.

Nevertheless, distinguishing between leading and lagging edges of the input signal inevitably causes the TDC to fail generating correct enable signals in case of sudden transitions of phase from 0°–180° to 180°–360°, and vice versa, on the same detection cycle. In this situation, it takes another cycle of reference signal for TDC to correctly detect the phase and generate a valid output. Thus, the phase should at least remain constant for two cycles of the reference signal. This means that the frequency of the reference signal (or the IF frequency) is at least twice the baseband symbol rate, i.e., roughly the bandwidth of the signal. The minimum phase step $\Delta\phi$, which depends on t_S and f_{IF}, is calculated as:

$$\Delta\phi = 2\pi t_S \cdot f_{IF}. \qquad (2)$$

(2) reveals that to achieve a higher resolution, lower f_{IF} is desired. However, as mentioned before, f_{IF} cannot go below twice the bandwidth of the baseband signal, thereby setting an upper bound for the resolution.

IV. Implementation and Experiments

The phase quantizer was fabricated in a 130nm standard CMOS process. f_{IF} and f_{REF} were chosen to be 40MHz, in this design to accommodate a 20MHz of channel bandwidth. The quadrature coupled ring oscillators oscillate at 3.41GHz. With N=12, the minimum phase step is 0.35° leading to 1024 phase steps or 10-bit resolution. For each range, 0°–180° and 180°–360°, six rising-edge and six falling-edge 6-bit TSPC counters are implemented. The outputs of twelve counters are added together using a 6- to 9-bit tree adder to form a 9-bit output. Counters for 180°–360° are implemented as count-down counters to avoid any sharp transition in the output code-word. Based on en_1 and en_2, an indicator signal S_{ind} is generated to determine if the measured time difference belongs to 0°–180° or 180°–360°. This signal acts as the tenth bit of the quantizer.

To verify the desired resolution, TDC was tested using an external square wave emulating the input (S_{LIM}) at 40MHz. The phase difference between input and the signal *REF* was swept between 0° to 360°. The output code-word was measured and the transfer curve is plotted in Fig 6.

As the phase varies between 0° to 180° and 180° to 360° the TDC output goes from 0 to 512 and then comes back to 0, while S_{ind} is readily generated to determine the absolute phase. However, a dead zone exists in the vicinity of 0° (360°), caused by the fact that TDC cannot generate very narrow enable signals en_1 and en_2. The minimum width for en_1 and en_2 are measured to be 125ps and 150ps, respectively. The total of 275ps translates to 3.96° of dead zone in phase detection. However, assuming uniform distribution for the input phase, the input phase falls into the dead zone for only 1.1% of the time; hence, the effect on SER is negligible (verified by simulation).

To verify the superior performance of polar quantizer compared to rectangular one, a complex Gaussian sequence was generated and modulated with a 40MHz carrier using a vector signal generator (VSG). The signal was fed into TDC to detect and quantize the phase. An ADL5511 was used to

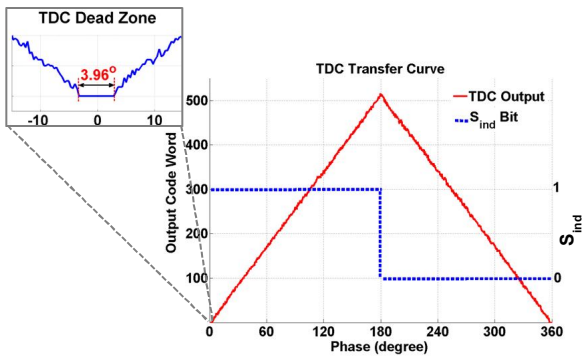


Fig. 6 Measured TDC transfer curve.

detect the amplitude. An ADC12040 12 bit ADC was used off-chip for amplitude part of polar quantization. The same ADC was used for rectangular quantization. The number of

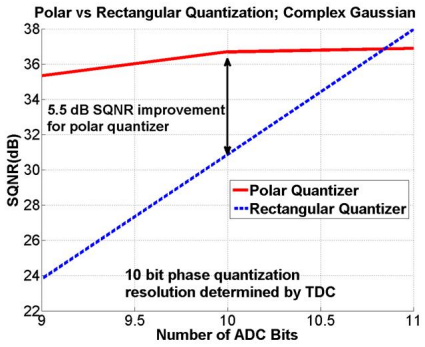


Fig. 7 Measured SQNR vs. ADC resolution. Equal number of bits for real, imaginary and amplitude parts.

bits for both the amplitude part of polar quantizer as well as rectangular quantizer is swept while the phase resolution is determined by TDC and is equal to 10 bits. Fig. 7 shows 5.5dB improvement in SQNR using polar quantizer for 10 bit resolution. It is also evident that reducing the amplitude resolution in polar quantizer from 10 to 9 bits for a fixed 10-bit TDC resolution does not degrade SQNR significantly (~1dB), translating to low quantizer sensitivity to amplitude resolution. In addition, even for 11 bits of ADC resolution, SQNR for polar quantizer is only slightly lower than that of rectangular quantizer (~1dB).

To demonstrate the capability of TDC in tracking abrupt changes in the S_{IF} phase (which could occupy more bandwidth compared to S_{BB} depending on the modulation scheme and pulse shaping filter used to generate S_{BB}), an I/Q modulator was used to alter the phase of the BPSK input signal between 128° and 128°+180° every 50ns, to find out if TDC can track the phase of the baseband signal for symbol rates as high as 20Msps. Fig 8 shows the BPSK input and reference signals, TDC outputs, input phase and quantized output phase. TDC output follows the input phase accurately.

Power consumption of TDC depends on the phase difference between input signal and the *REF*, and varies between 3.9- to 10.75-mW. The average power consumption of phase quantizer is 7.3-mW. Fig. 9 shows the die micrograph of the phase quantizer.

V. Conclusion

A novel architecture for polar quantization based on amplitude/phase detection and quantization was proposed. It not only relaxes the requirements on data converters in terms of resolution and dynamic range, but also improves SQNR. It addition it lowers the sensitivity of receivers to accuracy of RF gain as well as the ADC resolution used for amplitude quantization.

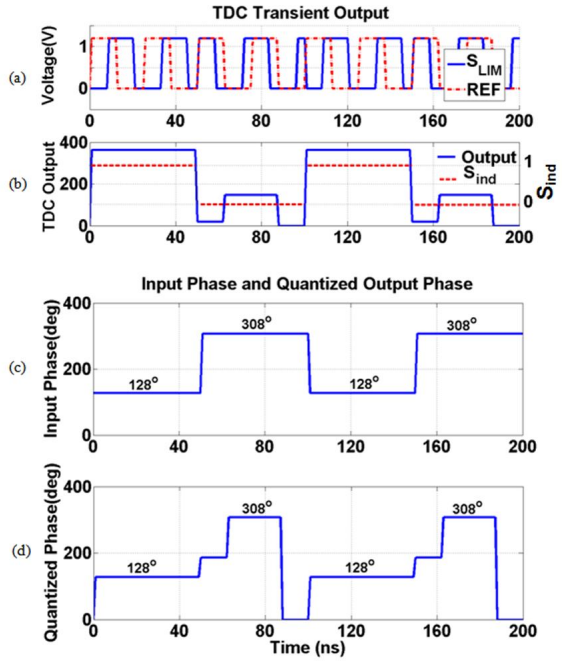


Fig. 8 (a) BPSK input and REF, (b) measured TDC outputs, (c) input and (d) measured quantized output phase.

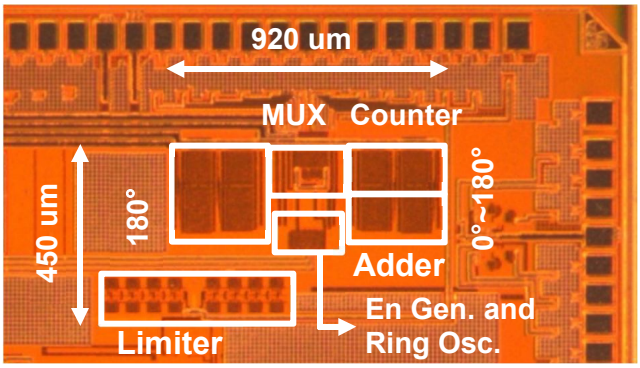


Fig. 9 Die photograph of phase quantizer.

Acknowledgement

Authors would like to acknowledge MOSIS for chip fabrication under MOSIS Educational Program (MEP). They are also thankful to Dr. Javid for his great help and support.

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