Ultra-low Voltage and Low power UWB CMOS LNA using Forward Body Biases

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***Abstract* — An ultra-wideband (UWB) low noise amplifier (LNA) was designed and fabricated using 0.18μm 1.8V CMOS technology. The adoption of forward body biases (FBB) in a 3-stage distributed amplifier enables an aggressive scaling of the supply voltages and gate input voltage to 0.6V. The low voltage feature from FBB leads to more than 50% power consumption saving to 4.2mW. The measured power gain (S_{21}) is higher than 10dB in 3.1~8.1GHz and noise figure is 2.83~4.7 dB in the wideband of 2~10GHz. Superior linearity is achieved with IIP3 as high as 4.2dBm and 12.5dBm at 6.5GHz and 10GHz, respectively.**

***Index Terms* — Low voltage, Low power, UWB, LNA, FBB, noise figure, linearity**

I. Introduction

Wideband systems have attracted an extensive research interest and development effort, due to increasing requirements of high data rate and low power in short range communication. The ultra-wideband (UWB) technology can pave the way for a wide range of applications, which use the frequency bands in 3.1 ~ 10.6 GHz and co-exist with the licensed spectrum. For an RF transceiver, low noise amplifier (LNA) acts as a key component whose gain and noise will determine the system sensitivity and dynamic range. Among the existing solutions for wideband amplifiers design, distributed amplifier (DA) has been widely used, due to its intrinsic broadband feature. However, high power consumption and large chip area becomes a roadblock hampering its applications in wideband system [1]-[3]. RC feedback topology becomes increasingly popular attributed to its advantage of superior wideband matching and flat gain. Unfortunately, it cannot offer sufficient gain and lower noise figure (NF) under the criterion of low power consumption [4]-[5]. Common gate (CG) topology [6] is one more promising solution to approach broadband input matching but the trade-offs between the gain, noise, and power dissipation remains a critical problem. For UWB technology to be viable in the hand-held wireless applications, it cannot be avoided that low power dissipation brings the most stringent challenge. In this paper, a UWB LNA with broadband impedance matching, flat gain, low noise, low voltage, low power consumption, and small chip area has been realized using 0.18μm 1.8V CMOS process, offering low cost and low power solution.

II. UWB LNA Circuit Design and Analysis

A. UWB LNA Circuit Topology

Fig.1 illustrates the circuit schematics of the proposed UWB LNA, which is composed of a common gate (CG) stage for wideband input matching, a common source (CS) amplifier at the second stage, and a source follower at the last stage as the output buffer and also for output matching.

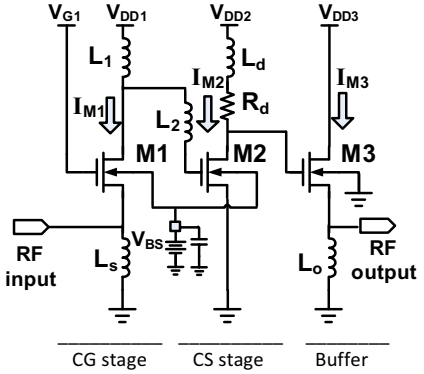

Fig. 1 The circuit schematics of the UWB LNA consisting of a CG input stage, a CS amplifying stage, and a source follower output buffer.

The function and operational principle of each component can be described according to the 3 stage architecture. First, the CG input stage contains a MOSFET M1 and two on-chip inductors, namely L_S and L_1. The input matching to 50Ω is realized by using L_S and M1's transconductance g_{m1} and gate-to-source capacitance C_{gs1}. This input matching is aimed at both power and noise matching. The second one is a CS amplifying stage, which contains a MOSFET M2, an on-chip inductor L_d, and a load resistor R_d. This CS amplifier was designed by adopting L_d and R_d to attain sufficient gain over the wide band and determine the 3dB bandwidth of this LNA. The L_d, so called a shunt peaking inductor can raise the gain at higher frequency and extend the usable bandwidth. Note that L_2 connecting M1's drain and M2's gate can achieve additional bandwidth extension. Forward body bias (FBB) scheme was employed by M1 and M2 in CG input stage and CS amplifying stage, respectively. This FBB technique can facilitate ultra-low voltage design by reducing M1 and

M2's V_T. In this way, the active power from V_{DD} can be effectively reduced. Finally, the last stage is a source follower buffer, which incorporates the third MOSFET M3 and an inductor L_O. M3 acts as a source follower with unit gain used to drive the test equipment for measuring this LNA. L_O was adopted to form with M3 as an output matching network, achieving output impedance equal to 50Ω over the wide bandwidth.

B. Common Gate Input Matching Circuit Analysis

Fig.2 (a) illustrates the circuit schematic of CG input matching network consisting of M1 represented by g_{m1} and C_{gs1} and a degeneration inductor L_S. The small signal equivalent circuit associated with this input matching stage is shown in Fig.2(b) and input impedance Z_{in} can be derived, according to (1)~(2).

$$Z_{in} = \frac{1}{g_{m1} + sC_{gs1} + \frac{1}{sL_s}} = \frac{j\omega L_s(1-\omega^2 C_{gs1}L_s) + (\omega L_s)^2 g_{m1}}{(1-\omega^2 C_{gs1}L_s)^2 + (\omega L_s)^2 g_{m1}^2} \quad (1)$$

For $\omega = 1/\sqrt{C_{gs1}L_s}$, the imaginary part of (1) vanishes and Z_{in} can be simplified to $1/g_{m1}$ to reach 50Ω by a suitable adjustment on M1's dimension and bias condition.

$$Z_{in} = \frac{1}{g_{m1}} \text{ at } \omega = \frac{1}{\sqrt{C_{gs1}L_s}} \text{ for input matching} \quad (2)$$

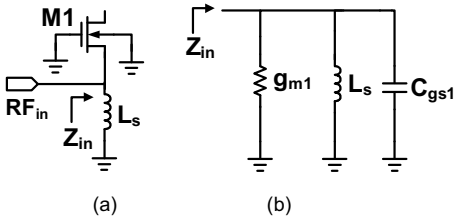

Fig.2 (a) the circuit schematics of CG input matching network (b) small signal equivalent circuit for the input impedance analysis

C. Shunt Peaking for Bandwidth Extension

The source degeneration using L_S at the CG input stage is a kind of narrow band matching technique. To meet the wide bandwidth > 5GHz required for UWB, shunt peaking method is employed for bandwidth extension to achieve flat gain over the wide band. Fig.3(a) and (b) illustrate the circuit topology and small signal equivalent circuit for the shunt peaking method. Note that C represents the effective load capacitance at the output node, including that of the subsequent stage. L_d is the inductor adopted to extend the usable bandwidth. According to Fig.3(b), the transfer function H(s) can be derived under the condition without and with L_d, given by (3) and (4), respectively. H(s) without L_d tends to degrade with increasing frequency, due to the increase of sR_dC at the denominator. As for H(s) with L_d for shunt peaking, it introduces an impedance component, sL_dg_m at the numerator, which can increase H(s) with increasing frequency and offset the degradation from sR_dC to keep the net impedance nearly constant over wider bandwidth. Note that the inductor L_d have to be optimized in the dimension to achieve high gain and should be sufficiently small so as to keep the resonance frequency, $\omega = 1/\sqrt{L_dC}$ out of the working band. The load resistor R_d is selected to place the zero-node frequency ($\omega_z = R_d / L_d$) as close as to the lower edge of the bandwidth to improve the power gain.

$$H(s) = g_m(R_d \,//\, \frac{1}{sC}) = \frac{g_m R_d}{1 + sR_dC} \quad (3)$$

$$H(s) = g_m\left[(R_d + sL_d)\,//\,\frac{1}{sC}\right] = \frac{g_m R_d + sL_d g_m}{1 + sR_dC + s^2 L_dC} \quad (4)$$

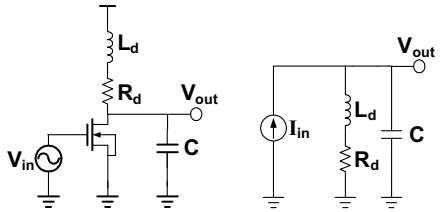

Fig. 3 (a) the circuit schematics of a CS amplifier with L_d in series with amplifier's output node as a shunt peaking scheme for bandwidth extension (b) small signal equivalent circuit for the shunt peaking circuit analysis

D. Forward Body Biasing Technique

The distributed amplifier (DA) has been widely used for wideband design, attributed to its intrinsic advantage of wideband input and output impedance matching. However, power consumption appears as the major drawback for DA in low power applications. FBB was implemented in this UWB LNA as a solution for low voltage and low power design. The operational principle of FBB technique is the lower V_{DD} associated with lower V_T driven by FBB. The effective reduction of V_{DD} can lead to power reduction. Referring to Fig. 1 for the circuit schematics of the proposed UWB LNA, FBB is adopted for M1 and M2 at CG input matching stage and CS amplifying stage, respectively. The FBB effect on the proposed UWB LNA performance was verified by ADS simulation. ZBB with V_{BS}=0V or FBB with V_{BS}=0.6V were applied to the body node of M1 and M2 simultaneously for this evaluation. First, the supply voltages to the drain and gate, such as V_{DD}=0.6V were fixed the same for different body biases like ZBB and FBB. The simulation result shown in Fig.4 indicates that FBB (V_{BS}=0.6V) can improve LNA performance in terms of higher power gain (S_{21}), lower noise figure (NF) and maintain sufficiently low input and output return loss (S_{11} and S_{22}). Then, the supply voltages were modified for ZBB to reach the performance achieved by FBB. Further simulation indicates that $V_{DD1}/V_{DD2}/V_{DD3}$ applied to CG/CS/output buffer stages have to be increased from 0.6V to 0.85V/0.7V/0.7V to reach the performance comparable with that under FBB. Table 1 summarizes the

performance under FBB and ZBB for a comparison. Note that FBB can help reduce V_{DD} from 0.85V for ZBB to 0.6V for FBB and reduce the power consumption by 3.92mW, from 7.815mW (for ZBB) to 3.89mW (for FBB), that is around 50% power saving for keeping all other performance parameters comparable.

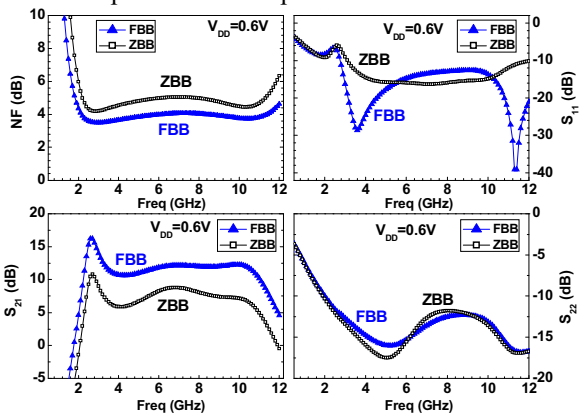

Fig. 4 Comparison of UWB LNA performance between ZBB (V_{BS}=0) and FBB (V_{BS}=V_{DD}=0.6V), fixed V_{DD}=0.6V (a) Noise figure, NF (b) power gain S_{21} (c) S_{11} (d) S_{22}.

Table I Comparison of UWB LNA performance between FBB (V_{BS}=V_{DD}=0.6V) and ZBB (V_{BS}=0,V_{DD1}=0.85V, V_{DD2}= V_{DD3}=0.7V)

UWB LNA Performance ADS Simulation	Unit	TT_FBB	TT_ZBB
Frequency	GHz	3.1 ~ 10.6	3.1 ~ 10.6
Supply Voltage : V_{DD1}	V	0.6	0.85
Supply Voltage : V_{DD2}, V_{DD3}	V	0.6	0.70
Body bias (V_{BS})	V	0.6	0
Bias current (core)	mA	5.70	9.07
Bias current (total)	mA	6.49	10.92
Power consumption (core)	mW	3.42	6.520
Power consumption (total)	mW	3.89	7.815
Gain S_{21} max / min	dB	13.28/10.63	13.48/10.9
Noise figure (NF) min/ max	dB	3.51/4.07	2.98/3.86
Input Return Loss, S_{11}	dB	< -12.3	< - 14
Output Return Loss, S_{22}	dB	< -13.48	< -14.04
Linearity, IIP3 @10GHz	dBm	-13.8	-9.2
Reverse isolation, S_{12}	dB	< -43.2	< -47.3

III. CHIP FABRICATION AND MEASUREMENT

The designed UWB LNA was fabricated in 0.18μm RF CMOS technology. Fig. 5 illustrates the chip layout and on-wafer measurement setup. The chip area including all RF and dc pads is as small as 0.874mm^2.

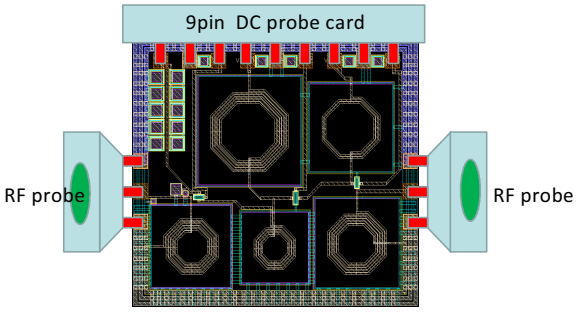

Fig.5 UWB LNA chip layout and on-wafer measurement setup for chip characterization

IV. RESULTS AND DISCUSSION

Fig.6(a)~(f) present the key performance parameters, such as input return loss (S_{11}), output return loss (S_{22}), power gain (S_{21}), reverse leakage (S_{12}), noise figure (NF_{50}), and stability (μ) measured from this UWB LNA chip under FBB (V_{BS}=V_{DD}=0.6V). The predicted performance from post-layout simulation is put in the same plot for a serious comparison. The results indicate that the measured characteristics can match post-layout simulation in the domain of 3 ~ 8GHz but show some degradation in input matching and power gain, i.e. higher S_{11} and lower S_{21} at higher frequencies, above 8 GHz. The power loss through the parasitic capacitance to the lossy Si substrate is proposed as the underlying mechanism. This kind of power loss generally increases dramatically when increasing frequency. Fig.7 presents the measured P_{out} versus P_{in} in which the third-order intercept point (IIP3) is determined from the intercept of fundamental and third order harmonic distortion (IMD3) term. As shown in Fig.7(a) and (b), the IIP3 can reach as high as 4.2 dBm and 12.5 dBm at 6.5 GHz and 10GHz, respectively.

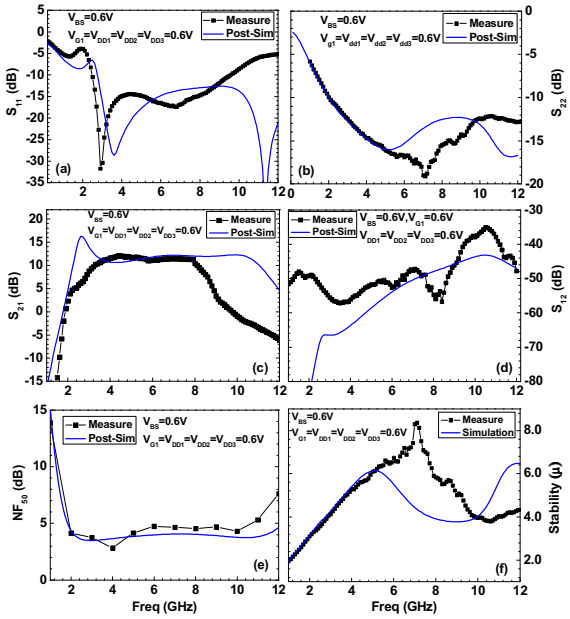

Fig.6 Comparison of measurement and post-layout simulation for UWB LNA under FBB (V_{BS}=V_{DD}=0.6V), 1~11GHz (a) S_{11} (b) S_{22} (c) S_{21} (d) S_{12} (e) NF_{50} and (f) μ (stability)

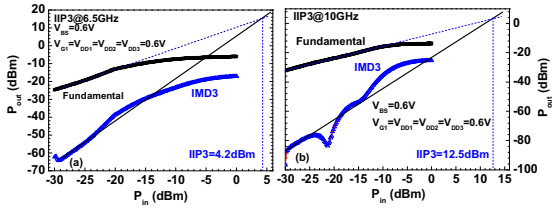

Fig. 7 Third order intercept point (IIP3) measured from UWB LNA (a) 6.5GHz (b) 10GHz, IIP3=12.5dBm

Table 2 summarizes the key performance parameters measured from this UWB LNA, and the comparison with post-layout simulation. The power gain achievable from this UWB LNA is S_{21}=10.14~12.08 dB in 3.1 ~ 8.1 GHz, which are around 1.2/0.5 dB lower than the max/min gain predicted by simulation. The measured NF_{50} is close to the simulation in the wide band of 2~10GHz. The min. NF_{50} is as low as 2.83 dB and the max. NF_{50} can be kept below 4.7 dB. This is an important achievement for LNA design and suggests the success of input inductive degeneration and bandwidth extension method using L_S and L_2. As for the linearity, the measured IIP3 can be as high as 4.2/12.5 dBm at 6.5/10 GHz. The power dissipation can be reduced to as low as 3.72mW for core only and 4.2mW for the whole chip, attributed to the ultra-low V_{DD} driven by FBB. This low power consumption matches simulation to nearly 95% and becomes the most appealing advantage realized by FBB technique. Table 3 summarizes UWB LNA performance in recent publications accomplished by using different circuit topologies, such as cascode, DA, CG and CS fabricated in 0.18µm, 0.13µm, and 90nm CMOS processes [7]-[10]. The comparison indicates that the UWB CMOS LNA realized in this work offers the advantages of sufficient gain (S_{21}>10dB) and bandwidth, lower NF_{50}, and higher linearity (IIP3) achieved by the lowest V_{DD} and power consumption. According to the figure-of-merit (FOM) defined by (5) including S_{21}, bandwidth (BW), noise figure (NF), and power dissipation (P_{diss}), UWB LNA in this paper can offer the best FOM with major contribution from lowest P_{diss} and lower NF.

$$FOM = \frac{S_{21(\max.dB)} \times BW_{GHZ}}{NF_{(\min,dB)} \times P_{diss(mW)}} \quad (5)$$

Table 2 Comparison of UWB LNA performance between post-sim and measurement under FBB

UWB LNA Performance	Unit	Post-sim	Measured
Frequency	GHz	3.1 ~ 10.6	3.1 ~ 10.6
Supply Voltages (V_{DD1}=V_{DD2}=V_{DD3})	V	0.6	0.6
Body bias (V_{BS})	V	0.6	0.6
Bias current (core)	mA	5.70	6.2
Bias current (total)	mA	6.49	7.0
Power consumption (core)	mW	3.42	3.72
Power consumption (total)	mW	3.89	4.20
Gain S_{21} max / min	dB	13.28/10.63	12.08/10.14
Noise figure (NF) min/ max	dB	3.51 / 4.07	2.83 / 4.7
Input Return Loss, S_{11}	dB	< -12.3	< - 12.45
Output Return Loss, S_{22}	dB	< -13.48	< -11.64
Linearity, IIP3 @10GHz	dBm	-13.8	12.5
Reverse isolation, S_{12}	dB	< -43.2	< -47.3

V. CONCLUSION

The UWB LNA in this design presents the advantages of low power dissipation (P_{dc}=4.2mW) from ultra-low V_{DD} of 0.6V, low noise (NF_{50}=2.83~ 4.7dB) and high linearity (IIP3@6.5/10GHz=4/12.5dBm) in the broad bandwidth, and small chip area (0.874mm^2). FBB has been proven as the major contributor to enable an aggressive reduction of V_{DD} in this 3-stage DA. It provides a promising solution for ultra-low voltage and low power UWB design using low cost RF CMOS technology.

Table 3 UWB LNA Performance Benchmark

UWB LNA	This work	[7]	[8]	[9]	[10]
Technology	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	90nm CMOS	0.13µm CMOS
BW(GHz)	3~8.1	0.4~10	2.7~9.1	2.6~10.2	1~10.6
V_{DD}(V)	0.6	1.8	0.6	1.2	---
P_{diss}(mW)	4.2	12	7	7.2	18
S_{21} (dB)	12.08/10.14	12.4/---	10	12.5~	16.75/15.25
NF (dB)	2.83/4.7	4.4/6.5	3.8/6.9	3/7	3.62/4.18
S_{11} (dB)	< -12.45	< -9	< -10	< -9	< -8
S_{22} (dB)	< -11.64	< -20	< -10	----	< -7
S_{12} (dB)	< -47.3	---	----	< -45	---
IIP3(dBm)	4.2@6.5GHz 12.5@10GHz	-6@6GHz	0@6GHz	----	---
Circuit Topology	3-stage DA CG+CS+FBB	CG+CS	2-stageDA +CS Amp.	Cascode Current-reuse	Current-reuse Noise cancel
Chip size	0.874	0.42	1.5725	0.64	0.5
FOM	5.544	2.255	2.406	4.398	2.468

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REFERENCES

[1] R.-C. Liu *et al.*, "A 0.6-22-GHz Broadband CMOS Distributed Amplifier," in *Proc. IEEE RFIC Symp. ,Jun. 2003,* pp. 103-106.

[2] H.-T. Ahn *et al.*, "A 0.5-8.5 GHz Fully Differential CMOS Distributed Amplifier," *IEEE JSSC,* vol. 37, pp. 985-993, Aug. 2002

[3] B. M. Ballweber *et al.*, "A Fully Integrated 0.5-5.5 GHz CMOS Distributed Amplifier," *IEEE JSSC,* vol. 35, pp. 231-239, Feb. 2000.

[4] K.-C. He *et al.*,"Parallel-RC Feedback Low-Noise Amplifier for UWB Applications," *IEEE Trans. Circuits and Systems –II*, vol.57, pp.582-586, Aug. 2010

[5] J. Jung *et al.*, "Ultra-wideband Low Noise Amplifier using a Cascode Feedback Topology," *Microwave and Optical Technology Letters,* vol. 48, pp. 1102-1104, Jun. 2006.

[6] Y. Lu *et al.*, "A Novel CMOS Low-Noise Amplifier Design for 3.1- to 10.6-GHz Ultra-wide-band Wireless Receivers," *IEEE Trans. Circuits and Systems- I,* vol. 53, pp. 1683-1692, Aug. 2006.

[7] K.-H. Chen *et al.*, "An Ultra-wide band 0.4-10GHz LNA in 0.18µm CMOS," *IEEE Trans. Circuits Syst.II, exp.briefs*, vol.54, pp.217-221, 2007

[8] Y.H. Yu *et al.*, "An Ultra-low Voltage UWB CMOS Low Noise Amplifier," in *Proc. APMC* 2006, pp.313-316

[9] G. Sapone *et al.*, "A 3-10-GHz Low Power CMOS Low Noise Amplifier for Ultra Wideband Communication," *IEEE Trans. Microwave Theory and Techniques*, vol. 59, pp. 678-686, Mar. 2011.

[10] A. M. El-Gabaly *et al.*, "Broadband Low-Noise Amplifier With Fast Power Switching for 3.1-10.6-GHz Ultra-Wideband Applications," *IEEE Trans. Microwave Theory and Techniques*, vol. 59, pp. 3146-3153, Dec. 2011.