A High-Resolution Short-Range CMOS Impulse Radar for Human Walk Tracking

Piljae Park, Sungdo Kim, Sungchul Woo, and Cheonsoo Kim
SoC Department, Electronics and Telecommunications Research Institute (ETRI),
218 Gajung, Yuseung, Daejeon 305-700, South Korea

***Abstract* — A single-chip impulse radar transceiver is presented. A high-resolution, enhanced SNR and controllability are achieved with a proposed architecture. By controlling timing between the transmit (TX) pulse and sampling clock of the receiver, echo pulses from targets are received and recovered. The TX pulse can adjust its spectrum occupancy by changing impulse shape. The 4-channel sampling receiver consists of a low noise amplifier, track and hold samplers, integrators, and a cascaded triple delay locked loop. The embedded control logic allows the radar to enhance the SNR of the received pulse using an averaging technique, and to operate at multiple reception modes.**

The real-time radar system measurements show that echo pulses are recovered with $\geq$100-psec range resolution while consuming 80 mW from 1.2-V of V_{dd}. An in-door human walking trace is successfully recorded. The transceiver is fabricated in a 130-nm CMOS technology occupying chip area of 3.4 mm^2.

***Index Terms* — UWB radar, radar measurements**

I. Introduction

Impulse radars have various applications from surveillance application to non-invasive bio-medical instruments. For these applications, range resolution and receiver sensitivity are critical requirements. Short pulses are transmitted and the target information is attained based on the received echo pulses from targets.

Recently, impulse radar systems using CMOS technology have been published [1] [2] [3]. While correlation based receivers, such as [3], work certain applications, its performance heavily depends on the match of the received pulse with transmitted pulse. In general, however, pulses are distorted when transmitted and received through the air. Thus, it has a limitation to obtain high spacial resolution. A receiver that does not restrict RX pulse shape is advantageous for high resolution in various clutter environments as well as antenna adaptation.

In this paper, the single chip impulse radar transceiver for a surveillance sensor network is proposed and human walk tracking is demonstrated. As the receiver is based on sampling rather than correlation, a high resolution is achieved and echo pulse distortion does not degrade system performance. Utilizing the DLL having embedded logic for the clocks required, the receiver achieves control flexibilities with small chip area; coarse and fine clock phases are available to select and sweep a certain range. An averaging technique is adapted in both circuit and signal processing domain to improve performance of the receiver. Using a digital signal processing (DSP) unit, the real time performance of the radar system is evaluated.

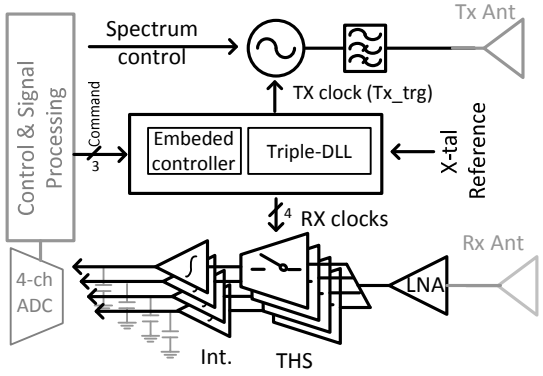

Fig. 1. The block diagram of the proposed radar. The single chip radar corresponds to the black line. The entire radar system is realized in two boards (radar, DSP) and broad band antennas.

II. A CMOS Impulse Radar

A. A Radar Architecture

A CMOS high-resolution impulse radar transceiver is proposed using a spectral adjustable impulse transmitter and high-resolution receiver adapting cascaded triple DLLs with embedded logic. Fig. 1 shows a simplified system block diagram. The transmitter radiates impulses that occupy 3$\sim$5 GHz band at the trigger signal (i.e., TX clock) rate. The trigger frequency, or pulse repetition frequency (PRF), is set to 10 MHz to accommodate upto 15-m range. The radiated impulses bounce back from targets and the echo signals are recovered in the receiver. The reception range is determined by the time difference between TX clock and receive (RX) clock since the echoes are sampled and reconstructed in the receiver. For the high resolution reception, sampling clocks of sub-nano second are required. A cascaded DLL is adapted to provide the TX/RX clocks of the radar. By switching the multiplex

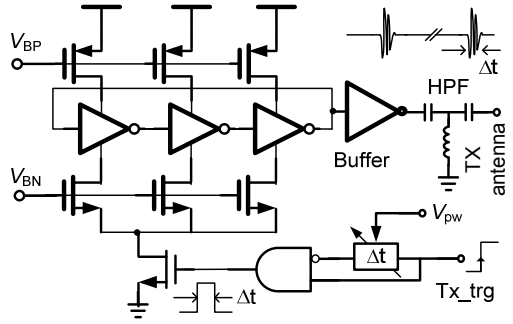

Fig. 2. The schematic diagram of the spectrum adjustable impulse transmitter.

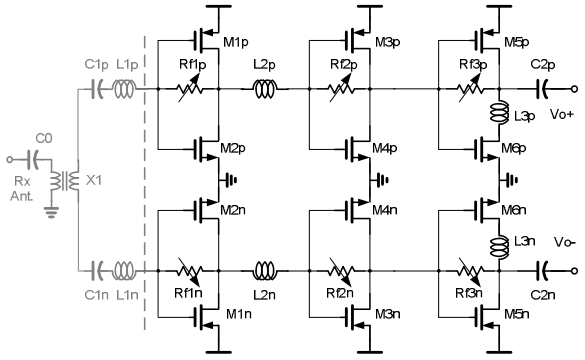

Fig. 3. The LNA schematic diagram. Grey line shows off-chip components.

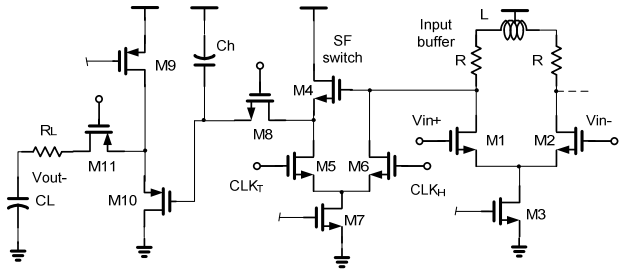

Fig. 4. The half circuit of the track and hold sampler (THS).

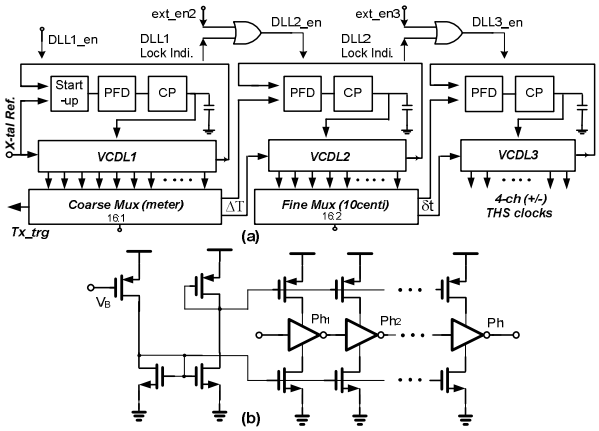

Fig. 5. The schematic diagram of (a) the triple DLL and (b) VCDL cell used in the DLL

(MUX) blocks in the DLL, timing relations between clocks are established and reception range is set. The logic block can alter radar reception mode (e.g., full-range/window-range mode), and perform averaging operation. Multiple pulses are be transmitted for measuring a single range point in order to improve SNR of measurements. The radar system is realized in two PCB boards and broadband antennas.

B. An Adjustable Impulse Transmitter

An impulse transmitter with adjustable pulse shape is utilized for the radar. In order to fit into the spectrum mask specified, the pulse shape can be altered.

Fig. 2 depicts the block diagram of the transmitter. The transmitter consists of three main blocks: a ring oscillator using current staved inverters, a trigger circuit, and an antenna driving buffer with a pulse-shaping high pass filter (HFP). To create adjustable TX pulses, the ring oscillator turns on and builds up an oscillation during the trigger circuit defined period of time Δt. Using delay cells and combination logic gates, the trigger circuit can provide variable Δt from 500 psec to several 10s nsec. Noe that the positive edges of the TX clocks from DLL initiate TX pulses, and the time between these to RX clocks defines radar receive range. Since current starved inverters are used for the oscillator, the steady-state oscillation frequency can be set by changing the delay of inverters. The ring oscillator in the transmitter is biased to have a 4-GHz steady-state oscillation frequency. To drive 50-Ω external sinusoid antenna used for the radar system, a buffer and HPF are used at the final stage. To reduce power spectral density at low frequencies, the integrated HPF is set to have a cutoff frequency of $\sim$3 GHz.

At 10 MHz PRF operation, sub-mW of power is consumed for the transmitter.

C. A High-Resolution Sampling Receiver

A 4-channel (4-ch) sampling receiver sharing a single LNA is used to receive and recover echo pulses from targets. As shown in Fig. 3, a wide-band LNA is designed based on three-stage resistive-feedback inverter structure in order to minimize the distortion – ringing – of the impulse signal. The increased pulse width due to ringing can blind a certain range, when large prolonged clutter pulses exist. Thus, ringing is highly undesirable for high-resolution radars using impulses. In order to obtain broadband characteristics, an inductive peaking technique

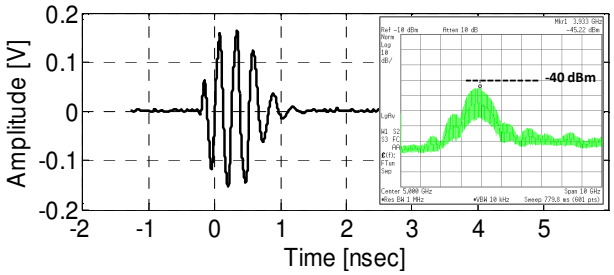

Fig. 6. The measured TX pulse (1-nsec of pulse width).

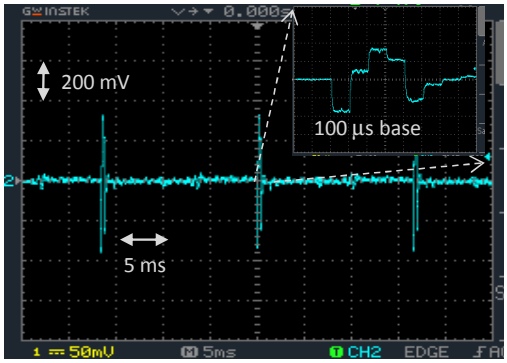

Fig. 7. The measured results of single channel output at the integrator load. Note that the all 4-ch results are combined in signal processing domain for the echo pulse recovery.

is used. By inserting adjustable feedback resistors between the input and output of the inverter, a flat and variable gain characteristics are obtained. From 3 to 5 GHZ, measured results show a power gain of 25-32 dB, noise figure of 3.25-4.1 dB, and IIP3 of $\sim$−24 dBm at 4.0 GHz.

In the core of the impulse receiver, THSs are adapted to sample wide-band differential input signals (i.e., impulses). Fig. 4 shows a half circuit of THS. To enhance bandwidth, an inductor peaking load is used at the front stage of the THS. A source follower switch is used and it is operating with RX clocks: track and hold clocks. The clock feedthrough to the load capacitor is blocked with transistors M_8. The final stage of the THS has PMOS transistors (M_9, M_{10}), and the voltage at the charge capacitor (C_h) is transfered to the load capacitor (C_L). The nominal V_{dd} of 1.2 V is used for the THS, whereas some of published works use boosted voltages [1] [4]. The voltage at the last stage load capacitance drives the integrator (not shown in Fig. 4) that charges off-chip capacitor interfacing with an external ADC. A cascaded triple DLL is proposed to generate required clocks (i.e., TX and RX clocks) for the radar transceiver. A multiple stages DLL for the radar has several advantages. First, switching delay variation for the clock selection can be remained smaller. Second, the control logic for the radar range is easily implemented as each DLL has corresponding range windows. Block diagram of the DLL is shown in Fig. 5(a). The DLL provides the 4-ch THSs with RX clocks having $\sim$100 psec time difference for each channel. Each DLL supplies accurate multi-phase clocks using a built-in feedback loop consisting of a phase detector, a charge pump and voltage controlled delay lines (VCDL). Fig. 5(b) shows a VCDL block in the DLL. The first DLL operating at a typical 10 MHz reference provides TX clock (Tx_trg). The clock phases of the first DLL VCDL corresponds to a meter resolution. The second DLL having input references from the first DLL provides clock phases that is further divided at the last stage DLL for RX clocks. To prevent false lock of the DLL, a start-up circuit and lock indicators are used.

D. An Embedded Radar Control Logic

As discussed in earlier section, the cascaded triple DLL features a simple architecture and easy control. The control logic is designed with hardware description language and synthesized. A receive range control has two different modes: full-range and window-range reception modes. The modes changes with external commands through three-wire serial interface from the control and processing unit in a separate board (see Fig. 1). A window-range mode, from 2- to 4-m for example, selects a TX clock from the first DLL phases that have corresponding time delay of pulse round-trip time. Then, by orderly sweeping the 2nd DLL phases, fine range sweep reception is performed. The radar receiver in the paper uses averaging techniques both circuit design and signal processing. For the reception, multiple pulses are transmitted to receive a single range point. This is done by the repeated RX clock selection using embedded logic. Also, the integrator circuit – transconductance amplifier – that charges off-chip capacitor load is utilized. In signal processing, multiple reconstructed echo pulses are used for a target decision. With these averaging schemes, an improved SNR is attained; random noise from the front-end stage as well as clock jitter can effectively be canceled out. The embedded logic can set the front-end stage with different gain mode. TX pulse shape can be altered to best extract the target features.

III. Measurement Results and Discussion

Fig. 6 depicts measurement results of the transmitter. A pulse having $\sim$1-nsec pulse width and 3-to-5 GHz spectrum occupancy is shown. The inset corresponds to the power spectral density of the pulses. As discussed in section II-B, the transmitter can adjust its pulse shape; in spectral domain, a center frequency and bandwidth are altered. The measured results confirm that the pulse width varies from 500 psec to several 10s nsec. The center

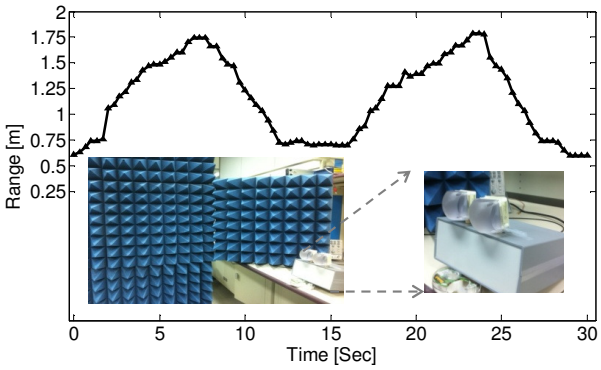

Fig. 8. The in-door human walk tracking results. The insets show measurement environment and radar system used for the experiments.

frequency changes from 1.2 GHz to above 4 GHz. The bandwidth of the pulse changes $\geq$2 GHz to several 10s MHz. To evaluate the receiver performance, pulses from the on-chip transmitter are fed into the receiver through a cable with an attenuator. For the measurements in Fig. 7, the radar mode is set as follow: first DLL phase sweeps 1 to 12 which corresponds $\sim$12-m range, second DLL is at full 16-phase sweep, average number of 1000 is set, an external 10 MHz reference is used. According to the average number set, 1K times of measurements are accumulated as a voltage at the off-chip capacitor for a single range point. A stair-like 100-μsec (1K x 1/10MHz) response is obtained. As with first and second DLL settings, period of 16.5 msec (11x15x100 μsec) is observed. The Fig. 7 shows only single channel measurements. In order to recover the pulses, 4-ch measurement data need to be aggregated. A range resolution of $\sim$1.5 cm is achieved and the accuracy is about the resolution when delay offset between TX and RX path is calibrated. The stand-alone real-time radar system adapting the radar transceiver in this paper measures walking human and the results are depicted in Fig. 8. For the experiments, the single-chip radar transceiver, a digital signal processing board using a commercial chip, and broad-band sinusoid antenna are utilized. The radar system operates simultaneously performing following process: transmitting pulses, echo pulse receiving, data processing, and results report to the sensor network. For data logging, a JTAG port on the DSP board is used. Recorded real-time, in-door measurements of walking trace are shown in Fig. 8. A $\sim$1.2 meter back-and-forth movement is clearly shown with time. The radar transceiver is fabricated in a 130-nm CMOS technology with options of top thick metal (3.35 μm) and MIM capacitor (1.5 fF/μm^2). A 48-pin QFN (quad-flat no-leads) package is used for the prototype radar chip. Fig. 9 shows die photo of the fabricated radar

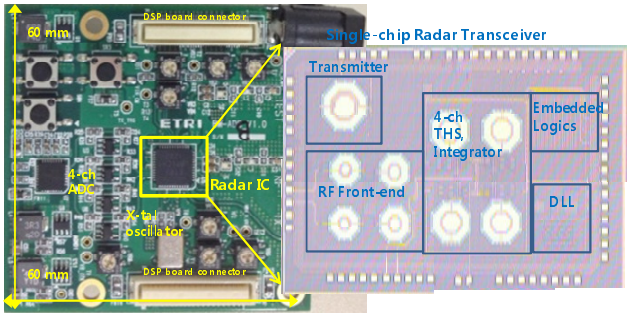

Fig. 9. The radar board and the micro-photograph of the fabricated radar transceiver.

transceiver chip and radar board. The transceiver occupies chip area of 3.4 mm^2 including pads. Power consumption of the entire transceiver is $\sim$80 mW from 1.2-V of V_{dd} at the maximum gain.

IV. Conclusions

This paper presents a single-chip, short-range, high resolution impulse radar transceiver for a sensor network. A spectrum adjustable impulse transmitter is demonstrated. Controllable pulse shape is achieved; pulse width of sub to tens of nano second, and a center frequency of 1.2 GHz to above 4 GHz are obtained. A 4-ch sampling receiver that includes a broad-band LNA, THS, a triple-DLL, and control logic is proposed. With built-in logic the radar can be operated in different modes, such as full-range, or window-range modes. A real-time in-door human walk tracking results are shown using the radar system incorporating radar transceiver in the paper, a DSP board, and antennas.

Acknowledgment

This work was sponsored by Dual Use Technology Program of DUTC (UM11018RD1).

References

[1] Ta-Shun Chu, *et al* "A short-range UWB impulse-radio CMOS sensor for human feature detection," *2011 IEEE International Solid-State Circuit Conference Digest of Technical Papers*, pp. 294-296, Feb. 2011.

[2] D.T. Wisland, *et al* "A CMOS nanoscale impulse radar utilized in 2-dimensional ISAR imaging system," *2012 IEEE Radar Conference*, pp. 714-719, May. 2012.

[3] D. Zito, *et al* "SoC CMOS UWB Pulse Radar Sensor for Contactless Respiratory Rate Monitoring," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 5, Issue 2, pp. 503-510, Dec. 2011.

[4] S. Shahramian, *et al* "A 30-GS/sec Track and Hold Amplifier in 0.13-μm CMOS Technology," *2006 IEEE Custom Integrated Circuits Conference*, pp. 493-496, Sep. 2006.

[5] Che-Fu Liang, *et al* "A Calibrated Pulse Generator for Impulse-Radio UWB Applications," *IEEE Journal of Solid-State Circuits*, vol. 41, Issue 11, pp. 2401-2407, Nov. 2006.