A 0.5-to-3 GHz Software-Defined Radio Receiver Using Sample Domain Signal Processing

Run Chen and Hossein Hashemi

Department of Electrical Engineering - Electrophysics,
University of Southern California, Los Angeles, CA 90089

***Abstract* — A 0.5-to-3 GHz software-defined radio receiver leveraging Sampled Domain Signal Processing (SPSD) is demonstrated in a 65nm LP CMOS technology. The SDSP approach achieves band-pass filtering, harmonic rejection, and frequency translation simultaneously. Input impedance matching is achieved in an active translational loop that tracks the desired RF frequency. The chip includes a wideband frequency synthesizer, multi-phase non-overlapping clock generation circuitry, bandgap and power supply regulators. It achieves out-of-band IIP3 > 11.7 dBm, IIP2 > 58 dBm, NF = 5.5 ~ 8.8 dB, and uncalibrated 3rd and 5th order harmonic rejections exceeding 47 dB and 52 dB, respectively.**

***Index Terms* — receiver, software-defined radio (SDR), sample domain, CMOS, wideband, reconfigurable.**

I. Introduction

Frequency allocation regulations combined with the rapid introduction of new wireless standards and applications have led to a high demand for integrated multi-mode, multi-band, and multi-standard wireless transceivers. The high nonrecurring engineering cost and development time associated with a new wireless transceiver hardware design has inspired the Software-Defined Radio (SDR) concept where the same wireless transceiver can be programmed to support any existing or upcoming standard.

The major challenge in designing SDR receivers is maintaining a high dynamic range over a wide frequency range. Direct down-conversion has been the preferred architecture in CMOS receivers due to its low area and power consumption. However, in wideband SDR receivers without a selective front-end filter (*e.g.*, SAW), interferences around the Local Oscillator (LO) frequency or its harmonics reduce the receiver dynamic range. To address these issues, passive-mixer based receiver architectures [1][2][3][4] and harmonic-reject receiver architectures [2][4][5] have been proposed. The higher transit frequency (f_T) of highly scaled CMOS transistors enables realization of techniques traditionally used in low frequency analog design, such as switched capacitor techniques, at radio frequency [5][6]. This opens up new possibilities for reconfigurable and software programmable radio architecture.

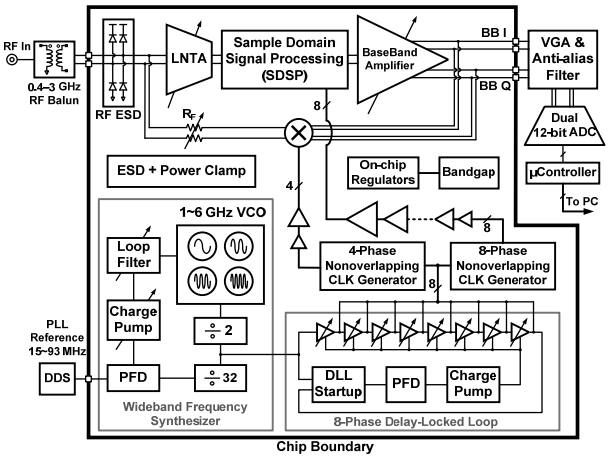

Fig. 1. Block diagram of the Sample Domain Signal Processing (SDSP) based SDR receiver.

The main contribution of this work is the demonstration of an SDR receiver architecture based on Sample Domain Signal Processing (SDSP) that achieves high dynamic range, harmonic rejection, and input impedance matching simultaneously.

II. Architecture

The proposed SDSP based receiver architecture is shown in Fig.1. The receiver front-end is a Low Noise Transconductance Amplifier (LNTA). A subsequent SDSP block translates the RF signal into quadrature baseband signals while rejecting the LO harmonics and achieving selective band-pass filtering. A translational loop is used for input impedance matching [7], in which the baseband signal is frequency up-converted and fed-back to the input through R_F. The input impedance is hence set by the ratio of R_F and the overall loop gain, and tracks the LO frequency. The receiver also includes an on-chip wideband frequency synthesizer, a multi-phase non-overlapping clock generator, bandgap and power supply regulators. The highly programmable chip allows independent control of the individual component values and bias operating points in nearly all individual building blocks. This fine-grained dynamic programmability enables an optimum performance under various situations (*e.g.*, modulation format, blocker level, SNR).

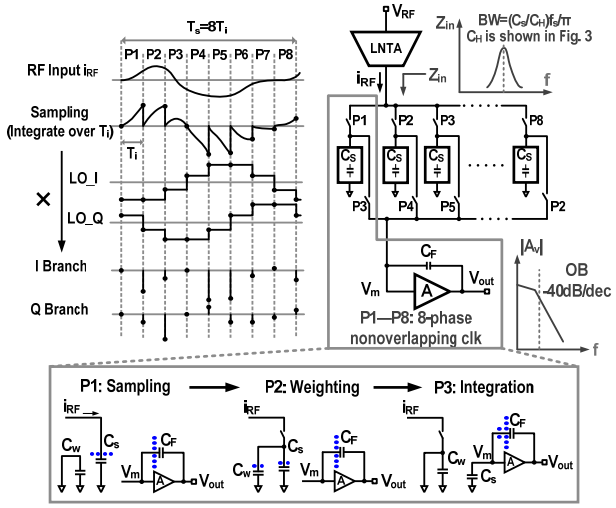

Fig. 2. SDSP operation principle.

The SDSP block (Fig. 2) contains 8 sampling units which are controlled by an 8-phase non-overlapping clock in an interleaved pattern. Each sampling unit contains a sampling capacitor, C_S, a weighting capacitor, C_W, and several MOS switches. For a typical zero-IF direct down-conversion scheme, the clock frequency, $1/T_S$, is equal to the RF frequency, f_{RF}, and each phase endures $T_S/8$. In order to achieve frequency translation and harmonic rejection, each sampling unit processes the signal in three phases: sampling, weighting, and integration. During the sampling phase, the RF current charges the pre-discharged C_S and converts the signal from a continuous waveform to discrete charges. The weighting process involves multiplying the sampled signal (charge) by a factor such that the equivalent LO waveform looks like a sinusoidal wave and does not contain 3rd and 5th harmonic components. This is accomplished by appropriate sizing the capacitance ratio between C_S and C_W which share the charge in this phase. The remaining charge on C_S is transferred to baseband amplifier feedback capacitor C_F while C_W is discharged in the integration phase. C_F continuously collects the remaining charge from all sampling units and the output voltage contains the down-converted RF information. In the actual implementation (Fig. 3), one more capacitor C_H is added in each sampling unit to ensure the input impedance of the SDSP is always low. It can be shown that this impedance has a bandpass shape centered at f_{RF} with bandwidth given by $(C_S/C_H)\cdot fs/\pi$. Therefore, voltage swing at the LNTA output remains low while out-of-band interferences are also attenuated. This is similar to the passive mixer based impedance translation schemes which provide a -20 dB/decade filtering for out-of-band interferences after the LNTA [1][2][3][4]. The SDSP block combined with the baseband amplifier including feedback R_B and C_F provides a -40 dB/decade filtering right after frequency translation.

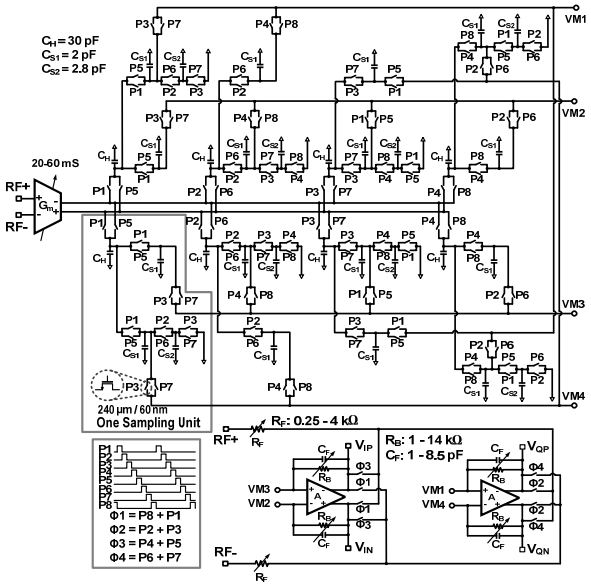

Fig. 3. Signal path circuit schematic of the SDR receiver.

III. Circuit Implementation

A. Signal Path

The receiver front-end LNTA is realized as three inverter-like cells in parallel, each of which can be turned on/off individually (Fig. 4(a)). The complementary stages enable large voltage swing and high transconductance linearity. The subsequent SDSP block schematic is shown in Fig. 3 and discussed in Section II.

B. Clock Scheme

An 8-phase non-overlapping clock scheme is used for 3rd and 5th order harmonic rejection (Fig. 1). A wideband integer-N frequency synthesizer with a fixed division ratio is implemented by a 4-tank Voltage Controlled Oscillator (VCO), shown in Fig. 4(b), to cover the 1 – 6 GHz range. Frequency synthesis is achieved through a programmable reference input provided by a 15 – 93 MHz Digital Direct Synthesizer (DDS). The frequency synthesizer output is tapped after the first divide-by-2 block to cover the 0.5 – 3 GHz RF frequency range. This clock is then used to generate an 8-phase clock by a wideband Delay Locked Loop (DLL). The output 8-phase clock then drives high speed digital logic to generate the 8-phase non-overlapping clocks for the SDSP and the 4-phase non-overlapping clocks for the frequency up-converter in the translational loop.

C. Bias & I/O Interfaces

The chip uses 2.5 V for I/O interfaces and the on-chip regulators with 1.2 V output that supply the noise-sensitive blocks (including the LNTA, and the charge pump of the DLL and the PLL). The SDSP core uses a separate 1.2 V

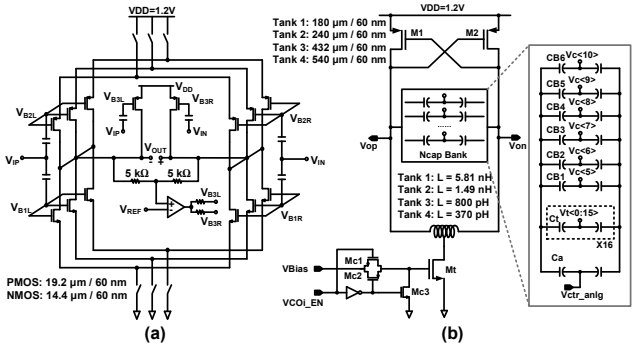

Fig. 4. Circuit schematic of (a) low noise transconductance amplifer, (b) 4-tank VCO.

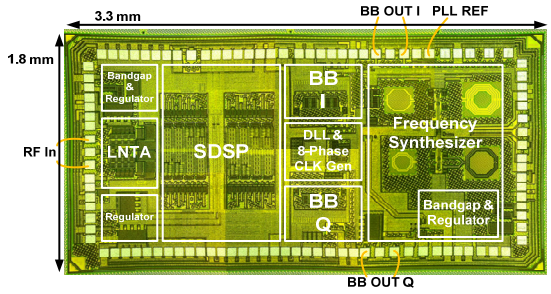

Fig. 5. Chip microphotograph of the SDR receiver.

supply. All pads, including the RF input, contain ESD protection and power clamp circuitries.

IV. Measurement Results

The SDR receiver chip is fabricated in a 65nm LP CMOS process (Fig. 5), packaged in a 48-pin 7 mm x 7 mm QFN, and soldered on a PCB that also includes baseband VGAs, anti-alias filters, and a dual 12-bit 100 MS/s ADC. An off-chip broadband balun is used to convert the RF input signal to differential signals. The quadrature baseband outputs of the receiver are sent to a PC through the USB3.0 port. A frequency programmable DDS produces the PLL reference.

The frequency synthesizer covers the 1 – 6 GHz range continuously with spur level of better than 60 dBc (Fig. 6(a)). Measured K_{VCO} for the 4-tank VCO is shown in Fig. 6(b). Loop filter, charge pump current, and the current of frequency dividers in the frequency synthesizer can be programmed independently to achieve the desired phase noise requirement. Fig. 6(c) shows a representative phase noise profile at 2.4 GHz when the PLL is either on or off. A representative 8-phase non-overlapping clock, when f_{LO} = 0.6 GHz, is shown in Fig. 6(d). The receiver can be continuously tuned to operate anywhere within 0.5 – 3 GHz. Fig.7 illustrates the receiver conversion gain, input reflection coefficient, noise figure and power consumption versus frequency at a few representative settings. The conversion gain is 35 dB at low frequencies and drops to

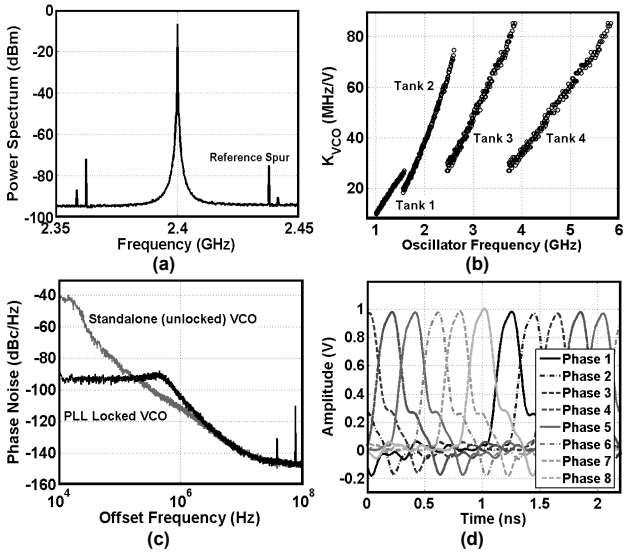

Fig. 6. (a) Measured VCO output spectrum when PLL is locked; (b) Measured K_{VCO} of the oscillator; (c) Measured phase noise when PLL is on and off; (d) Measured outputs of the 8-phase non-overlapping clock generator when DLL is locked.

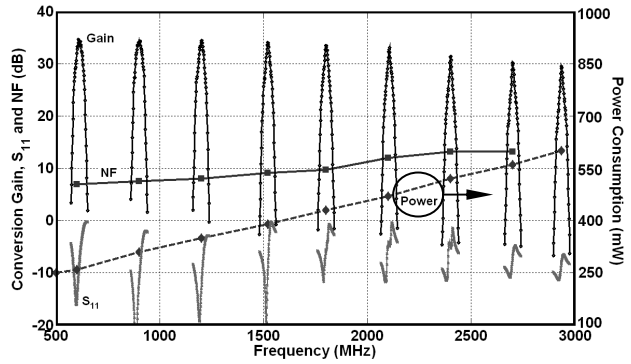

Fig. 7. Measured receiver conversion gain, S_{11} and noise figure for a few representative settings within the 0.5 – 3 GHz input frequency range.

30 dB at 3 GHz. The 5 dB gain loss, which leads to a higher NF at 3 GHz, is partially due to the insertion loss of the off-chip RF balun, and partially due to the overlapping between clock phases at high frequencies. All measurements include the loss of off-chip balun, PCB transmission lines, and all connectors.

The in-band IIP3 and OIP3 for the maximum gain setting are -12.4 dBm and 19 dBm, respectively. The out-of-band IIP3 and IIP2 are 11.7 dBm and 58 dBm, respectively. The out-of-band blocker power that causes 1dB compression point is -1 dBm (Fig. 8). Fig. 9(a) shows the baseband output SNR as a function of blocker power when f_{LO} = 614 MHz. In these measurements, the bandwidth of the band-pass impedance presented by the SDSP to the LNTA is set to $(C_S/C_H)\cdot f_S/\pi$ = 12.5 MHz and the bandwidth of the baseband amplifier is set to $1/(2\pi R_B C_F)$ = 8 MHz. SNR degradation of less than 6 dB

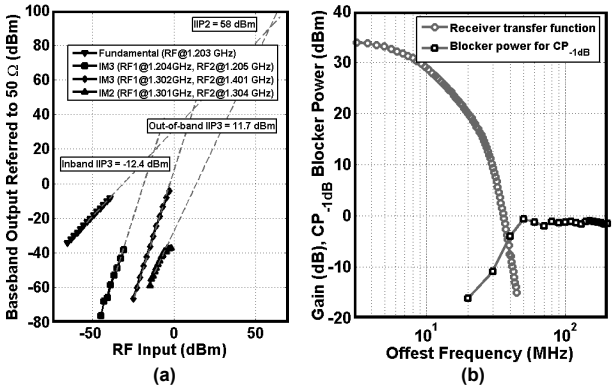

Fig. 8. (a) Measured IIP3 and IIP2; (b) Transfer function and blocker -1dB compression power level versus offset frequency.

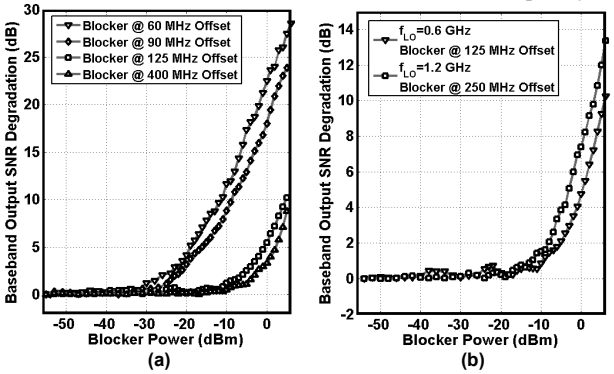

Fig. 9. Output SNR degradation versus blocker power levels at (a) f_{LO} = 614 MHz; (b) two different RF and blocker frequencies.

for out-of-band blockers as large as 0 dBm validates the aforementioned SDSP-based band-pass filtering. When the ratio of C_S/C_H is fixed, the bandwidth of the SDSP input impedance is proportional to the sampling frequency f_S, which tracks f_{RF}. In Fig. 9(b), the ratio of blocker offset frequency and the input frequency is kept constant in the measurements to verify the proper filtering property of the SDSP block. The uncalibrated 3rd order and 5th order harmonic rejections are above 47 dB and 52 dB, respectively. The harmonic rejection ratio is larger in higher RF frequencies due to the front-end low-pass filtering effect.

The overall chip power consumption varies from 250 to 600 mW depending on the LO frequency and other settings (Fig. 7). The main contributors to the overall power consumption are the 8-phase non-overlapping clock generator and the clock buffers which drive the MOS switches in the SDSP block. A key advantage of the proposed architecture is that the 60 – 300 mA current consumption of these blocks directly scales with technology, and can also be reduced significantly through employing common techniques used in low-power digital chips. Table I summarizes the chip performance. The other complete SDR receiver [3], does not achieve any harmonic rejection while it consumes lower power due to a better technology (40nm versus 65nm LP).

TABLE I. PERFORMANCE SUMMARY AND COMPARISON

Parameter	[2]	[3]	[4]	[5]	[6]	This work
CMOS Technology	65nm	40nm	40nm	90nm	90nm	65nm LP
Supply Voltage (V)	1.2 / 2.5	1.2 / 2.5	1.3	1 / 2.5	1.2	1.2 / 2.5 [3]
Frequency (GHz)	0.1 ~ 2.4	0.4 ~ 6	0.08 ~ 2.7	0.8 ~ 6 [2]	0.5 ~ 3.8	0.5 ~ 3
Signal Domain	Continuous	Continuous	Continuous	Continuous + Sample	Sample	Sample
Gain (dB)	40 ~ 70	70	72	>20	60	35
NF (dB)	5.5	3 ~ 7.5	1.5 ~ 2.4	5 @ 0.9 GHz 5.5 @ 2.5 GHz	5.1 ~ 6	6.8 ~ 13.2 [4]
IB IIP_3 (dBm)	-	+6	-	-3.5	-13 ~ -3	-12.4 [5]
OOB IIP_3 (dBm)	+25	+10	13.5		2.5	11.7
IIP_2 (dBm)	58	+70	54	+60	+50	> 58
OOB Blocker Power for CP_{-1dB} (dBm)	-	-8	-	-13.5	-	-1
3rd Order HR (dB)	35.4	No	42	38	No	> 47
5th Order HR (dB)	42.6	No	45	40	No	> 52
HR Frequency Range (GHz)	< 1	-	0.08 ~ 2.7	< 1.05	-	0.5 ~ 3
Frequency Synthesizer (GHz)	No	6 ~ 12	No	0.82 ~ 5.4 [2]	No	1 ~ 6
Phase Noise (dBc/Hz) @ 1MHz offset	-	-	-	-	-	-120 ~ -110
Power Consumption (mW)	30 ~ 70 [1]	64 ~ 100	35 ~ 78 [1]	> 100	47 ~ 115 [1]	250 ~ 600
Area (mm^2)	2	2	2	3.8	0.45	5.9

[1] Without frequency synthesizer.
[2] RF frequency not completely covered from 0.8 to 6 GHz.
[3] 2.5 V only used for regulators and I/O buffers. The core circuit 1.2 V power supply only.
[4] Includes the loss of the off-chip balun and t-lines: 1.3 dB @ 1 GHz, 4.4 dB @ 3 GHz.
[5] IB IIP_3 measured @ max gain setting.

V. CONCLUSIONS

Technology scaling offers transistors with higher speed and lower power consumption for digital operation. RF signal processing leveraging mixed-signal techniques enables reconfigurability and software programmability. A proof-of-concept SDR based on sample domain signal processing was presented that achieves high dynamic range across a wideband frequency range.

ACKNOWLEDGEMENT

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