A Highly-Linear CMOS RF Programmable-Gain Driver Amplifier with a Digital-Step Differential Attenuator for RF Transmitters

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***Abstract* — This paper presents a CMOS RF programmable-gain driver amplifier (RF PGDA) for wireless transmitters. Digital-step differential attenuators precede a programmable-gain amplifier in order to enhance the dynamic range and to save power consumption, especially at low gain region. The RF PGDA fabricated in 0.13-µm CMOS technology with a 1.2 V supply voltage achieves a dynamic range of 49 dB with a step error of less than 0.5 dB and highly-linearized output satisfying the WCDMA/LTE specifications.**

***Index Terms* — Digital-step attenuator, long-term evolution (LTE), programmable-gain amplifier (PGA), RF transmitter, variable-gain amplifier (VGA), wideband code division multiple access (WCDMA).**

I. Introduction

Direct up-conversion RF transmitters have received a lot of attentions because they have structures amenable to single-chip integration in CMOS process. Recently, it has become necessary for RF transmitters of cellular standards to have a high dynamic range, *e. g.*, more than 74 dB for wideband code division multiple access (WCDMA). Thus, a RF programmable-gain amplifier (PGA) has become an essential block in a direct up-conversion RF transmitter to cover the high dynamic range by cooperating with a baseband variable-gain amplifier.

In this paper, we propose a fully-integrated CMOS RF programmable-gain driver amplifier (RF PGDA) for a direct up-conversion RF transmitter targeting WCDMA and long-term evolution (LTE), which obtains increased dynamic range by using a digital-step differential attenuator and amplifies the output power of a mixer up to a sufficient level for driving a following power amplifier (PA) at high gain region. In addition, it enables fine control of the dynamic range by turning on/off shunt switches beside the common-gate transistors of a cascode amplifier. Moreover, the implemented RF PGDA adopts linearization techniques to keep delivering highly-linearized output at every state of gain setting.

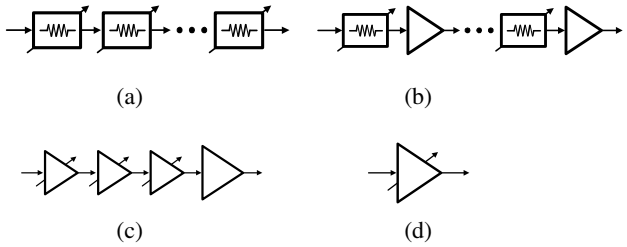


Fig. 1. RF PGA structure. (a) Only attenuators. (b) Series of an attenuator with an amplifier [1]. (c) Cascaded PGAs [2]. (d) Single-stage PGA [3].

II. RF PGDA Design

A. Previous Works on RF PGAs

Fig. 1 shows simplified structures of previously reported RF PGAs. Fig. 1(a) is composed of only attenuators. Although it is known that the utilization of only RF attenuators as a transmit power control unit consumes less DC power than a RF PGA, an additional RF amplifier next to the attenuator is required because the output power of a typical mixer at the preceding stage of the attenuator is not high enough to directly drive a following power amplifier. In Fig. 1(b), authors present multiple stages consisting of a series of attenuator with fixed-gain RF amplifier to acquire both wide dynamic range and sufficient output power, which result in large noise in the receiver band at 190 MHz offset and large power consumption even at low gain region. In Fig. 1(c), several PGAs are cascaded to enhance dynamic range because gain control range per one PGA is limited due to the linearity degradation at low gain region. As a result, the occupied area on a chip is increased and power consumption becomes large. Fig. 1(d) adopts binary-weighted transconductance cells using *R-2R* ladder structure to enhance the dynamic range with only one stage of PGA. Thus, it achieves low noise, high dynamic range, and high accuracy of gain step. However, its supply

voltage is 2.8 V and power consumption at low gain mode is still high.

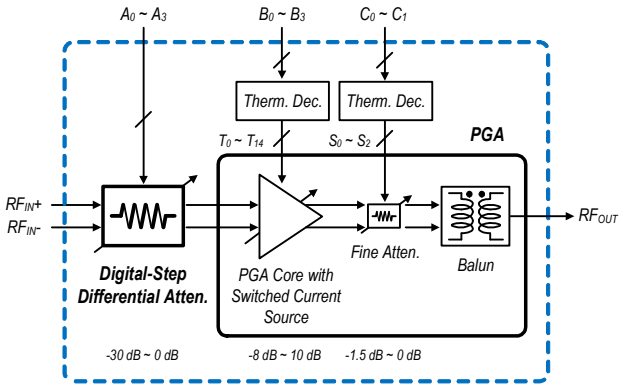


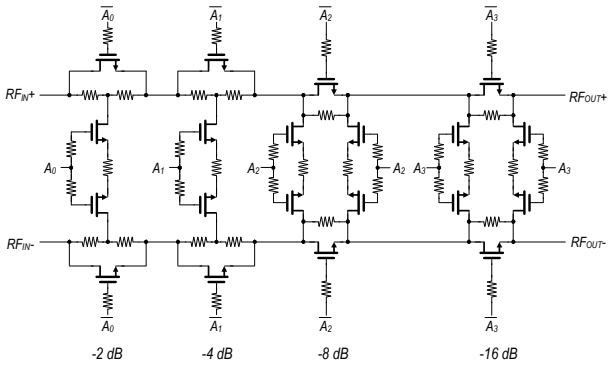
Fig. 2. Proposed RF PGDA structure.

B. Proposed RF PGDA Architecture

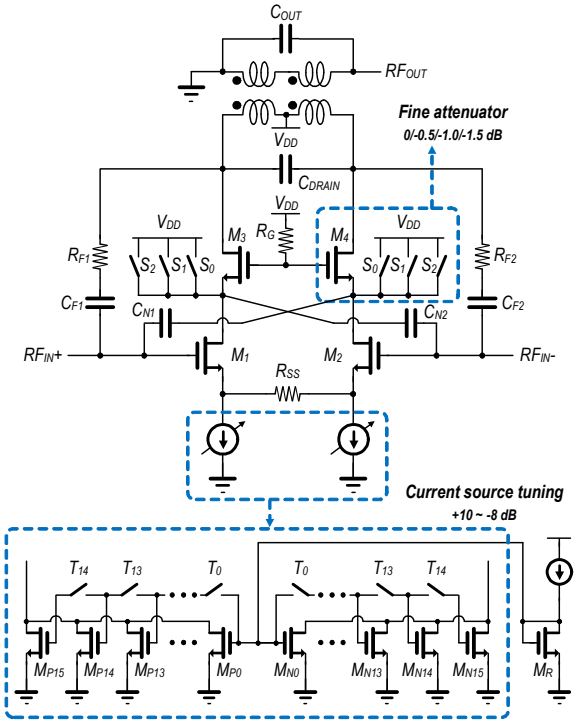
Fig. 2 shows the architecture of the proposed RF PGDA. It consists of a digital-step differential attenuator, a PGA core, a fine attenuator, and a balun.

The digital-step differential attenuator conducts a coarse power control with a dynamic range up to 30 dB with a 2 dB step via 4-bit digital control. Fig. 3(a) shows the schematic of the designed digital-step differential attenuator. The fundamental architecture is based on the switched T-type for -2 dB/-4 dB attenuator stages and the switched -type for -8 dB/-16 dB attenuator stages, as demonstrated in [6]. Compared with [6], the attenuator structure in this work is modified to have differential input/output interfaces because both the output port of a typical mixer and the input port of the designed PGA of this work are differential. Another difference is that 0.5 dB and 1.0 dB attenuator stages are removed to reduce the occupied area.

The PGA section of this work covers the dynamic range from -8 dB to +10 dB, as indicated in Fig. 2. Fig. 3(b) describes its simplified schematic. The main part of the designed PGA is based on a differential cascode amplifier with transistors, M_1–M_4. The transconductance of the PGA is controlled by turning on/off the switches, T_0–T_{14}, in the current sources. The feedback resistors, R_{F1} and R_{F2}, significantly linearizes the output of the PGA near maximum gain region even when its power level is as high as that of a typical driver amplifier, in spite of the low supply voltage (V_{DD}=1.2 V). In addition, cross-coupled capacitors, C_{N1} and C_{N2}, are inserted to neutralize the nonlinear Miller effect of the gate-drain parasitic capacitance at M_1 and M_2 [4]. For the purpose that the effective input capacitance seen at the gate of M_1 or M_2 becomes less dependent of the small signal gain of the common-source stage, $C_{N1,2}$ is set almost equal to the gate–drain parasitic capacitance of M_1 or M_2 as long as the stability of the circuit is guaranteed.



(a)



(b)

Fig. 3. Schematics of the proposed RF PGDA. (a) Digital-step differential attenuator. (b) PGA.

The fewer current sources are turned on at low gain region, the more third harmonic distortion is generated. The source degeneration resistor, R_{SS}, helps the PGA reducing the third harmonic distortion at low gain region [5].

Additional fine control is simply realized using shunt switches to V_{DD} at the common-gate stage, as shown in Fig. 3(b). The amount of current flowing through the drain–source of M_3 or M_4 is delicately attenuated by turning on the shunt switches, S_0–S_2, so this enables the power to be controlled with a 0.5 dB step instead of using finer step attenuators in the preceding digital-step differential attenuator section. If the size of switches is reduced and the number of them is increased, much finer control of dynamic range is feasible.

Signal conversion from differential to single-ended form at the final output stage is implemented by means of an on-chip transformer, which also simplifies the output matching network and enables fully-integration of the overall RF PGDA.

In order to reduce power consumption at low gain region, the power control from maximum gain to minimum gain is conducted with the following sequence: current sources of the PGA are firstly turned off, then the digital-step attenuators are switched on turn by turn until reaching the minimum gain. Below the gain of -10 dB, only one current source of the PGA is turned on.

III. MEASUREMENT RESULTS

The proposed RF PGDA was fabricated in 0.13-μm CMOS process. Fig. 4 shows the implemented chip photograph. The total size including the ESD protection devices and bonding pads is 2.1 mm × 0.9 mm.

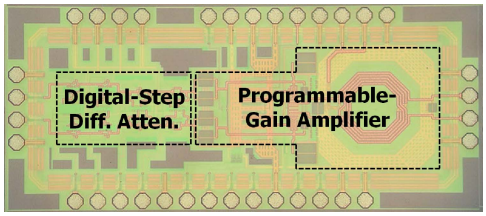


Fig. 4. Chip photograph.

Fig. 5(a), (b), and (c) show the measurement results of a 1-tone continuous-wave (CW) input. According to Fig. 5(a), gain of each state stays flat up to the input power of 0 dBm at 1.95 GHz. Fig. 5(b) indicates that output power of each gain setting with 0 dBm input power is also flat within band I uplink region. Fig. 5(c) shows the measurement result of the output power and 1 dB gain step error with respect to the gain setting when a 1-tone CW signal with 0 dBm at 1.95 GHz is introduced, which shows that the maximum absolute value of the 1 dB step error does not exceed 0.5 dB. The RF PGDA of this work is designed under the criterion that IMD3 is below -40 dB at every stage of gain setting and Fig. 6 verifies its validity using a 2-tone test.

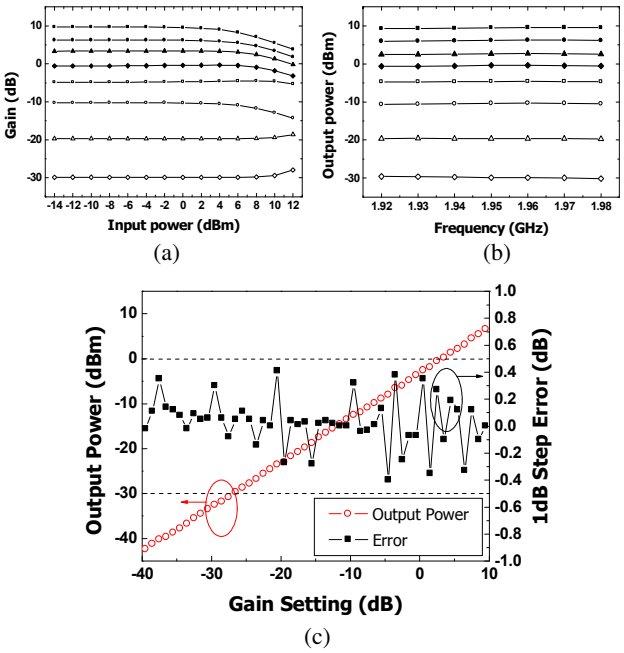


Fig. 5. Measurement results with a 1-tone CW input. (a) Gain vs. input power. (b) Output power vs. frequency. (c) Output power and 1 dB step error vs. gain setting.

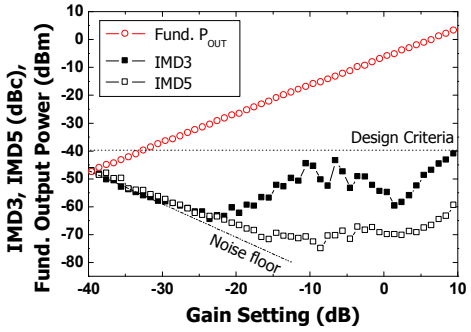
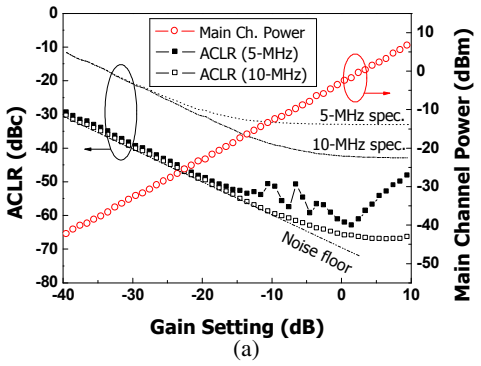
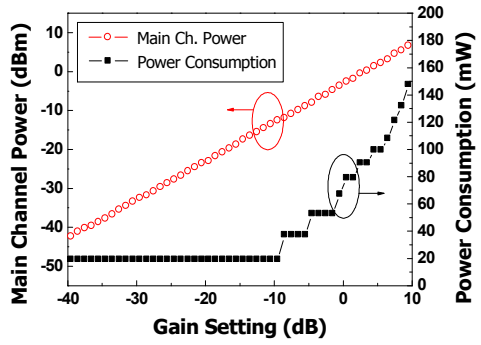


Fig. 6. IMD3, IMD5, and fundamental output power (one-side) vs. gain setting with 2-tone input (5 MHz space).

Fig. 7(a) shows the measured ACLR and main channel power with a WCDMA-modulated signal of -3 dBm at 1.95 GHz. The main channel power varies from -42.36 dBm to 6.6 dBm in 1 dB steps according to the gain setting, which is adjusted by digital control words, with ACLR satisfying the 3GPP specification. The DC power consumption is 145.2 mW at the maximum gain setting and 18.0 mW at the minimum gain setting, as shown in Fig. 7(b). The WCDMA performances are summarized and compared with [1] in Table I.



(a)



(b)

Fig. 7. Measurement results with a WCDMA signal. (a) ACLR and main channel power vs. gain setting. (b) Main channel power and power consumption vs. gain setting.

TABLE I
PERFORMANCE COMPARISON USING A WCDMA SIGNAL WITH 5 MHZ CHANNEL BANDWIDTH

Reference	[1]	This work
Supply voltage (V)	1.5/2.5	1.2
Max. output power at main channel (dBm)	4.0	6.6
1 dB gain step error (abs.) (dB)	< 1.0	< 0.5
Power consumption @ max. gain (mW)	100.0	145.2
Power consumption @ min. gain (mW)	67.5	18.0
ACLR (5/10 MHz) @ max. gain (dBc)	-48/-60	-48/-66
Error vector magnitude (RMS) (%)	< 1	< 1.7
Output noise @ 190 MHz offset (dBm/Hz)	< -136	< -153.4

TABLE II
PERFORMANCE COMPARISON USING A LTE SIGNAL WITH 20 MHZ CHANNEL BANDWIDTH

Reference	[3]	This work
Supply voltage (V)	2.8	1.2
Max. output power at main channel (dBm)	3.4	3.4
Power consumption @ P_{OUT} = 0 dBm (mW)	103	106
Power consumption @ P_{OUT} = -24 dBm (mW)	36.1	18.0
ACLR (20/40 MHz) @ P_{OUT} = 0 dBm (dBc)	-40/–	-54/-61

For a fair comparison with the RF PGA in [3], we measured the performance with a LTE-modulated signal centered at 1.95 GHz. The performance is compared in Table II, which shows higher linearity at an output power of 0 dBm and lower power consumption at an output power of -24 dBm.

IV. CONCLUSION

A new architecture of a RF PGDA with a digital-step differential attenuator is proposed. The implemented chip features highly linear output up to sufficient level as a driver amplifier, low power consumption even at low gain region, and high dynamic range of 49 dB with a step error of less than 0.5 dB. The experimental results exhibit a maximum output power of 6.6 dBm satisfying 3GPP ACLR specification, power consumption of 18 mW at an output power of -42.36 dBm for WCDMA and applicable performances for even LTE with a bandwidth of 20 MHz.

ACKNOWLEDGEMENT

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